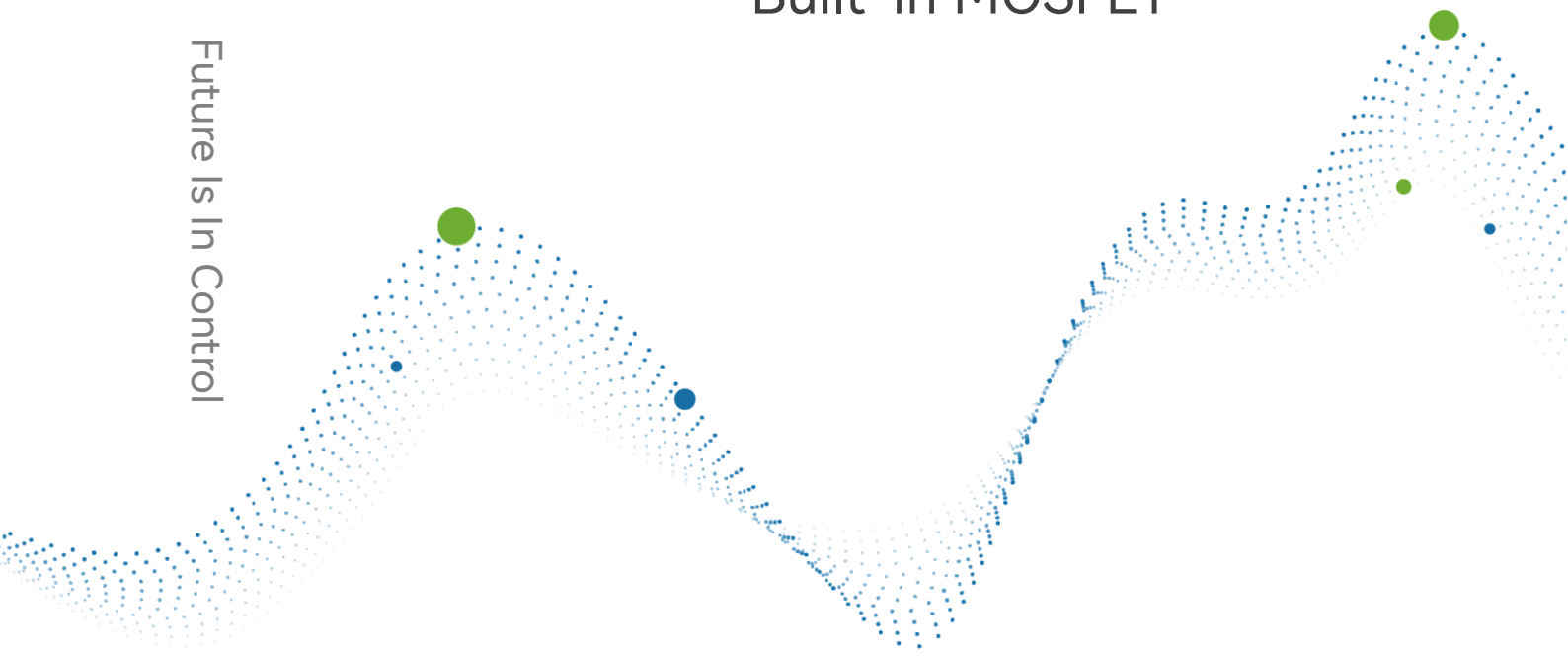
Fortior Tech

DATASHEET

FT8215

Three-phase BLDC Motor Controller with Built-in MOSFET

Future Is In Control



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Contents

1 System Introduction

1.1 Overview

FT8215 is a highly integrated IC with built-in MOSFET for three-phase BLDC motor drive applications. Due to a high level of integration, the chip has few peripheral components and features with low noise and small torque ripple. Motor parameters, startup control parameters and speed regulation mode can be configured via GUI, and are stored in built-in EEPROM. Analog voltage input, PWM, I²C interface or CLOCK mode is available for motor speed regulation. Moreover, the chip integrates speed indicator to read motor speed in real time via FG/RD/SDA or SPEED/SCL pin. Constant speed control mode, constant current control mode, constant power control mode or voltage-loop control mode is optional. In addition, the chip is secured with a wide range of protection features, including over-current protection (OCP), temperature sensor detect (TSD), motor lock protection (MLP), under-voltage lockout (UVLO), phase loss protection, etc. Sleep-mode current of the chip is about 40μA.

1.2 Applications

FT8215Q: Floor fans, cooling fans, etc.

FT8215P: Floor fans, cooling fans, and laptop cooling fans etc.

FT8215Q

FT8215P

1.3 Features

- Sensorless FOC
- Built-in MOSFET
- Constant speed control mode, constant current control mode or voltage-loop control mode is optional
- Analog voltage input, PWM, I²C interface or CLOCK mode for motor speed regulation
- I²C interface for motor control or motor states feedback
- Rotor initial position detection
- Tailwind and headwind detection
- Soft-on, Soft-off
- Average drive current:
  - FT8215Q: 2A
  - FT8215P: 1.05A
- Built-in EEPROM
- Configurable multi-segment output curve
- Protection features, including OCP, UVLO, TSD, MLP, phase loss protection, etc.
- Forward or reverse rotation selectable
- FG and RD output

1.4 Application Diagram

Due to space limitations in the diagram layout, the following abbreviations are used in the application circuit: ASPEED is abbreviated as ASPD, SPEED/SCL as SPD, FG/RD/SDA as FG.

1.4.1 FT8215Q

Figure 1-1 Typical Application Diagram of FT8215Q (Single-shunt Current Sampling)

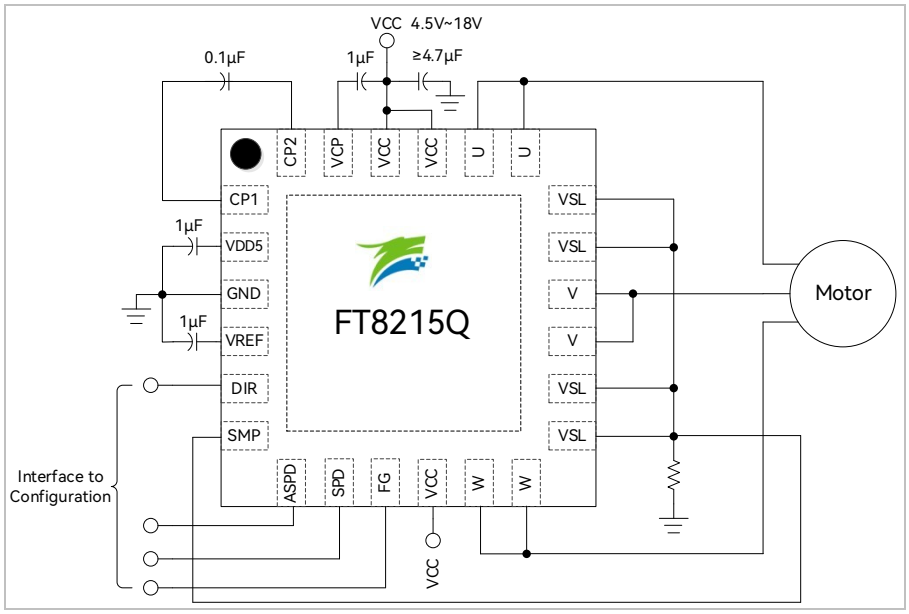
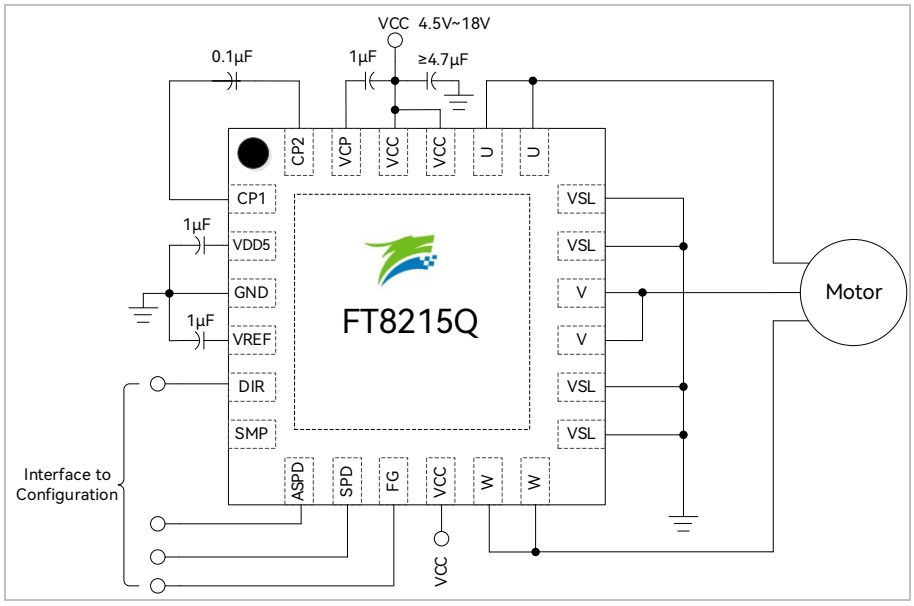


Figure 1-2 Typical Application Diagram of FT8215Q (Dual/Triple-shunt Current Sampling)



1.4.2 FT8215P

Figure 1-3 Typical Application Diagram of FT8215P (Single-shunt Current Sampling)

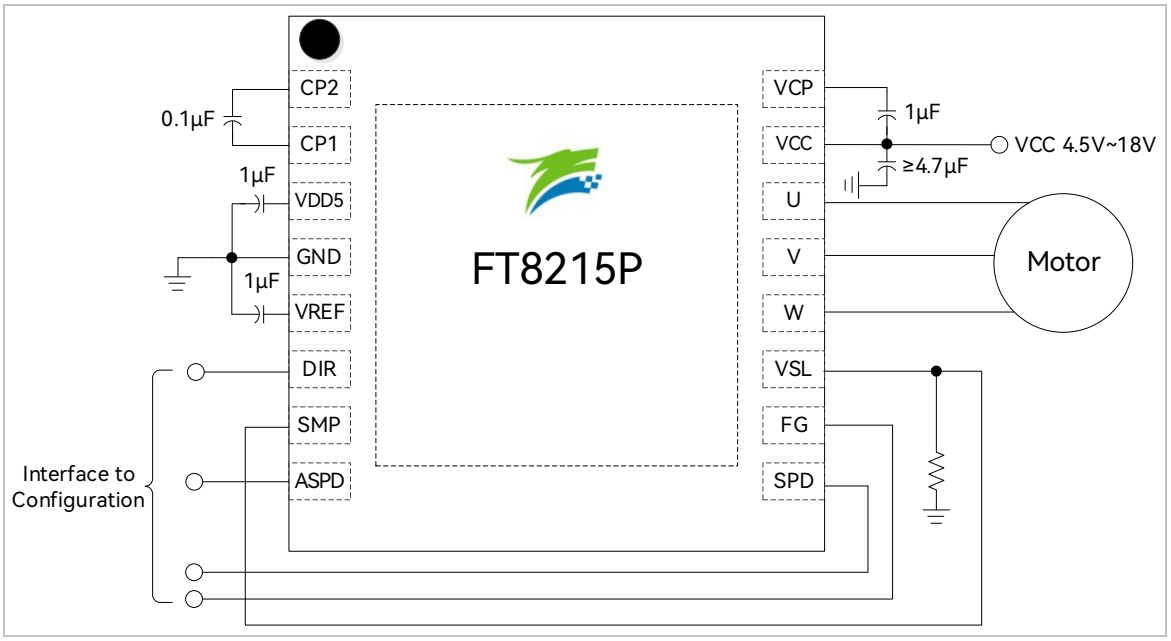
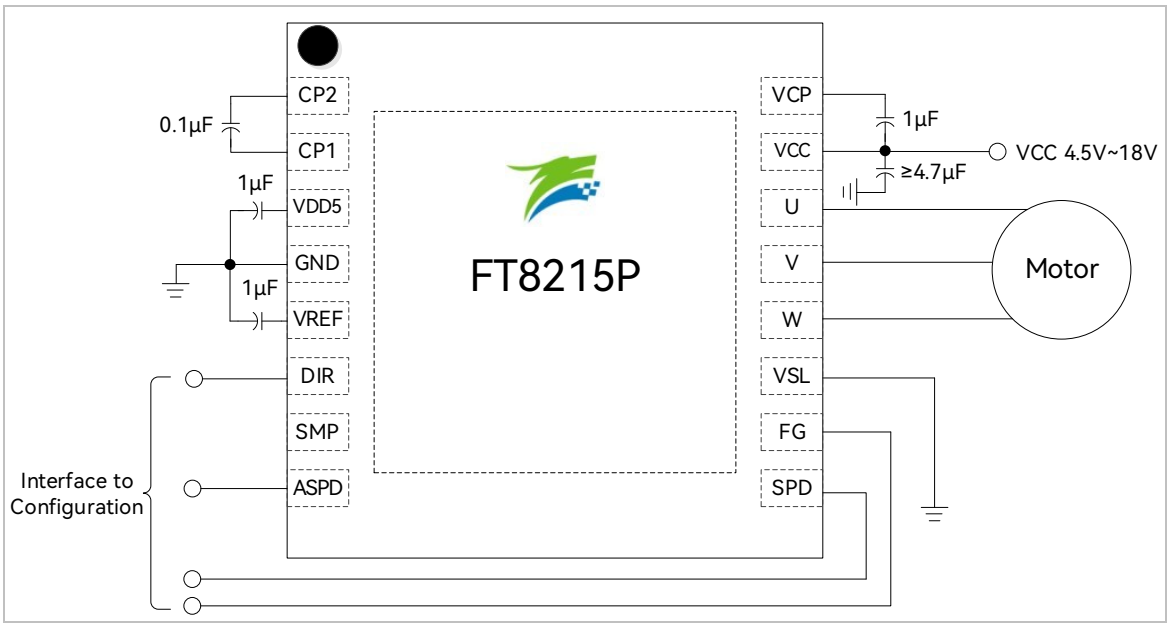
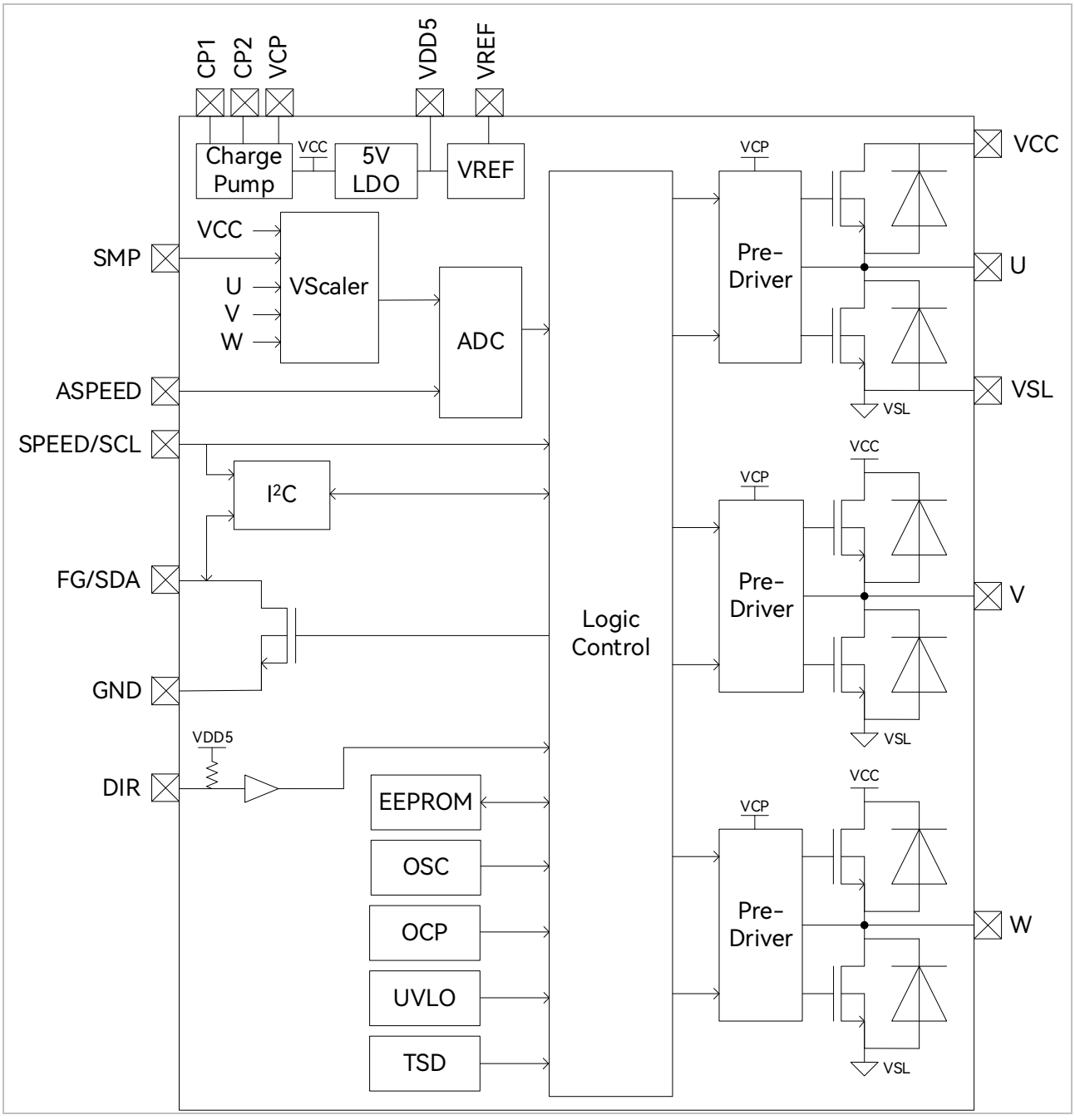


Figure 1-4 Typical Application Diagram of FT8215P (Dual/Triple-shunt Current Sampling)



1.5 Functional Block Diagram

Figure 1-5 Functional Block Diagram of FT8215Q / FT8215P



1.6 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- DB = Digital Bidirectional
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

1.6.1 FT8215Q QFN24 Pins

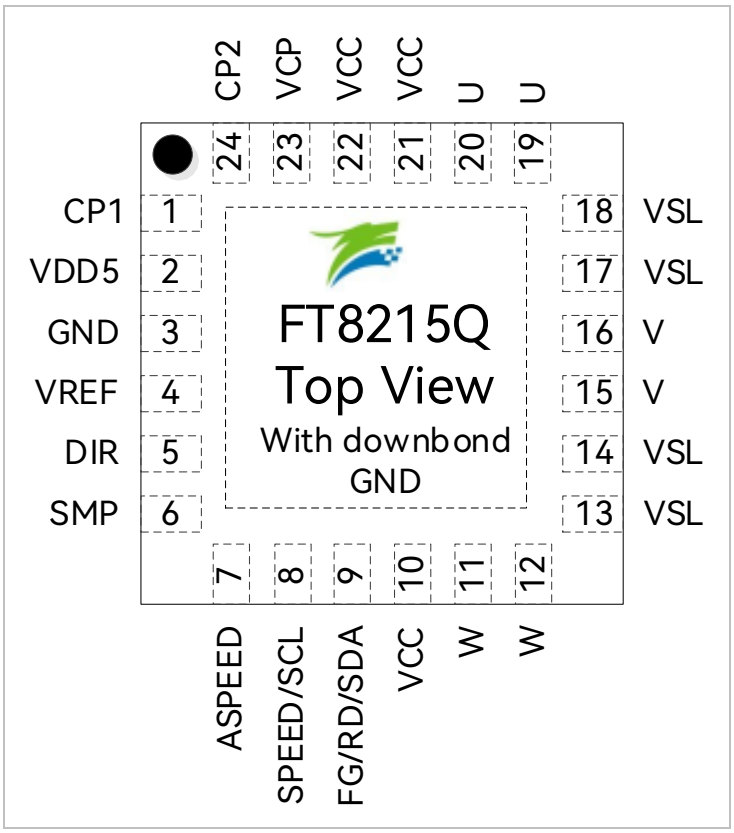
Table 1-1 FT8215Q QFN24 Pin Descriptions

Pin	FT8215Q QFN24	IO Type	Function Descriptions
CP1	1	AO	Charge pump pin, with a 1μF capacitor connected to CP2 pin
VDD5	2	P	5V LDO output with a 1μF ~ 4.7μF capacitor connected to ground
GND	3	P	Ground
VREF	4	AI	ADC reference voltage, with a 1μF external capacitor connected to ground
DIR	5	DI	Motor rotation control, with built-in pull-up resistor 0: Reverse rotation. U --> W --> V. 1: Forward rotation. U --> V --> W.
SMP	6	AI	Bus current sampling input
ASPEED	7	AI	Analog voltage input for motor speed regulation
SPEED/ SCL	8	DI/ DB	Input of PWM or CLOCK mode-based speed regulation I²C SCL
FG/RD/ SDA	9	DO/ DB	Motor speed signal or motor block indication, with collector open-drain output I²C SDA
VCC	10	P	Input power supply
W	11	DO	W-phase output
W	12	DO	W-phase output
VSL	13	DO	Low-side ground output
VSL	14	DO	Low-side ground output
V	15	DO	V-phase output
V	16	DO	V-phase output
VSL	17	DO	Low-side ground output
VSL	18	DO	Low-side ground output

Pin	FT8215Q QFN24	IO Type	Function Descriptions
U	19	DO	U-phase output
U	20	DO	U-phase output
VCC	21	P	Power input, 4.5V ~ 18V DC, with a capacitor of 4.7μF or above connected to ground
VCC	22	P	Input power supply
VCP	23	P	Charge pump output, with a 1μF~4.7μF capacitor connected to VCC pin
CP2	24	AO	Charge pump pin, with a 0.1μF capacitor connected to CP1 pin

1.6.2 FT8215Q QFN24 Pinout Diagram

Figure 1-6 FT8215Q QFN24 Pinout Diagram



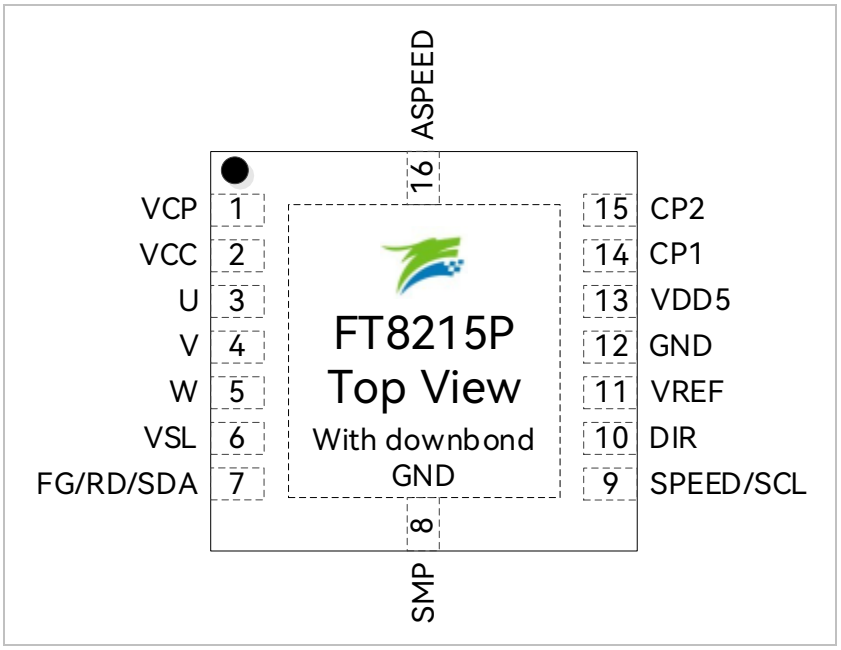
1.6.3 FT8215P PLQFN16 Pins

Table 1-2 FT8215P PLQFN16 Pin Descriptions

Pin	FT8215P PLQFN16	IO Type	Function Descriptions
VCP	1	P	Charge pump output, with a 1μF~4.7μF capacitor connected to VCC pin
VCC	2	P	Power input, 4.5V ~ 18V DC, with a capacitor of 4.7μF or above connected to ground
U	3	DO	U-phase output
V	4	DO	V-phase output
W	5	DO	W-phase output
VSL	6	DO	Low-side ground output
FG/RD/ SDA	7	DO/ DB	Motor speed signal or motor block indication, with collector open-drain output I^2C SDA
SMP	8	AI	Bus current sampling input
SPEED/ SCL	9	DI/ DB	Input of PWM or CLOCK mode-based speed regulation I^2C SCL
DIR	10	DI	Motor rotation control, with built-in pull-up resistor 0: Reverse rotation. U --> W --> V. 1: Forward rotation. U --> V --> W.
VREF	11	AI	ADC reference voltage, with a 1μF external capacitor connected to ground
GND	12	P	Ground
VDD5	13	P	5V LDO output with a 1μF ~ 4.7μF capacitor connected to ground
CP1	14	AO	Charge pump pin, with a 1μF capacitor connected to CP2 pin
CP2	15	AO	Charge pump pin, with a 0.1μF capacitor connected to CP1 pin
ASPEED	16	AI	Analog voltage input for motor speed regulation

1.6.4 FT8215P PLQFN16 Pinout Diagram

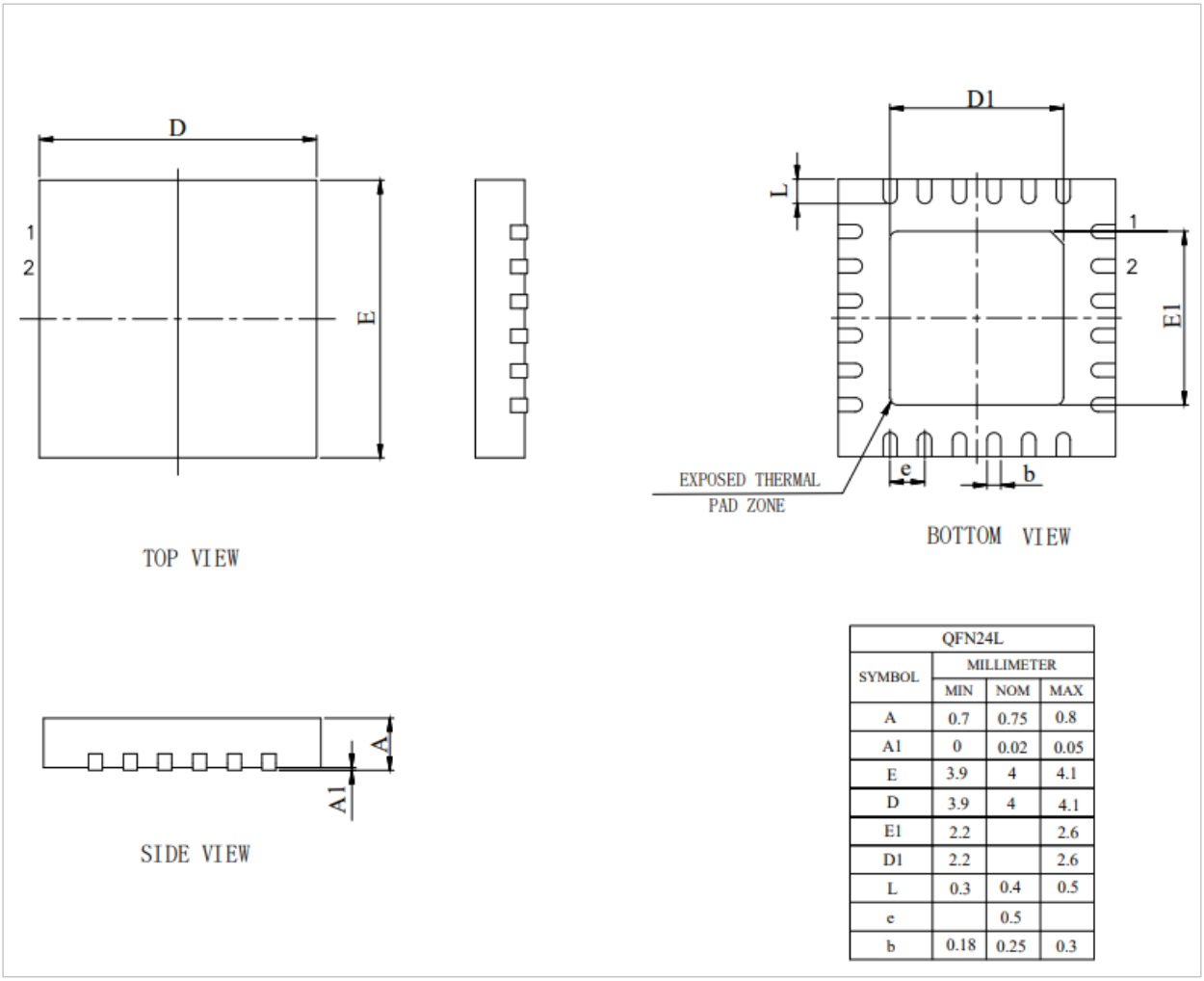
Figure 1-7 FT8215P PLQFN16 Pinout Diagram



2 Package Information

2.1 FT8215Q QFN24_4X4 Package Drawings and Dimensions

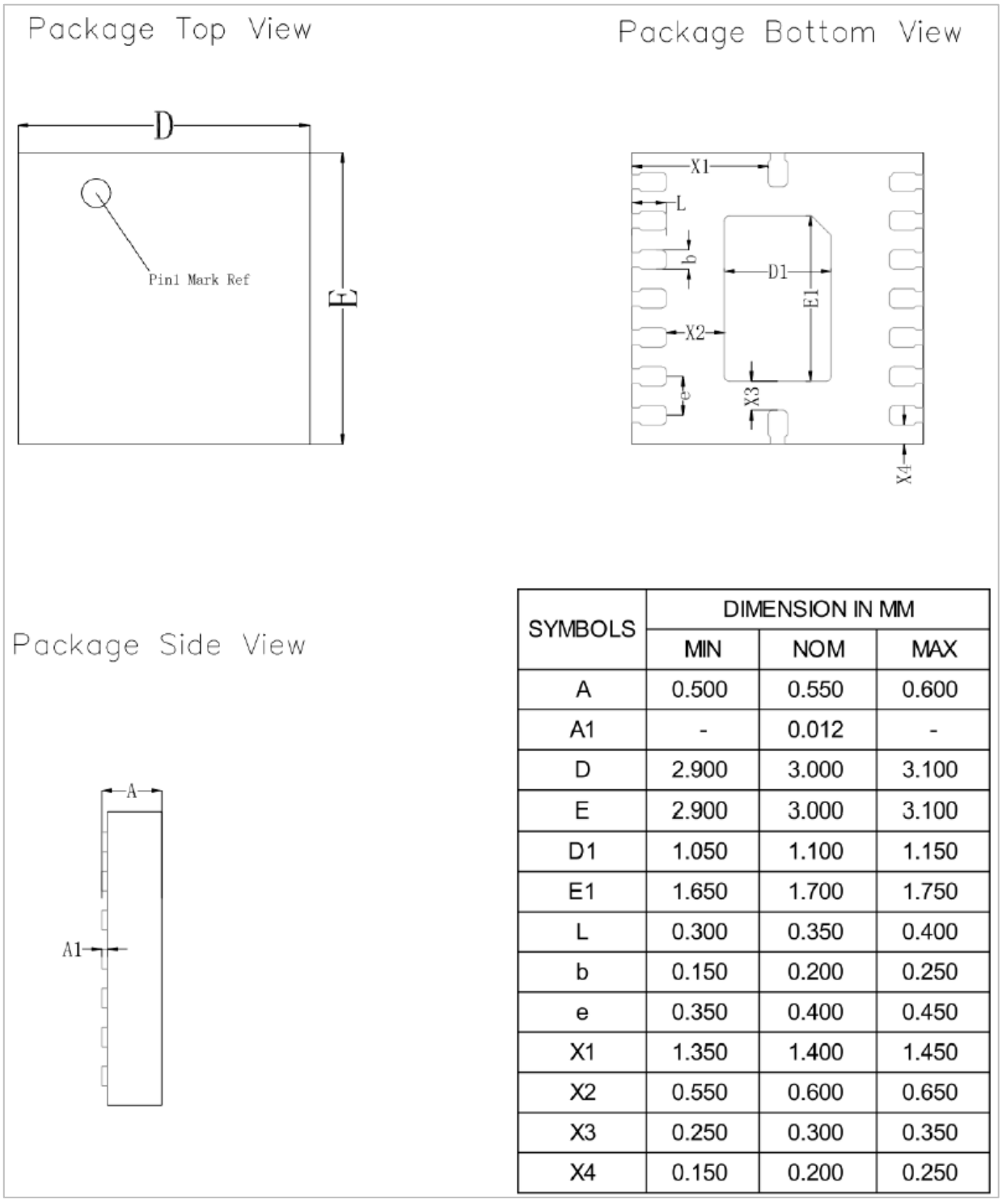
Figure 2-1 FT8215Q QFN24_4X4 Package Drawings and Dimensions



QFN24L			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
E	3.9	4	4.1
D	3.9	4	4.1
E1	2.2		2.6
D1	2.2		2.6
L	0.3	0.4	0.5
e		0.5	
b	0.18	0.25	0.3

2.2 FT8215P PLQFN16_3X3 Package Drawings and Dimensions

Figure 2-2 FT8215P PLQFN16_3X3 Package Drawings and Dimensions



SYMBOLS	DIMENSION IN MM		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	-	0.012	-
D	2.900	3.000	3.100
E	2.900	3.000	3.100
D1	1.050	1.100	1.150
E1	1.650	1.700	1.750
L	0.300	0.350	0.400
b	0.150	0.200	0.250
e	0.350	0.400	0.450
X1	1.350	1.400	1.450
X2	0.550	0.600	0.650
X3	0.250	0.300	0.350
X4	0.150	0.200	0.250

3 Ordering Information

Table 3-1 Model Selections

Model	Power supply(V)	Rdson (High Side + Low Side) (Ω)	Average Drive Current (A)	Control Features						Protection Features					Operating Junction Temperature T_J(°C)	Lead-free	Package
				Drive Type	Speed Regulation			Forward and Reverse Rotation	Initial Position Detection	OCP	TSD	UVLO	MLP	Phase Loss Protection			
					I^2C	PWM/CLOCK	Analog Voltage										
FT8215Q	4.5~ 18	0.25	2	Sensorless Sine-wave	√	√	√	√	√	√	√	√	√	√	-40 ~ 150	√	QFN24 (4 x 4mm)
FT8215P	4.5~ 18	0.25	1.05	Sensorless Sine-wave	√	√	√	√	√	√	√	√	√	√	-40 ~ 150	√	PLQFN16 (3 x 3mm)

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

(T_A = 25℃ and V_{CC} = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature T_{STG}		-55	-	150	℃
VCC to VSS Voltage		-0.3	-	22	V
VDD5 to VSS Voltage		-0.3	5	6.5	V
FG/U/V/W/CP1 to VSS Voltage		-0.3	-	VCC + 0.3	V
VSL to VSS Voltage		-0.3	-	0.5	V
VCP/CP2 to VSS Voltage		-0.3	-	VCC + 6.0	V
VREF/DIR/SMP/ASPEED/SPEED to VSS Voltage		-0.3	-	VDD5 + 0.3	V

Attention

Stress values greater than Table 4-1 "Absolute Maximum Ratings" listed above may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

4.2 Global Electrical Characteristics

4.2.1 FT8215Q

Table 4-2 Global Electrical Characteristics of FT8215Q

(T_A = 25℃ and V_{CC} = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage		4.5	-	18	V
VDD5 Operating Voltage	VCC > 5.5V; I = 0mA ~ 10mA	4.8	5	5.2	V
VREF Reference Voltage		4.3	4.5	4.7	V
VCC Operating Current I_{VCC}	T_A = 25℃ (Average)	-	-	2	A

	T_A = 85℃ (Average)	-	-	1.8	A
VCC Sleep-mode Current $I_{VCC-SLEEP}$		-	36	-	μA
Peak Phase Current I_{PHASE}	Sinusoidal Peak Current	-	-	3.0	A
Rdson (high-side MOS + low-side MOS)		-	0.25	0.4	Ω

4.2.2 FT8215P

Table 4-3 Global Electrical Characteristics of FT8215P

(T_A = 25℃ and V_{CC} = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage		4.5	-	18	V
VDD5 Operating Voltage	VCC > 5.5V; I = 0mA ~ 10mA	4.8	5	5.2	V
VREF Reference Voltage		4.3	4.5	4.7	V
VCC Operating Current I_{VCC}	T_A = 25℃ (Average)	-	-	1.05	A
	T_A = 85℃ (Average)	-	-	0.9	A
VCC Sleep-mode Current $I_{VCC-SLEEP}$		-	36	-	μA
Peak Phase Current I_{PHASE}	Sinusoidal Peak Current	-	-	3.0	A
Rdson (high-side MOS + low-side MOS)		-	0.25	0.4	Ω

4.3 Protection Electrical Characteristics

Table 4-4 Protection Electrical Characteristics

(T_A = 25℃ and V_{CC} = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Under-voltage Lockout V_{UVLO}		3.2	3.5	3.8	V
VCC UVLO Hysteresis Voltage $V_{UVLO-HYS}$		-	0.5	-	V
I_{OCP} OCP Threshold Current		3.5	4.0	4.5	A
T_{TSD} TSD Threshold Temperature		-	165	-	℃
T_{TSD_HYS} TSD Hysteresis Temperature		-	15	20	℃

4.4 IO Electrical Characteristics (DIR/SPEED/ASPEED)

Table 4-5 IO Electrical Characteristics (DIR/SPEED/ASPEED)

(T_A = 25℃ and V_{CC} = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Voltage V_{IH}		2.5	-	VDD5	V
Low-level Input Voltage V_{IL}		0	-	0.6	V

SPEED/DIR/ASPEED Pull-up Resistor	SPEED pin in PWM/CLOCK speed regulation mode	-	33	-	kΩ
SPEED Pull-down Resistor		-	21	-	kΩ

4.5 PWM/CLOCK Input Frequency

Table 4-6 PWM/CLOCK Input Frequency

(T_A = 25℃ and V_{CC} = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWM Input Frequency		20	-	100k	Hz
CLOCK Input Frequency		20	-	1400	Hz

4.6 Analog Voltage Input for Speed Control

Table 4-7 Analog Voltage Input for Speed Control

(T_A = 25℃ and V_{CC} = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ASPEED Input Voltage		0	-	VREF	V

4.7 Package Thermal Resistance

4.7.1 FT8215Q QFN24 Package Thermal Resistor

Table 4-8 QFN24 Package Thermal Resistance of FT8215Q

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	50	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	25	℃/W

4.7.2 FT8215P PLQFN16 Package Thermal Resistor

PLQFN16 Package Thermal Resistor of FT8215P41

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	90	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	45	℃/W

Note

[1] The actual measurements may vary depending on the conditions

5 Function Descriptions

5.1 VREF

VREF is applied to internal digital logic and analog circuits only, and cannot be used for external circuits. A capacitor of 1μF or above shall be added at VREF pin to stabilize the power supply.

5.2 DIR

Forward or reverse direction control (DIR) pin is used to reverse motor rotation by changing the DIR level. Pull-ups make the pin state as "High" (or "1") by default.

5.3 SMP

SMP pin is used as the input of bus current sampling in single-shunt current sampling mode.

5.4 ASPEED

Analog voltage for motor speed regulation (ASPEED) pin is used to input analog voltage for speed regulation.

5.5 SPEED/SCL

Speed control (SPEED) pin is used to input duty cycle for speed regulation depending on the settings. In addition, SPEED pin serves as the clock line (SCL) for I^2C communication.

5.6 FG/RD/SDA

Speed detection and fault indication (FG/RD/SDA) pin is an open-drain output. When this pin is set to FG, it outputs speed feedback signal to indicate rotation speed of the motor, and when it is set to RD, it outputs high-level signal to indicate the fault state. In addition, the pin serves as the data line (SDA) for I^2C communication.

5.7 VSL

In single-shunt current sampling mode, this pin is connected to ground with the sampling resistor. In dual/triple-shunt current sampling mode, this pin is short to ground. VSL to VSS voltage cannot be over 0.5V.

5.8 Speed Control

5.8.1 Speed Control Modes

The chip supports four types of speed control input interface: PWM, analog voltage, I^2C and CLOCK, and only one of them can be chosen at a time. If analog voltage is selected, voltage value input to the ASPEED pin controls the speed; if PWM or CLOCK is selected, duty cycle of PWM or CLOCK signal input to SPEED pin controls the speed/SCL; and if I^2C is selected, SPEED/SCL pin serves as the clock line (SCL) and FG/RD/SDA pin as the data line (SDA).

5.8.2 Speed Control Curve

The control waveform is presented as below, where x-coordinate refers to the duty cycle of PWM input (In I^2C control and analog control modes, the input can be converted to the corresponding PWM duty cycle), and y-coordinate refers to the output duty cycle, which represents different physical quantities in different control modes.

The y-coordinate represents Duty in voltage-loop control mode. The multi-segment speed control curve is obtained by setting five output duty cycle reference points. The start point is determined by X_ON, and the maximum duty cycle PWM_X98 can be set as 98% or 100%. The three inflection points of speed regulation curve are fixed at 25%, 50% and 75%, and the corresponding output reference Y_ON, Y_25, Y_50, Y_75 and Y_MAX are configurable.

Figure 5-1 Multi Segment Output Curve in Voltage-loop Control Mode (PwmOffMode = 0)

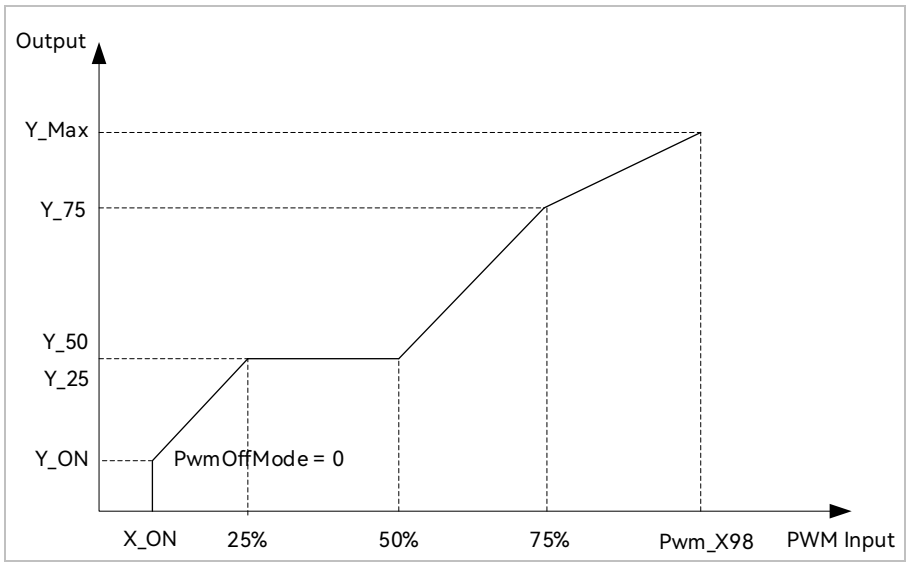
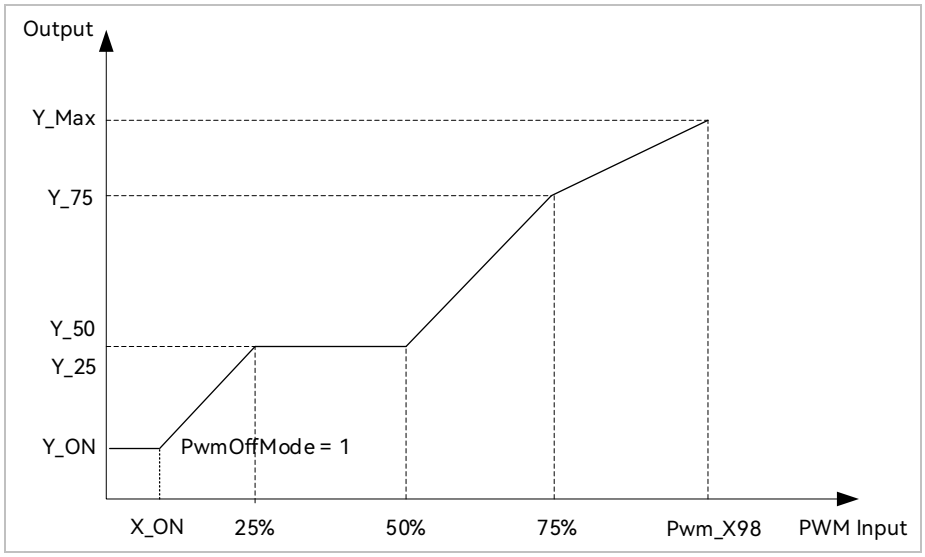


Figure 5-2 Multi Segment Output Curve in Voltage-loop Control Mode (PwmOffMode = 1)



In speed-loop/current-loop/power-loop control mode, y-coordinate represents motor speed/current In this case, only Y_ON and Y_MAX are configurable, and the output of other points between them increases linearly as the input varies.

Figure 5-3 Output Curve in Speed-loop or Current-loop Control Mode (PwmOffMode = 0)

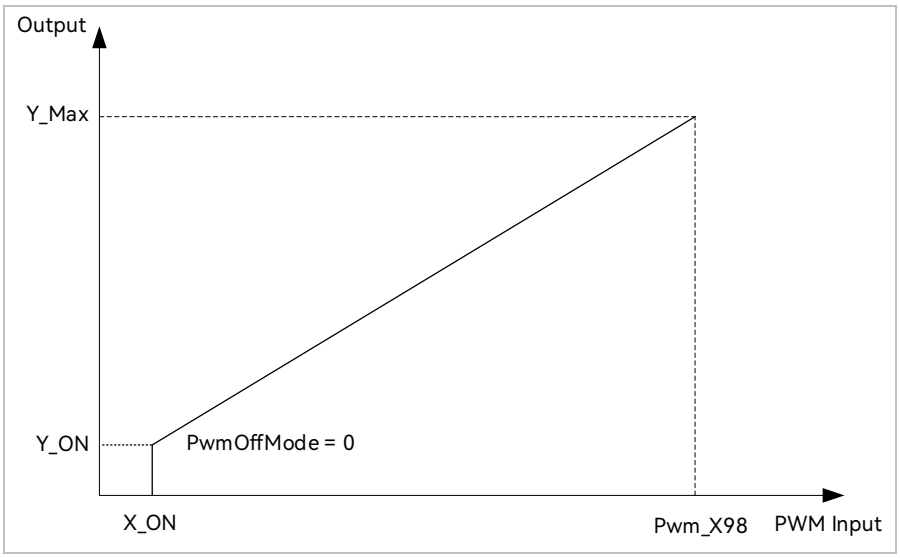
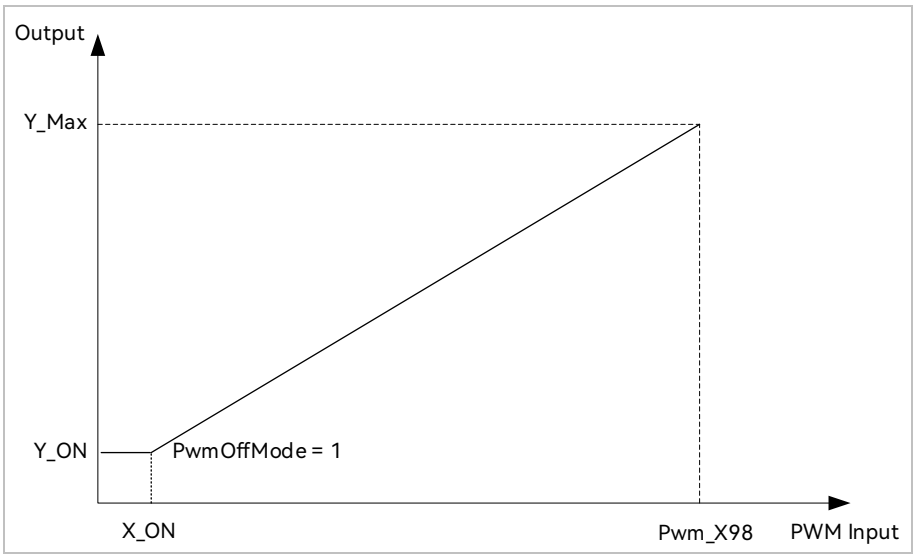


Figure 5-4 Output Curve in Speed-loop or Current-loop Control Mode (PwmOffMode = 1)



5.9 Sleep Mode

The motor enters sleep mode when the motor stays in stop state for 6 seconds.

Wakeup conditions: In I²C speed control mode, the chip exits sleep mode after receiving the matched I²C ID. In PWM or CLOCK speed control mode, if inverted input is disabled, the chip exits sleep mode when a high-level voltage is input to SPEED/SCL pin; and if inverted input is enabled, the chip exits sleep mode when a low-level voltage is input to SPEED/SCL pin. In analog voltage control mode, the chip exits sleep mode when the voltage of ASPEED pin is greater than 1.5V or when a high-level

voltage is input to SPEED/SCL pin.

5.10 Soft-on and Soft-off

Soft-on feature gradually increases the current during start-up process, and soft-off feature gradually decreases the current during shut-down process. The two features protect the motor from abrupt startup or shutdown and reduce noise during operation.

Figure 5-5 Soft-on Phase Current Waveform

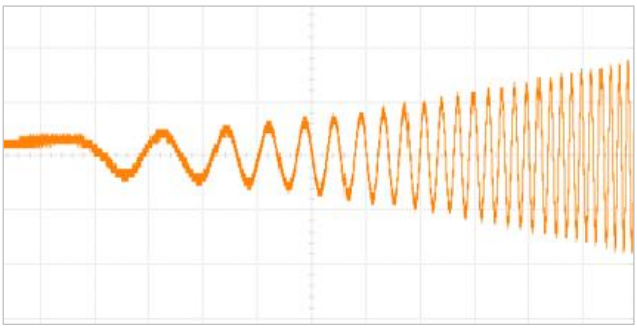
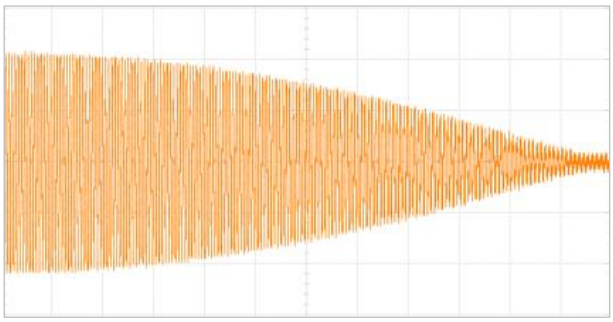


Figure 5-6 Soft-off Phase Current Wave



5.11 Motor Lock Protection

Motor lock protection circuitry monitors operating state of the motor. When the conditions for motor lock are satisfied, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.12 Phase Loss Protection

Phase loss protection circuitry monitors operating state of the motor. When the conditions for phase loss are satisfied, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.13 Over-current Protection (OCP)

When the sampling current exceeds the over-current protection threshold, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.14 Temperature Sensor Detect (TSD)

When the chip junction temperature is greater than 165℃, the chip automatically turns off the output until the chip junction temperature drops below 150℃ and then resumes the output.

5.15 Frequency Multiplication and Division of FG

Configuring FG/RD/SDA to FG outputs FG signal, that is, FG/RD/SDA pin is selected to output FG signal. The output frequency of FG signal is determined by FGDIV (frequency division coefficient) and FGMUL (frequency multiplication coefficient). FGMUL can be set as 1, 2, 3 and 4, while FGDIV as 1, 1/3, 1/4 and 1/5. k (coefficient of output frequency) = FGMUL*FGDIV.

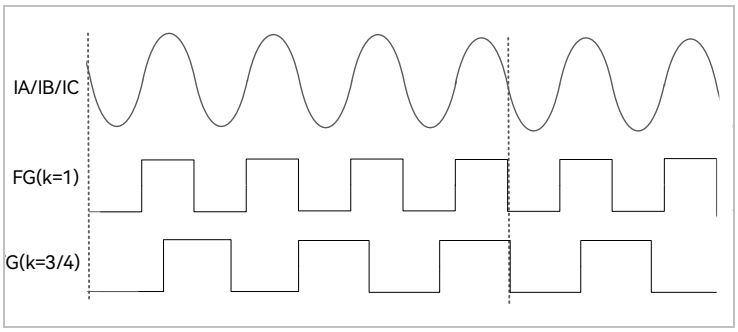
Table 5-1 FG Configurations

Coefficient of Output Frequency (k)		FGMUL			
		1	2	3	4
FGDIV	1	1	2	3	4
	1/3	1/3	2/3	3/3	4/3
	1/4	1/4	2/4	3/4	4/4
	1/5	1/5	2/5	3/5	4/5

The number of FG signals in one mechanical cycle is equal to pp*k (pp refers to pole-pair number of the motor). (pp refers to pole-pair number of the motor)

Example: For a 4-pole-pair motor, if FGMUL is set as 3 and FGDIV as 1/4, that is, k = 3/4, three FG signals are displayed in one mechanical cycle (4 * 3/4).

Figure 5-7 FG Output Waveforms When k = 1 and k= 3/4



5.16 CLOCK Speed Regulation Mode

In this mode, SPEED pin serves as the input of reference PWM frequency, and motor speed changes with reference PWM frequency. FGMUL and FGDIV are used to set the factor between motor speed and reference PWM frequency: Motor Speed = (reference PWM frequency*60/pp)/(FGMUL*FGDIV).

Example: For a 5-pole-pair motor, if FGDIV is set as 1/3 and FGMUL as 2 (i.e., k = 2/3), and the reference PWM frequency is 100Hz, then motor speed = (100Hz*60/5) / (2/3) = 1800rpm. In this case, the output frequency from FG pin is determined by FGDIV and FGMUL.

6 Revision History

Rev.	Description	Date	Prepared By
V1.0	First release	2021/01/11	Bruce Long
V1.1	1. Added Chapter 4 Electrical Characteristics; 2. Added Chapter 5 Function Descriptions.	2021/12/23	Bruce Long
V1.2	1. Added more information in Chapter 5; 2. Changed document format.	2021/12/28	Shawn Liang
V1.3	Standardized document format.	2022/04/19	Black Hu
V1.4	Minored content and format.	2022/06/09	Michelle Xie
V1.5	1. Corrected the model number from FT8132Q to FT8215Q in Table 1-1 FT8215Q QFN24 Pin List; 2. Corrected minimum value of PWM Input Frequency Range from 100 Hz to 20Hz in Table 4-5 PWM/CLOCK Input Frequency Range; 3. Added “If there are any differences between the Chinese and the English contents, please take the Chinese version as the standard.” in Copyright Notice; 4. Standardized document format.	2023/03/29	Eric Deng
V1.5Beta	1. Corrected maximum and minimum values of VCC Operating Voltage from 6V and 28V to 5V and 18V respectively in Table 4-2 FT8215Q Global Electrical Characteristics; 2. Added descriptions on SCL and SDA pins in Table 1-1 FT8215Q QFN24 Pins; 3. Modified waiting time for the chip to reset from 6s to 4s in sections 5.11 Motor Lock Protection, 5.12 Phase Loss Protection and 5.13 Over-current Protection; 4. Proofread the entire document and corrected wrong words.	2023/07/07	Eric Deng
V2.0	1. Added descriptions on FT8215D; 2. Updated product picture of FT8215Q; 3. Added “≥4.7μF” to the capacitor between VCC and the ground in Figure 1-1 Typical Application Diagram of FT8215Q (Single-shunt Current Sampling) and Figure 1-2 Typical Application Diagram of FT8215Q (Dual/Triple-shunt Current Sampling); 4. Modified “1μF” in the description on pin #21 (VCC) as “4.7μF” in section 1.6.2 FT8215Q Pins; 5. Updated section 2.1 FT8215Q QFN24_4x4; 6. Added the title “T_A = 25℃ and VCC = 12V unless	2024/12/19	Freya Fu

Rev.	Description	Date	Prepared By
	otherwise specified" to Table 4-1 Absolute Maximum Ratings ~ Table 4-7 ASPEED Electrical Characteristics; 7. Modified "Outout" as "Output" and "PWM Inout" as "PWM Input" in all figures in section 5.8.2 Speed Control Curve; 8. Modified "I2C" to "I^2C"; 9. Standardized document format.		
V2.1	1. Updated Figure 1-5 Functional Block Diagram of FT8215Q / FT8215D; 2. Updated Figure 2-2 FT8215D DFN16_3.3X3.3 Package Drawings and Dimensions; 3. Added Chapter 5.14 Temperature Sensor Detect (TSD); 4. Optimized Figure 1-3 Typical Application Diagram of FT8215D (Single-shunt Current Sampling), Figure 1-4 Typical Application Diagram of FT8215D (Dual/Triple-shunt Current Sampling) and Figure 1-7 FT8215D DFN16 Pinout Diagram; 5. Modified some descriptions.	2025/04/14	Eric Deng
V2.2	1. Modified the Min. of VCC Operating Voltage of FT8215Q and FT8215D as 4.5V; 2. Added "VCC > 5.5V" to VDD5 Operating Voltage of FT8215Q and FT8215D in 4.2 Global Electrical Characteristics; 3. Modified "4.4 IO Electrical Characteristics (DIR/SPEED/FR)" as "4.4 IO Electrical Characteristics (DIR/SPEED/ASPEED)"	2025/08/14	Freya Fu
V3.0	1. Added FT8215P; 2. Deleted FT8215D; 3. Modified "FG" pin as "FG/RD/SDA" and "SPEED" as "SPEED/SCL"; 4. Added SMP pin in section 1.5 Functional Block Diagram; 5. Modified Typ. of Rdson as "0.25Ω" in section 4.2 Global Electrical Characteristics; 6. Standardized document format.	2025/12/31	Freya Fu

Fortior Technology (Shenzhen) Co., Ltd

Room 203, 2/F, Building No.11, Keji Central Road 2,
Software Park, High-Tech Industrial Park, Shenzhen,
P.R. China

Tel.: 0755-26867710
Fax: 0755-26867715
P.C.: 518057
Web: http://www.fortiortech.com