Datasheet

Three-Phase BLDC Motor Controller with Built-in MOSFET FT8215QA

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Contents

FT8215QA Three-Phase BLDC Motor Controller with Built-in MOSFET

1 System Introduction

1.1 Overview

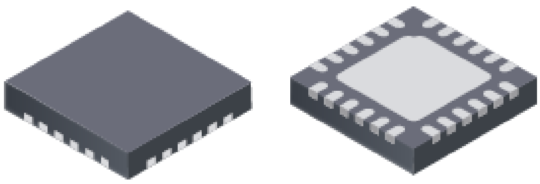
FT8215QA is an IC with built-in three-phase MOSFET designed for BLDC motor drive. Due to a high level of integration, few peripheral components are required. The chip controls the motor with low noise and small torque ripple. Motor parameters, startup control parameters and speed regulation mode can be configured via GUI, and are stored in built-in EEPROM. Analog voltage, PWM, I2C interface or CLOCK mode is optional for motor speed regulation. Moreover, the chip integrates speed indicator, which reads motor speed in real time via FG pin or I2C interface. Speed control mode, current control mode or voltage-loop control mode is optional. In addition, the chip supports over-current protection (OCP), under-voltage lockout (UVLO), over-temperature protection (OTP), motor lock protection (MLP) and phase-loss protection. The sleep current of chip is about 40μA.

1.2 Applications

Floor fans; Cooling fans.

1.3 Features

- Sensorless FOC mode
- Built-in MOSFET
- Speed control mode, current control mode or voltage control mode
- Analog voltage, PWM, I2C interface or CLOCK mode for motor speed regulation
- Real time information interactions by I2C for motor control and motor states readback
- Rotor initial position detection
- Tail wind and contrary wind detection
- Soft-On, Soft-Off
- Built-in EEPROM
- Configurable multi-segment output curve
- Protection against over-current, under-voltage, over-temperature, motor lock and phase loss
- Forward or reverse direction of rotation
- FG and RD output



FT8215QA QFN24

1.4 Typical Application Diagram

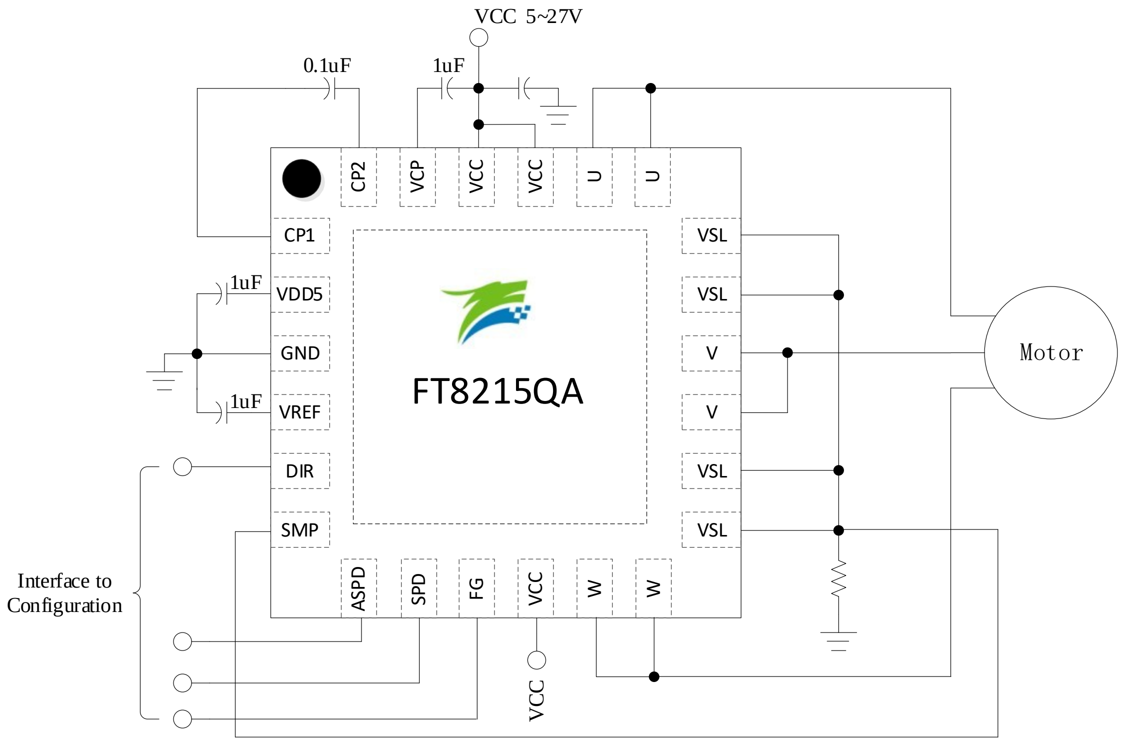


Figure 1-1 Typical Application Diagram of FT8215QA (Single-shunt Sampling)

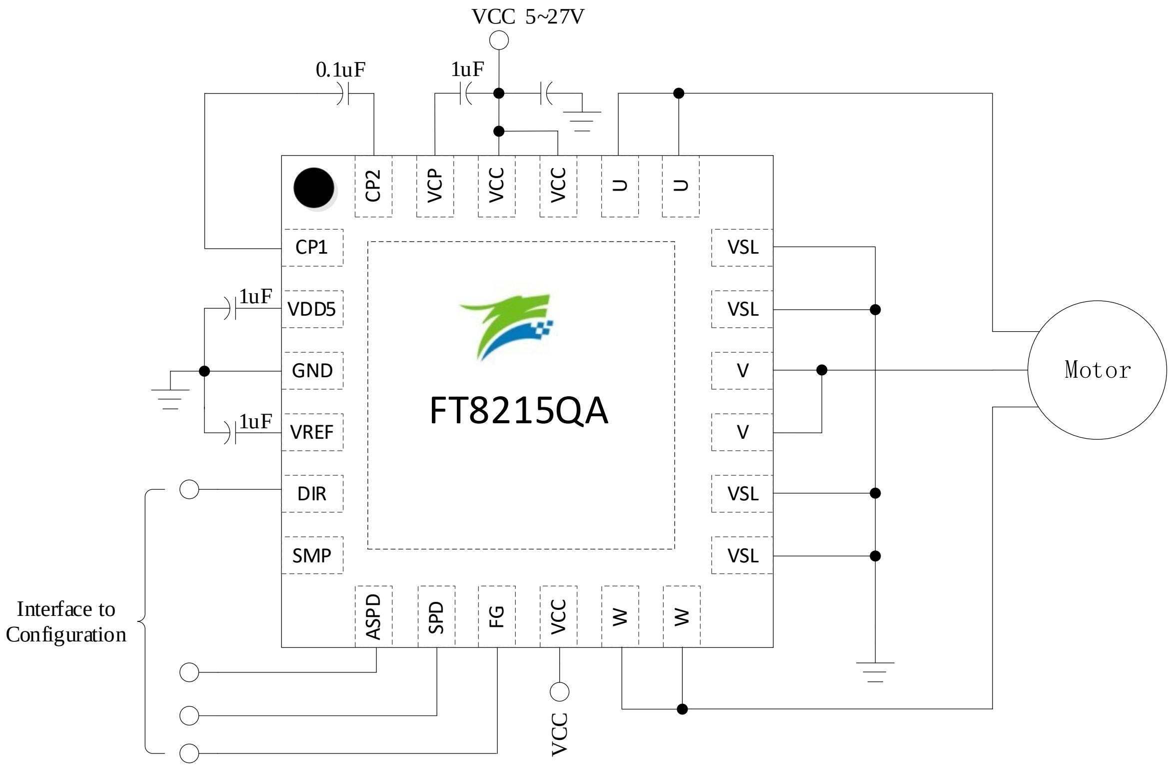


Figure 1-2 Typical Application Diagram of FT8215QA (Dual/Triple-shunt Sampling)

1.5 Functional Block Diagram

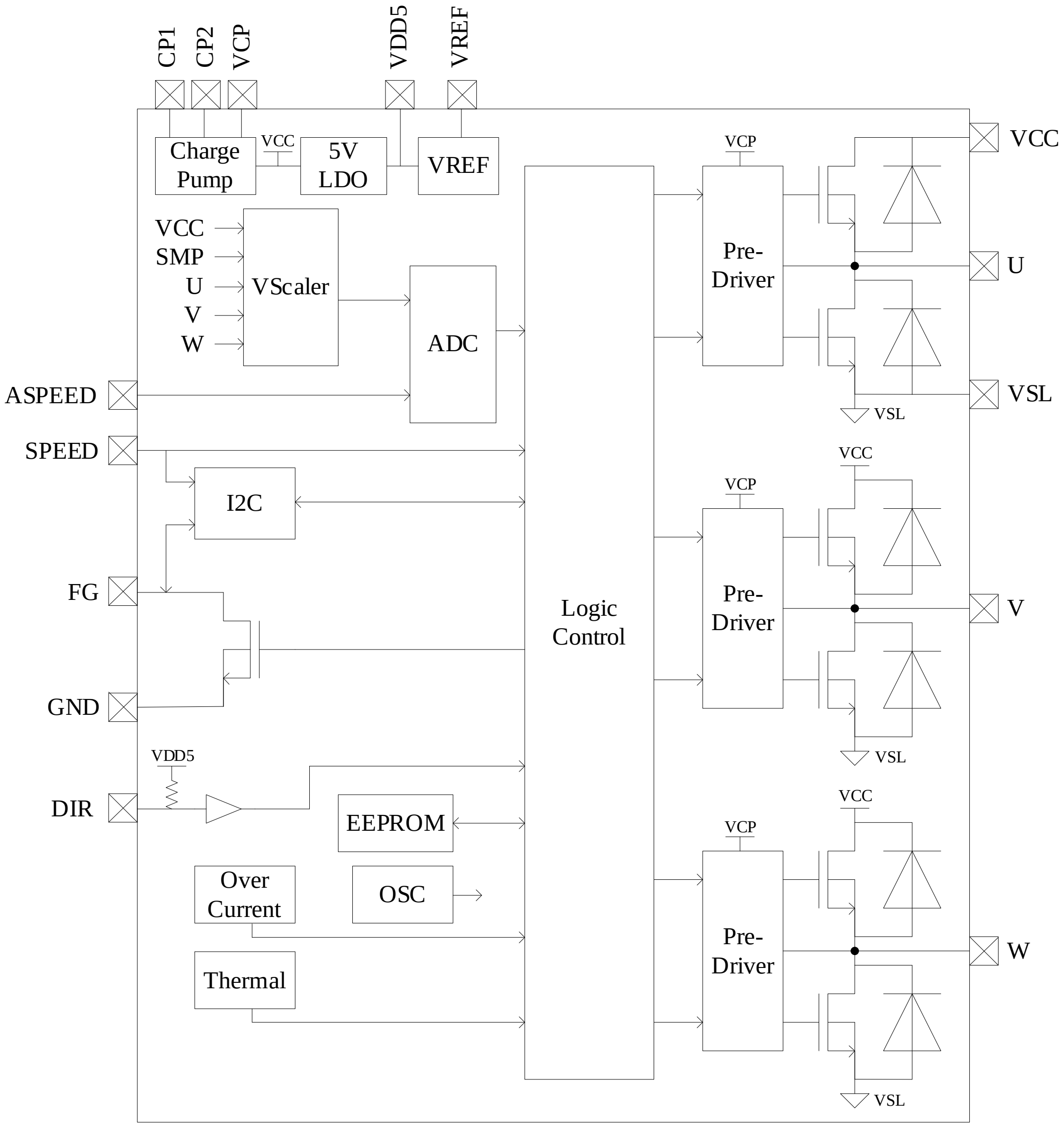


Figure 1-3 Functional Block Diagram of FT8215QA

1.6 Pin Diagram

1.6.1 FT8215QA QFN24 Pin Diagram

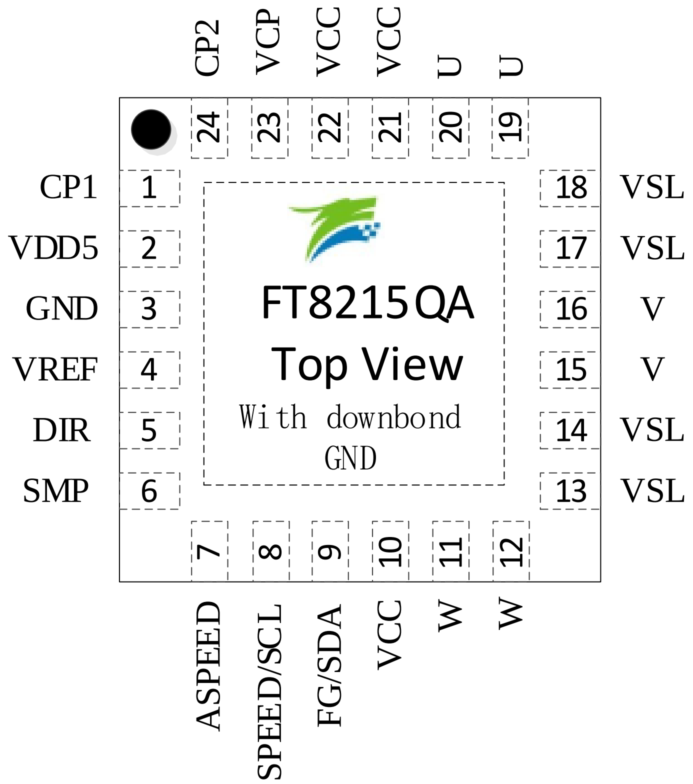


Figure 1-4 Pin Diagram of FT8215QA QFN24

1.7 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

1.7.1 FT8215QA QFN24 Pin List

Table 1-1 FT8215QA QFN24 Pin List

Pin	FT8215QA QFN24	IO Type	Description
CP1	1	AO	Charge pump pin, with a 0.1μF capacitor connected between CP2 and CP1
VDD5	2	P	5V LDO output, with a 1~4.7μF capacitor connected to ground
GND	3	P	Ground
VREF	4	AI	ADC voltage reference, with an external 1μF capacitor connected to ground
DIR	5	DI	Motor rotation control, with built-in pull-up resistor 1: Forward output phase sequence: U-->V-->W 0: Reverse output phase sequence: U-->W-->V
SMP	6	AI	Bus current sampling input
ASPEED	7	AI	Speed control with analog voltage input
SPEED/ SCL	8	DI	PWM or CLOCK mode input for speed control I2C SCL
FG/ SDA	9	DO	Speed or motor block indication output; Collector open-drain output I2C SDA
VCC	10	P	Power supply input
W	11	DO	W-phase output
W	12	DO	W-phase output
VSL	13	DO	Low-side source connection
VSL	14	DO	Low-side source connection
V	15	DO	V-phase output
V	16	DO	V-phase output
VSL	17	DO	Low-side source connection
VSL	18	DO	Low-side source connection
U	19	DO	U-phase output
U	20	DO	U-phase output
VCC	21	P	Power supply input, 5~27V, with a capacitor of 1μF or above connected to ground

Pin	FT8215QA QFN24	IO Type	Description
VCC	22	P	Power supply input
VCP	23	P	Charge-pump output, with a 1~4.7μF capacitor connected to VCC pin
CP2	24	AO	Charge-pump pin, with a 0.1μF capacitor connected between CP2 and CP1

2 Package Information

2.1 QFN24_4X4

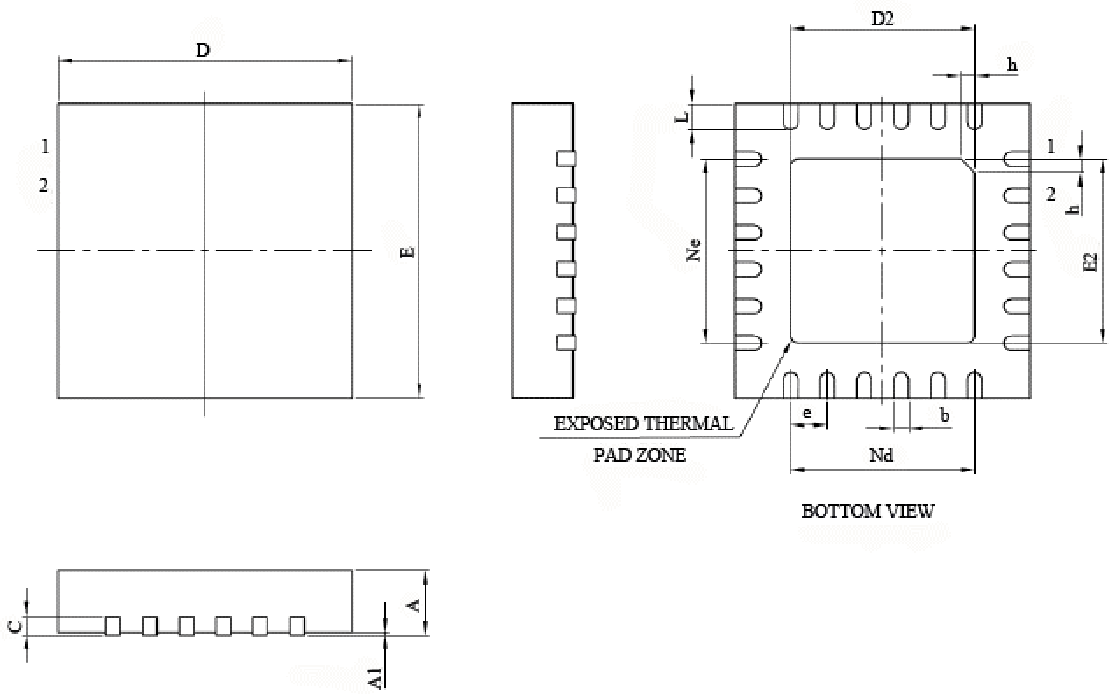


Figure 2-1 Package Diagram of QFN24_4X4

Table 2-1 Package Dimensions of QFN24_4X4

Symbol	Dimensions In Millimeter		
	Min	**Nom**	**Max**
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.35	2.50	2.65
L	0.35	0.40	0.45
h	0.30	0.35	0.40
N	Pin Number = 24		

3 Ordering Information

Table 3-1 Model Selections

Type	Package	Power Supply (V)	Rdson (High Side + Low Side)	Bus Current Average Value (A)	Control Functions						Protection					Operation Temperature T_j (°C)	Lead-free
					Driver Method	Speed Regulation Mode			Forward and Reverse Rotation	Initial Position Detection	Over-current Protection	Over-temperature Protection	Under-voltage Protection	Motor Lock Protection	Phase Loss Protection		
						I2C	PWM/CLOCK	Analog Input									
FT8215QA	QFN24 (4x4mm)	5~27	0.25	1.3	Sensorless Sine-wave	√	√	√	√	√	√	√	√	√	√	–40~150	√

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_j		–40	—	150	℃
Storage Temperature Tstg		–55	—	150	℃
VCC to VSS Voltage		–0.3	—	30	V
VDD5 to VSS Voltage		–0.3	5	6.5	V
FG, U, V, W and CP1 to VSS Voltage		–0.3	—	VCC + 0.3	V
VSL to VSS Voltage		–0.3	—	0.5	V
VCP and CP2 to VSS Voltage		–0.3	—	VCC + 6.0	V
VREF/DIR/SMP/ASPEED/SPEED to VSS Voltage		–0.3	—	VDD5 + 0.3	V

Note: Stress values greater than those listed in Table 4-1 Absolute Maximum Ratings may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

4.2 Global Electrical Characteristics

Table 4-2 Global Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage		5	—	27	V
VDD5 Operating Voltage	I = 0~10mA	4.8	5	5.2	V
VREF Voltage Reference		4.3	4.5	4.7	V
VCC Operating Current I_{VCC}	T_A = 25℃ (average)	—	—	1.3	A
	T_A = 85℃ (average)	—	—	0.8	A
VCC Sleep-Mode Current $I_{VCC\text{-}sleep}$		—	36	—	μA
Peak Current of Phase Current I_{PHASE}	Sine-wave Peak Current	—	—	2.8	A
Rdson (High Side + Low Side)		—	0.22	0.4	Ω

4.3 Protection Electrical Characteristics

Table 4-3 Protection Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC UVLO Threshold Voltage V_{UVLO}		3.2	3.5	3.8	V
VCC UVLO Hysteresis Voltage $V_{UVLO\text{-}HYS}$		—	0.5	—	V
Over-current Threshold I_{ocp}		2.3	2.8	3.3	A
Junction Temperature T_{TSD}		—	165	—	℃
Temperature Hysteresis T_{TSD_HYS}		—	15	20	℃

4.4 IO Electrical Characteristics (DIR/SPEED/FG)

Table 4-4 IO Electrical Characteristics (DIR/SPEED/FG)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Voltage V_{IH}		2.5	—	VDD5	V
Low-level Input Voltage V_{IL}		0	—	0.6	V
SPEED/DIR/ASPEED Pull-up Resistance	SPEED pin in PWM/CLOCK speed regulation mode	—	33	—	kΩ
SPEED Pull-down Resistance		—	21	—	kΩ

4.5 PWM/CLOCK Input Frequency Range

Table 4-5 PWM/CLOCK Input Frequency Range

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWM Input Frequency Range		20	—	100k	Hz
CLOCK Input Frequency Range		20	—	1400	Hz

4.6 ASPEED Electrical Characteristics

Table 4-6 ASPEED Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ASPEED Input Voltage Range		0	—	VREF	V

4.7 Thermal Characteristics

Table 4-7 QFN24 Thermal Characteristics

Parameter	Test Conditions	Value	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance [1]	JEDEC standard, 2S2P PCB	50	°C/W
θ_{JC} Junction-to-case Thermal Resistance [1]	JEDEC standard, 2S2P PCB	25	°C/W

Note:

[1] Test results may vary depending on the actual conditions

5 Function Description

5.1 VREF

VREF is applied to internal digital logic and analog circuits only, and cannot be used for external circuits. A capacitor of 1μF or above shall be added at VREF pin to stabilize the power supply.

5.2 DIR

Forward or reverse direction control (DIR) pin is used to reverse motor rotation by changing DIR level. Pull-ups make the pin state as "High" by default.

5.3 SMP

SMP pin is used as the input of bus current sampling in single-shunt current sampling mode.

5.4 ASPEED

Analog voltage for motor speed regulation (ASPEED) pin serves as the analog input of analog voltage speed regulation mode. In this mode, analog voltage is input to control motor speed.

5.5 SPEED

Speed control (SPEED) pin is used to input duty cycle (PWM mode) or frequency (CLOCK mode) for speed regulation depending on the settings. In addition, SPEED pin serves as the clock line (SCL) for I2C communication.

5.6 FG

Speed detection and fault indication (FG/RD) pin is an open-drain output. When this pin is set to FG, it outputs speed feedback signal to indicate rotation speed of the motor, and when it is set to RD, it outputs high-level signal to indicate the fault state. In addition, FG/RD pin serves as the data line (SDA) for I2C communication.

5.7 VSL

In single-shunt current sampling mode, this pin is connected to ground with the sampling resistor. In dual/triple-shunt current sampling mode, this pin is short to ground. VSL to VSS voltage cannot be over 0.5V.

5.8 Speed Regulation

5.8.1 Speed Regulation Mode

The chip supports four types of speed control input interface: PWM, analog voltage, I2C and CLOCK, and only one of them can be chosen at a time. If analog voltage is selected, voltage value input to ASPEED pin controls the speed; if PWM or CLOCK is selected, duty cycle of PWM or CLOCK signal input to SPEED pin controls the speed; and if I2C is selected, SPEED pin serves as the clock line (SCL) and FG/RD pin as the data line (SDA).

5.8.2 Speed Regulation Curve

The control waveform is presented as below, where x-coordinate refers to duty cycle of the PWM input pin

(In I2C control and analog control modes, the input is converted to the corresponding PWM duty cycle); and y-coordinate refers to the output duty cycle, which represents different physical quantities in different control modes.

The y-coordinate represents Duty in voltage-loop control mode. The multi-segment speed control curve is obtained by setting five output duty cycle reference points. The start point is determined by X_ON, and the maximum duty cycle PWM_X98 can be set as 98% or 100%. The three inflection points of speed regulation curve are fixed at 25%, 50% and 75%, and the corresponding output reference Y_ON, Y_25, Y_50, Y_75 and Y_MAX are configurable.

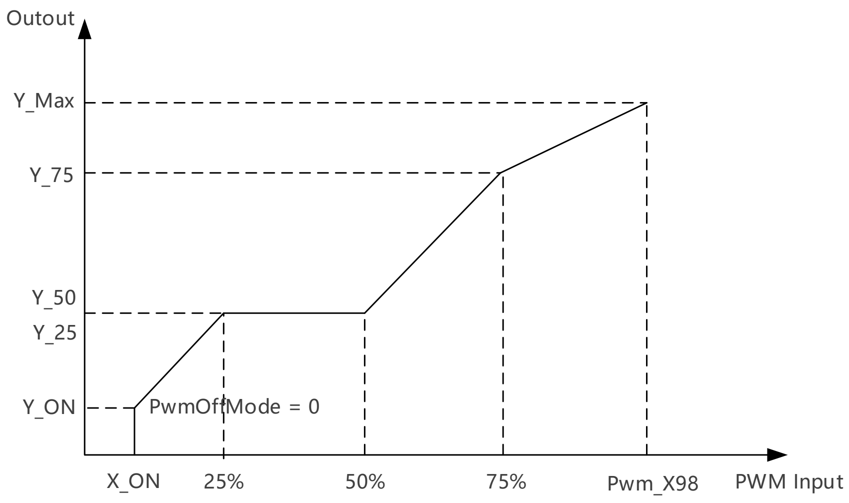


Figure 5-1 Multi Segment Output Curve in Voltage-loop Control Mode (PwmOffMode = 0)

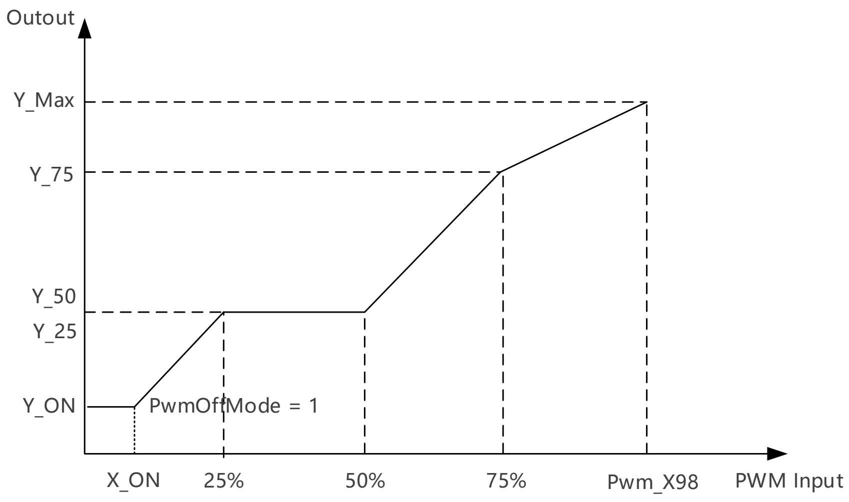


Figure 5-2 Multi Segment Output Curve in Voltage-loop Control Mode (PwmOffMode = 1)

When speed control/current control mode is selected, y-coordinate represents motor speed/current. In this case, only Y_ON and Y_MAX are configurable, and the output of other points between them increases linearly as the input varies.

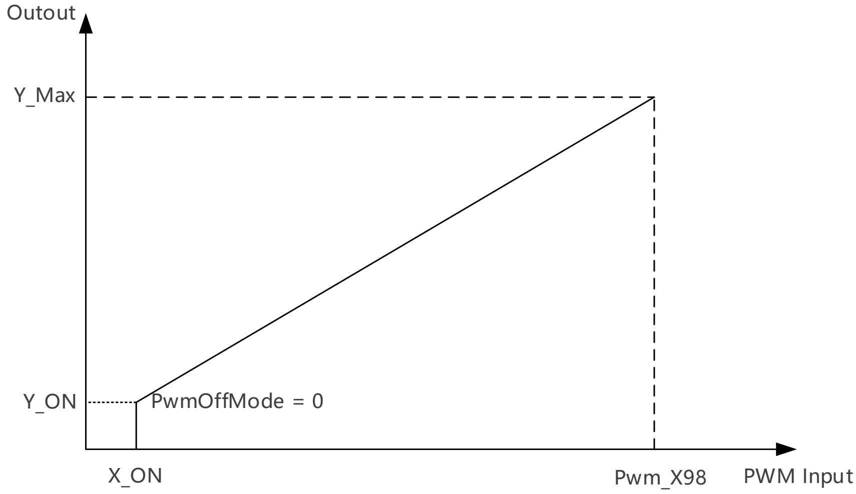


Figure 5-3 Output Curve in Speed/Current-loop Control Mode (PwmOffMode = 0)

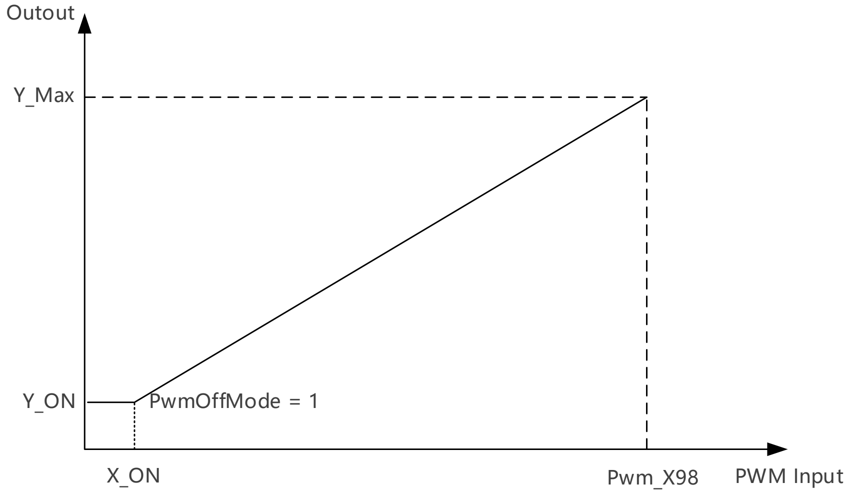


Figure 5-4 Output Curve in Speed/Current-loop Control Mode (PwmOffMode = 1)

5.9 Sleep Mode

The chip enters Sleep mode when the motor stays in stop state for 6 seconds.

Wakeup conditions: In I2C speed control mode, the chip exits sleep mode after receiving the matching I2C ID. In PWM or CLOCK speed control mode, if inverted input is disabled, the chip exits sleep mode when a high-level voltage is input to SPEED pin; and if inverted input is enabled, the chip exits sleep mode when a low-level voltage is input to SPEED pin. In analog voltage control mode, the chip exits sleep mode when the voltage of ASPEED pin is greater than 1.5V or when a high-level voltage is input to SPEED pin.

5.10 Soft-On and Soft-Off

Soft-On feature gradually increases the current during start-up process, and Soft-Off feature gradually decreases the current during shut-down process. The two features protect the motor from abrupt startup or shutdown and reduce noise during operation.

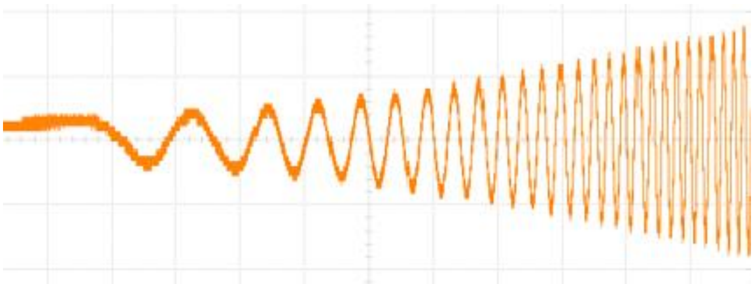


Figure 5-5 Soft-On Phase Current Wave

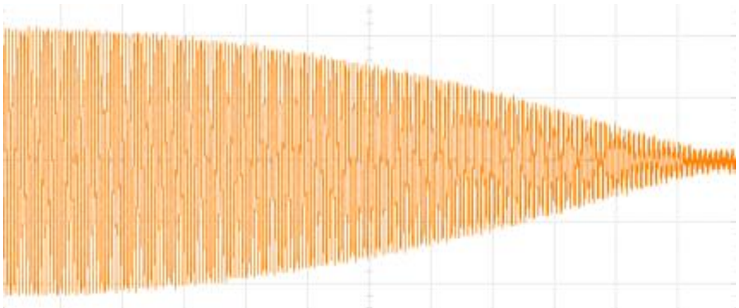


Figure 5-6 Soft-Off Phase Current Wave

5.11 Motor Lock Protection

Motor lock protection circuitry monitors operating state of the motor. When the conditions for motor lock are satisfied, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.12 Phase Loss Protection

Phase loss protection circuitry monitors operating state of the motor. When the conditions for phase loss are satisfied, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.13 Overcurrent Protection

When the sampling current exceeds the over-current protection threshold, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.14 Frequency Multiplication and Division of FG

Configuring FG/RD pin to FG outputs FG signal. The output frequency of FG signal is determined by FGDIV (frequency division coefficient) and FGMUL (frequency multiplication coefficient). FGMUL can be set as 1, 2， 3 and 4, while FGDIV as 1, 1/3, 1/4 and 1/5. k (coefficient of output frequency) = FGMUL*FGDIV.

Table 5-1 FG Configurations

Coefficient of Output Frequency (k)		FGMUL			
		1	2	3	4
FGDIV	1	1	2	3	4
	1/3	1/3	2/3	3/3	4/3
	1/4	1/4	2/4	3/4	4/4
	1/5	1/5	2/5	3/5	4/5

The number of FG signals in one mechanical cycle is equal to pp*k (pp refers to pole-pair number of the motor).

Example: For a 4-pole-pair motor, if FGMUL is set as 3 and FGDIV as 1/4, that is, k = 3/4, three FG signals are displayed in one mechanical cycle (4 * 3/4).

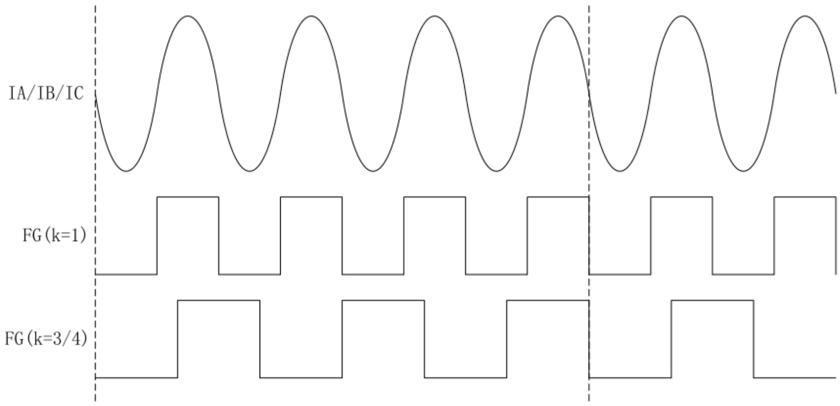


Figure 5-7 FG Output Waveforms when k = 1 and k = 3/4

5.15 CLOCK Speed Regulation Mode

In this mode, SPEED pin serves as the input of reference PWM frequency, and motor speed changes with reference PWM frequency. FGMUL and FGDIV are used to set the factor between motor speed and reference PWM frequency: Motor Speed = (reference PWM frequency*60/pp)/(FGMUL*FGDIV).

Example: For a 5-pole-pair motor, if FGDIV is set as 1/3 and FGMUL as 2 (i.e., k = 2/3), and the reference PWM frequency is 100Hz, then motor speed = (100Hz*60/5) / (2/3) = 1800rpm. In this case, the output frequency of FG signal is determined by FGDIV and FGMUL.

6 Revision History

Rev.	Descriptions	Date	Prepared By
V1.0	Initial version	2021/01/11	Bruce Long
V1.1	1. Added Chapter 4 Electrical Characteristics. 2. Added Chapter 5 Function Description.	2021/12/23	Bruce Long
V1.2	1. Added more information in Chapter 5. 2. Changed document format.	2021/12/28	Shawn Liang
V1.3	Standardized document format.	2022/04/19	Black Hu
V1.4	Minor content and format change.	2022/06/09	Michelle Xie
V1.5	1. Corrected the model number from FT8132Q to FT8215QA in Table 1-6-1 FT8215QA QFN24 Pin List. 2. Corrected minimum value of PWM Input Frequency Range from 100 Hz to 20Hz in Table 4-5 PWM/CLOCK Input Frequency Range. 3. Added "If there are any differences between the Chinese and the English contents, please take the Chinese version as the standard." in Copyright Notice. 4. Standardized document format.	2023/03/29	Eric Deng
V1.5Beta	1. Updated VCC 5~18V in 1.4 Typical Application Diagram to VCC 5~22V; 2. Updated power supply input of VCC in 1.7.1 FT8215QA QFN24 Pin List from "5~18V" to "5~22V"; 3. Updated power supply in 3 Ordering Information from "5~18V" to "5~22V"; 4. Updated maximum value of VCC to VSS Voltage in Table 4-1 Absolute Maximum Ratings from 22V to 30V; 5. Updated maximum value of VCC Operating Voltage in Table 4-2 Global Electrical Characteristics from 18V to 22V; 6. Proofread descriptions in section 1 System Introduction and section 5 Function Description; 7. Modify the driving current (average value) from 2A to 1A; 8. The working current of VCC is Ivcc, and the average value of T_A =25 ° C is modified from 2A to 1A, and the average value of T_A =85 ° C is modified from 1.8A to 0.8A; 9. Standardized document format.	2023/05/30	Kelly Li
V1.6Beta	1. Updated VCC 5~22V in 1.4 Typical Application Diagram to VCC 5~27V; 2. Updated power supply input of VCC in 1.7.1 FT8215QA QFN24 Pin List from "5~22V" to "5~27V"; 3. Updated power supply in 3 Ordering Information from	2023/12/12	Kelly Li

	"5~22V" to "5~27V; 4. The maximum value of "VCC working voltage" in Table 4.2 of the global electrical characteristics has been changed from 22V to 27V, and the maximum Peak Current of Phase Current I_{PHASE} has been changed from 3.0A to 2.8A; 5. The maximum and minimum current values for Over-current Threshold Iocp in table 4-3 have been changed from 3.5~4.5A to 2.3~3.3A, and the typical value has been changed from 4.0A to 2.8A.		
V1.7Beta	1. Updated maximum value of VCC Operating Current I_{VCC} in Table 4-2 Global Electrical Characteristics from 1A to 1.3A.	2024/05/07	Elena Sun
V1.8Beta	1. Deleted "Bus current: 1A (average value)" in section 1.3 Features; 2. Modified Bus Current Average Value "1A" in section 3 Ordering Information as "1.3A".	2025/05/22	Elena Sun

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