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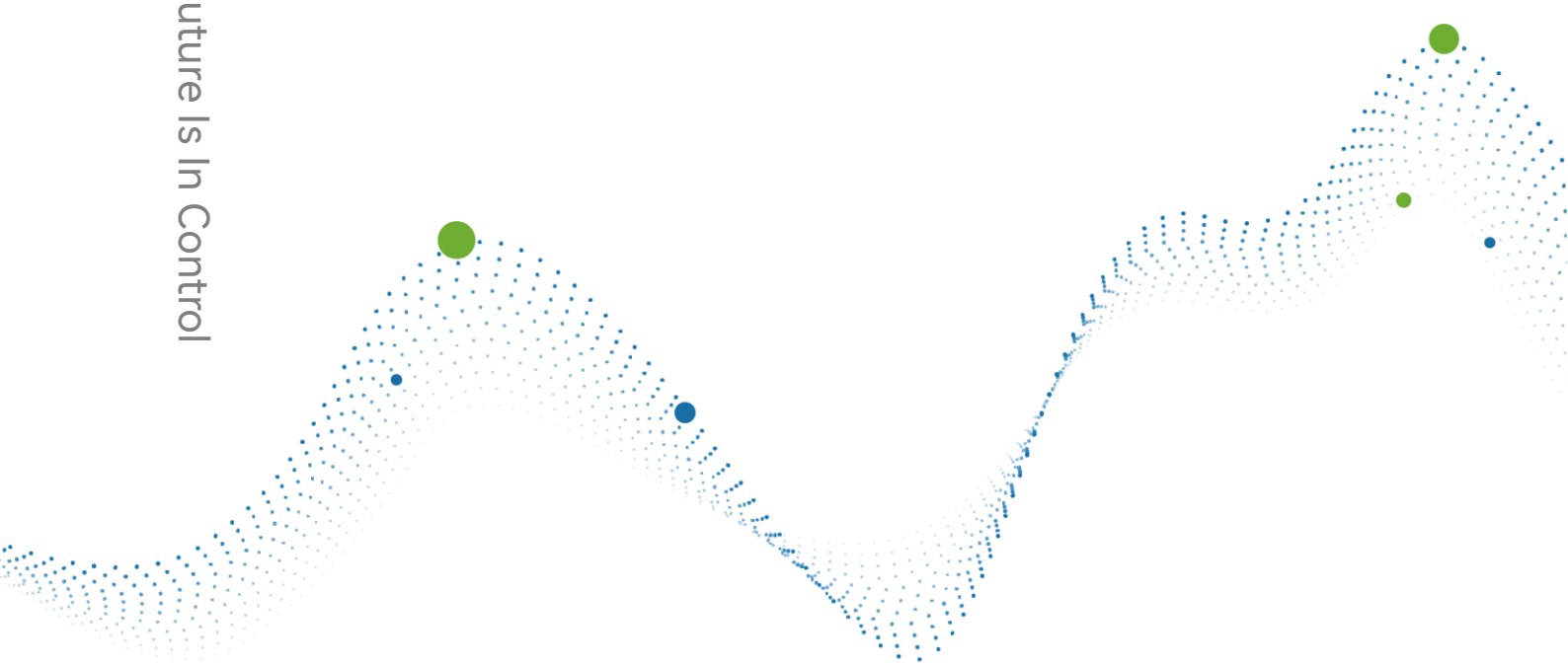
DATASHEET

FT3207

Three-phase Fully Integrated BLDC Motor Controller

Future Is In Control



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Contents

1 System Introduction

1.1 Overview

FT3207 is a fully integrated IC with built-in MOSFET designed for three-phase BLDC motor control applications. It supports sensorless sine-ware drive to reduce audible noise. External resistor and capacitor can be used to set its startup mode, forced commutation time, FG generation, forward or reverse rotation and external PWM input frequency. FT3207 also supports short circuit protection, over-voltage protection (OVP), over-current protection (OCP), motor lock protection (MLP) and temperature sensor detect (TSD), and offers a low-power mode with the sleep-mode current about 60μA, making it especially suitable for those applications that require low power consumption and low noise, such as notebook cooling fans.

For ease of description and distinction, any subsequent mention of specific model numbers indicates that the feature is exclusive to that model. Otherwise, the feature is common to the FT3207 series of chips.

FT3207 series chips includes FT3207N (DFN10), FT3207NAA (DFN10), and FT3207P (PLQFN10).

1.2 Applications

FT3207N Notebook cooling fans

FT3207NA: Notebook cooling fans

FT3207P: Notebook cooling fans and micro fans

1.3 Features

- VCC voltage range: 2V ~ 6V
- FT3207N/FT3207NA drive current: 0.8A@85℃
- FT3207P drive current: 0.7A@85℃
- Sensorless control
- Five-segment sine wave drive
- Seven-segment sine wave drive (FT3207N / FT3207P)
- Full duty-cycle startup/soft startup
- Low power consumption
- Tailwind and headwind detection
- Configurable commutation frequency for startup
- Auto-tuning lead angle
- External PWM input for speed regulation
- FG, 1/2 FG, 1/3 FG, 2/3 FG or RD output
- Support protection features, including short circuit protection, OVP, OCP, MLP, TSD, etc.

1.4 Package

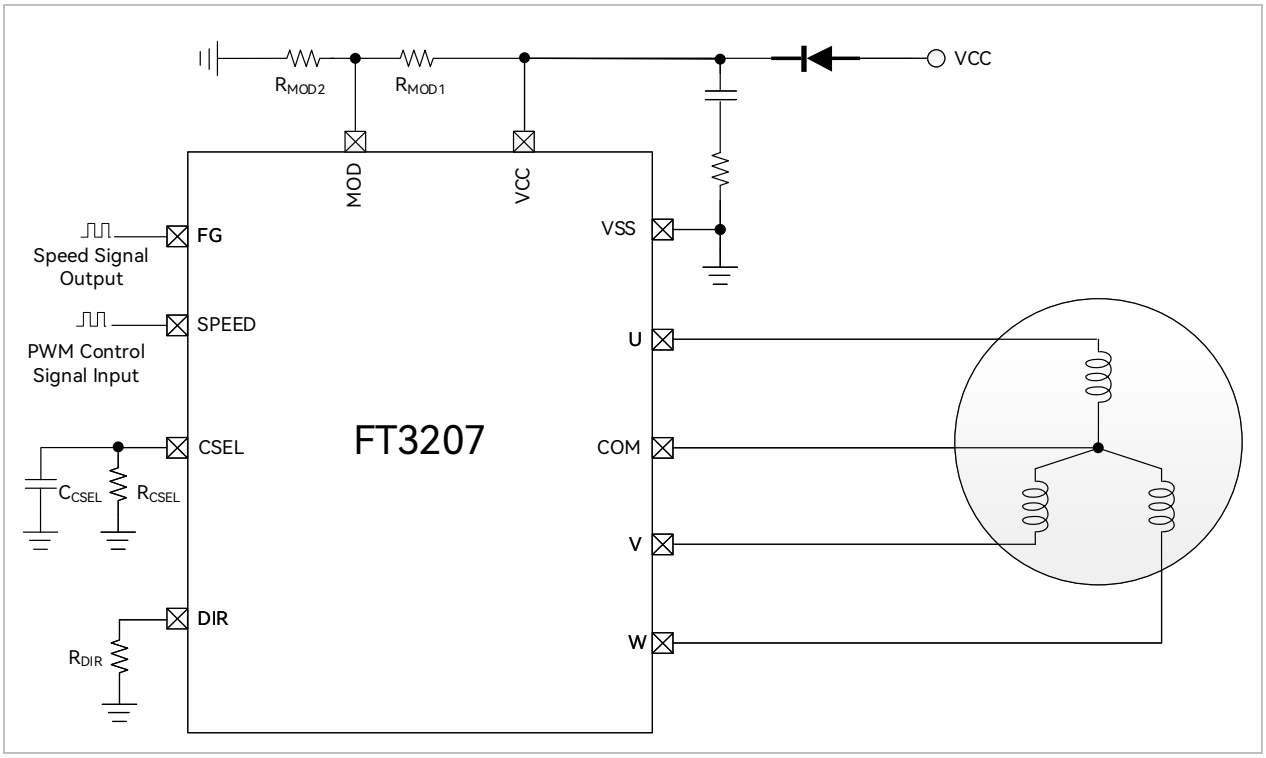
FT3207N

FT3207NA

FT3207P

1.5 Typical Application Diagram

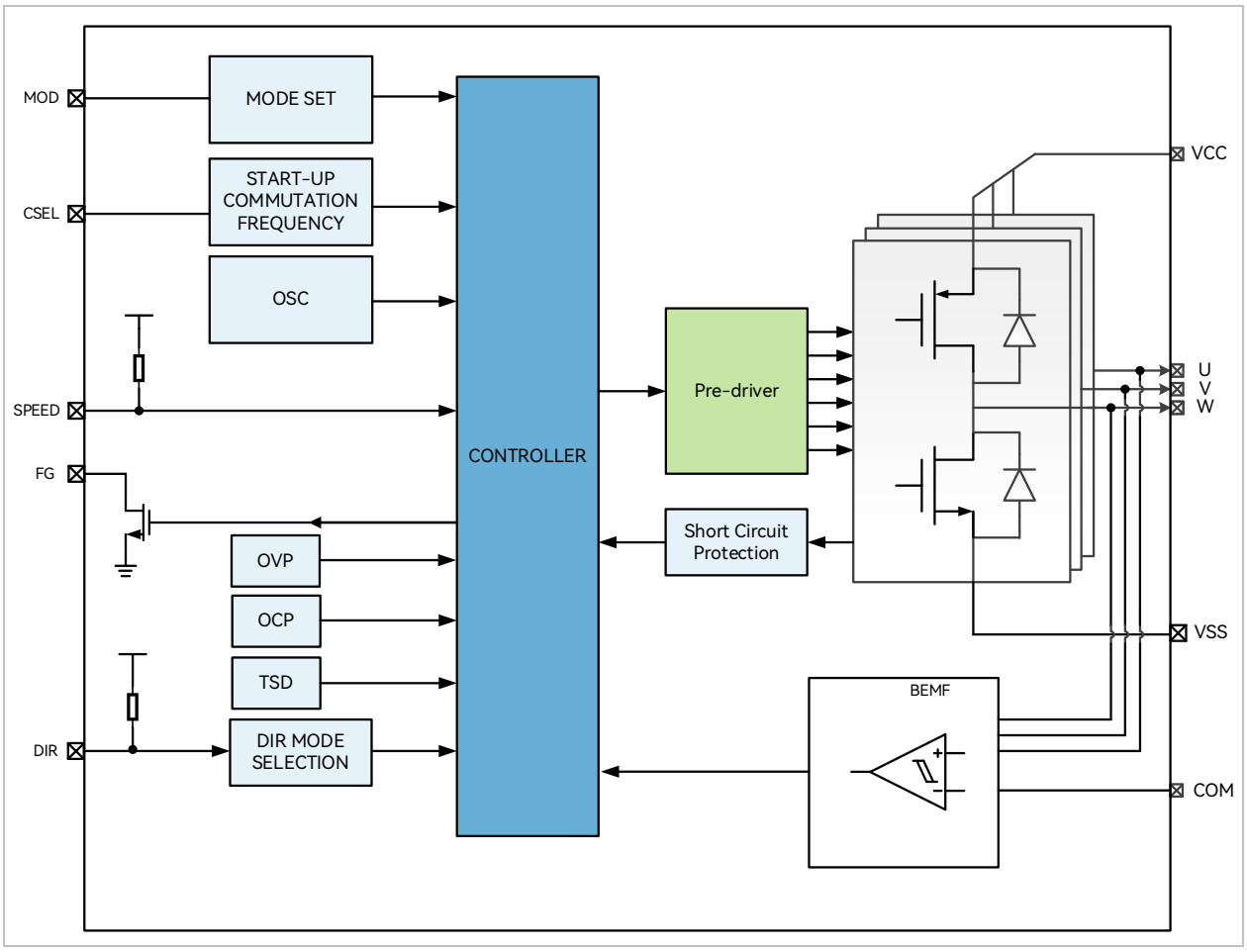
Figure 1-1 Typical Application Diagram of Sensorless Control



1.6 Functional Block Diagram

1.6.1 FT3207

Figure 1-2 Functional Block Diagram of FT3207



1.7 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- DB = Digital Bidirectional
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

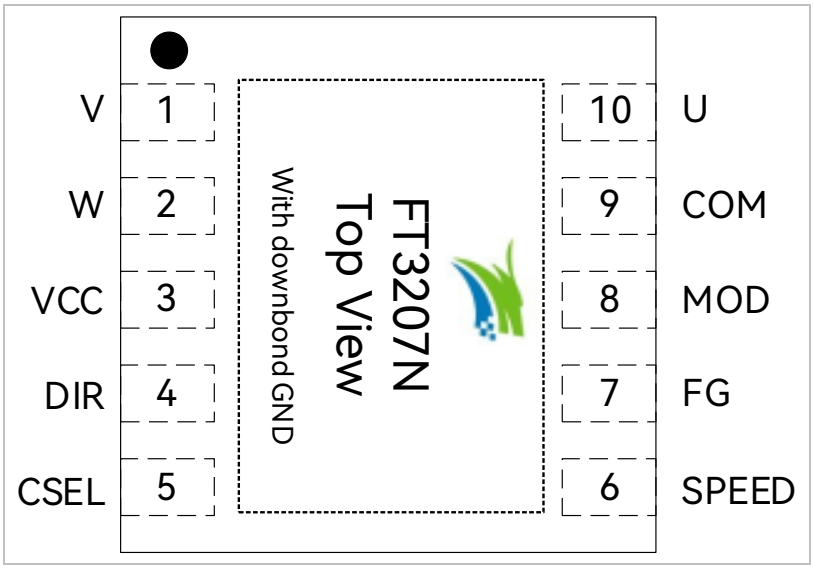
1.7.1 FT3207N DFN10 Pins

Table 1-1 FT3207N DFN10 Pin Descriptions

Pin	FT3207N DFN10	IO Type	Description
V	1	DO	V-phase output
W	2	DO	W-phase output
VCC	3	P	Input power supply
DIR	4	AI	Motor operation mode selection. See Mapping between R_{DIR} and Motor Functions.
CSEL	5	AI	Forced commutation time selection. See Mapping between R_{CSEL}/C_{CSEL} and Forced Commutation Time/Lead Angle Mode.
SPEED	6	DI	PWM input for speed regulation PWM input range: 20Hz ~ 62.5kHz or 0.3kHz ~ 62.5kHz, which is determined by MOD pin configuration.
FG	7	DO	Speed signal output
MOD	8	AI	MOD mode selection. See Mapping between R_{MOD1}/R_{MOD2} and Function Parameters.
COM	9	AI	Motor neutral point input
U	10	DO	U-phase output
Bottom Pad	-	P	Ground

1.7.2 FT3207N DFN10 Pinout Diagram

Figure 1-3 FT3207N DFN10 Pinout Diagram



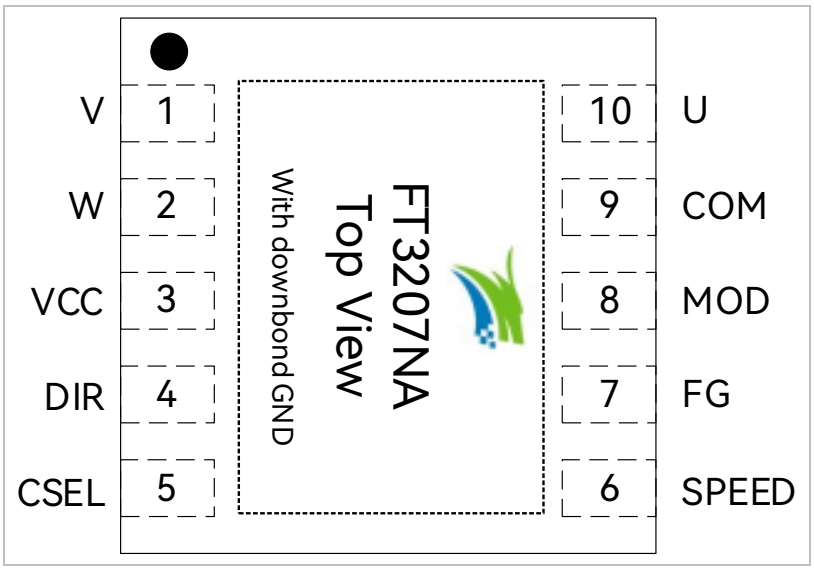
1.7.3 FT3207NA DFN10 Pins

Table 1-2 FT3207NA DFN10 Pin Descriptions

Pin	FT3207NA DFN10	IO Type	Description
V	1	DO	V-phase output
W	2	DO	W-phase output
VCC	3	P	Input power supply
DIR	4	AI	Motor operation mode selection. See Mapping between R_{DIR} and Motor Functions.
CSEL	5	AI	Forced commutation time selection. See Mapping between R_{CSEL}/C_{CSEL} and Forced Commutation Time/Lead Angle Mode.
SPEED	6	DI	PWM input for speed regulation PWM input range: 20Hz ~ 62.5kHz or 0.3kHz ~ 62.5kHz, which is determined by MOD pin configuration.
FG	7	DO	Speed signal output
MOD	8	AI	MOD mode selection. See Mapping between R_{MOD1}/R_{MOD2} and Function Parameters.
COM	9	AI	Motor neutral point input
U	10	DO	U-phase output
Bottom Pad	-	P	Ground

1.7.4 FT3207NA DFN10 Pinout Diagram

Figure 1-4 FT3207NA DFN10 Pinout Diagram



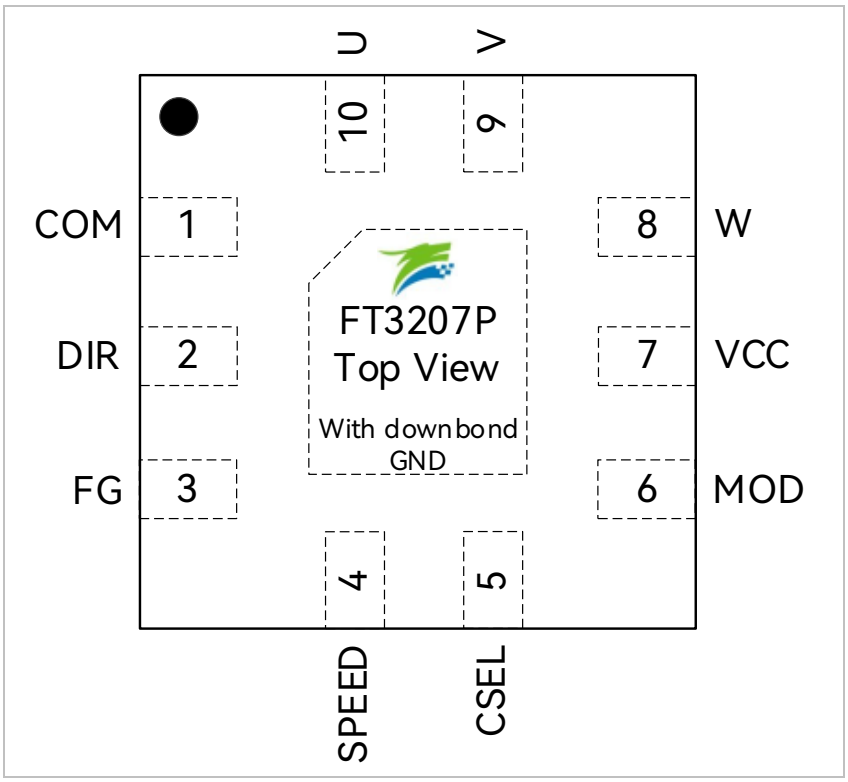
1.7.5 FT3207P PLQFN10 Pins

Table 1-3 FT3207P PLQFN10 Pinout Diagram

Pin	FT3207P PLQFN10	IO Type	Description
COM	1	AI	Motor neutral point input
DIR	2	AI	Motor operation mode selection. See Mapping between R_{DIR} and Motor Functions.
FG	3	DO	Speed signal output
SPEED	4	DI	PWM input for speed regulation PWM input range: 20Hz ~ 62.5kHz or 0.3kHz ~ 62.5kHz, which is determined by MOD pin configuration.
CSEL	5	AI	Forced commutation time selection. See Mapping between R_{CSEL}/C_{CSEL} and Forced Commutation Time/Lead Angle Mode.
MOD	6	AI	MOD mode selection. See Mapping between R_{MOD1}/R_{MOD2} and Function Parameters.
VCC	7	P	Input power supply
W	8	DO	W-phase output
V	9	DO	V-phase output
U	10	DO	U-phase output
Bottum Pad	-	P	Ground

1.7.6 FT3207P PLQFN10 Pinout Diagram

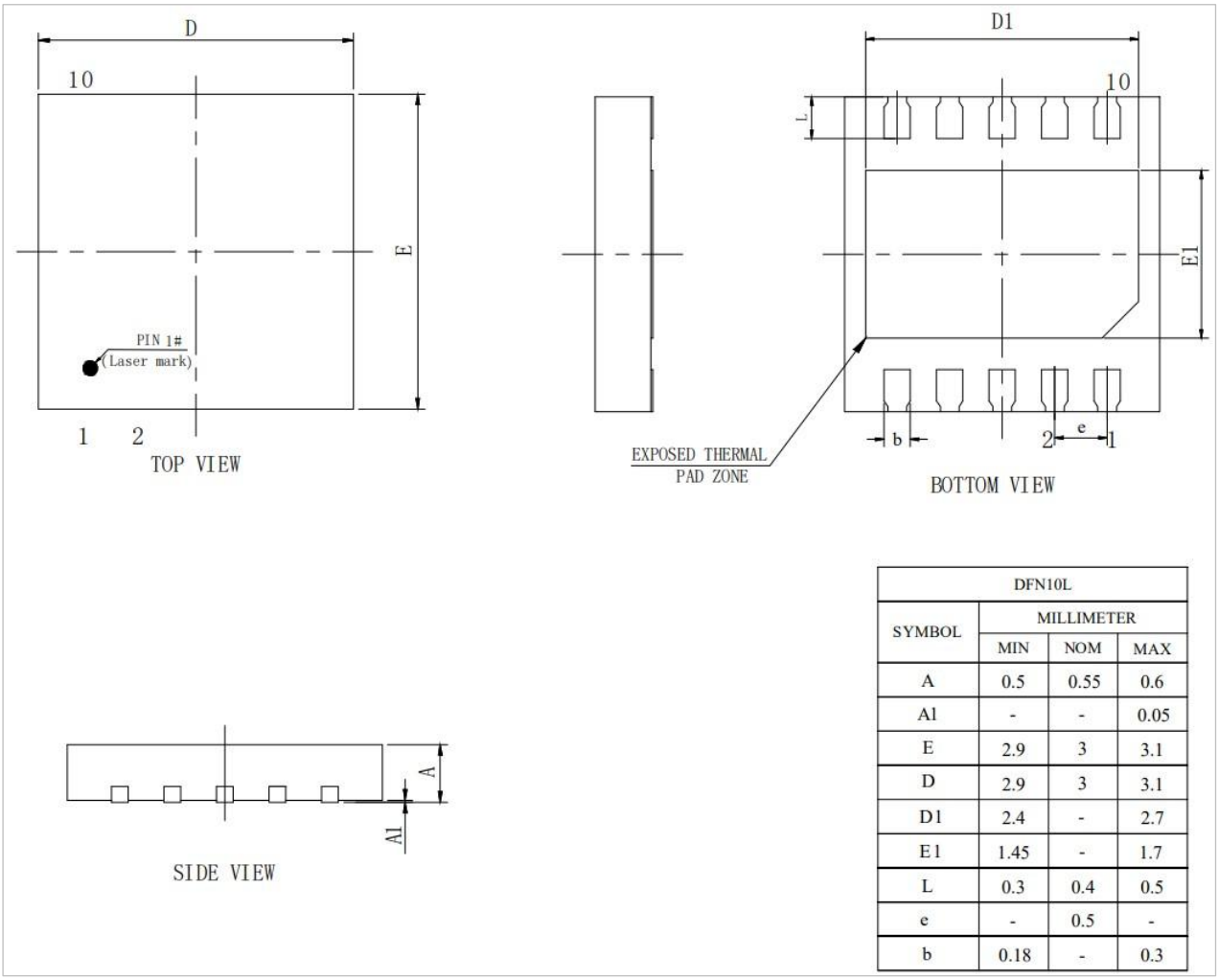
Figure 1-5 FT3207P PLQFN10 Pinout Diagram



2 Package Information

2.1 DFN10_3X3 (FT3207N / FT3207NA)

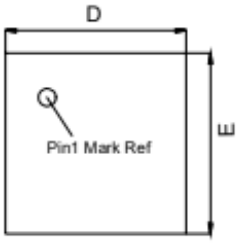
Figure 2-1 FT3207N / FT3207NA DFN10_3x3 Package Drawings and Dimensions



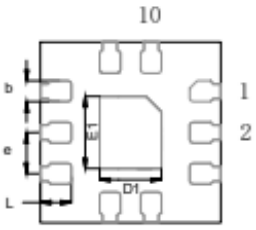
DFN10L			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.5	0.55	0.6
A1	-	-	0.05
E	2.9	3	3.1
D	2.9	3	3.1
D1	2.4	-	2.7
E1	1.45	-	1.7
L	0.3	0.4	0.5
e	-	0.5	-
b	0.18	-	0.3

2.2 PLQFN10_1.75x1.75 (FT3207P)

Figure 2-2 FT3207P PLQFN10_1.75x1.75 Package Drawings and Dimensions



TOP VIEW



BOTTOM VIEW

SIDE VIEW

PLQFN1.75*1.75-10L			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.340	0.370	0.400
Al	0.007	0.012	0.017
D	1.650	1.750	1.850
E	1.650	1.750	1.850
Dl	0.550	0.600	0.650
El	0.650	0.700	0.750
L	0.250	0.300	0.350
e	—	0.400	—
b	0.150	0.200	0.250

3 Ordering Information

Table 3-1 Model Selections

Model	Power Supply (V)	Rdson (High Side + Low Side) (Ω)	Average Drive Current (A)	Drive Type	Control Features									Protection Features					Operating Temperature T_J (°C)	Lead-free	Package
					Speed Regulation			SVPWM			Forward and Reverse Rotation	Soft Startup	Tailwind and Headwind Detection	Short Circuit Protection	OVP	OCP	TSD	MLP			
					I^2C	PWM	Analog Voltage	Carrier Frequency (kHz)	Five-segment	Seven-segment											
FT3207N	2 ~ 6	0.7	0.8	Sensorless Sine-wave	-	√	-				√	√	√	√	√	√	√	√	-40 ~ 150	√	DFN10 3X3mm
FT3207NA	2 ~ 6	0.7	0.8	Sensorless Sine-wave	-	√	-	93.75	√	-	√	√	√	√	√	√	√	√	-40 ~ 150	√	DFN10 3x3mm

Model	Power Supply (V)	Rdson (High Side + Low Side) (Ω)	Average Drive Current (A)	Drive Type	Control Features									Protection Features					Operating Temperature T_J (°C)	Lead-free	Package
					Speed Regulation			SVPWM			Forward and Reverse Rotation	Soft Startup	Tailwind and Headwind Detection	Short Circuit Protection	OVP	OCP	TSD	MLP			
					I^2C	PWM	Analog Voltage	Carrier Frequency (kHz)	Five-segment	Seven-segment											
FT3207P	2 ~ 6	0.7	0.7	Sensorless Sine-wave	-	√	-	93.75	√	√	√	√	√	√	√	√	√	√	-40 ~ 150	√	PLQFN10 1.75x1.75 mm

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Exceeding the stress value specified in Table 4-1 to Table 4-7 may permanently damage the device. These are stress ratings only; operation outside the specified conditions is not recommended. Extended operation under absolute maximum rated conditions may affect device reliability.

4.1.1 FT3207N

Table 4-1 Absolute Maximum Ratings of FT3207N

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature T_{STG}		-55	-	150	℃
Power Dissipation P_d		-	1.05	-	W
VCC to VSS Voltage		-0.3	-	7	V
Other IOs to VSS Voltage Except VCC		-0.3	-	VCC	V

4.1.2 FT3207NA

Table 4-2 Absolute Maximum Ratings of FT3207NA

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature T_{STG}		-55	-	150	℃
Power Dissipation P_d		-	1.05	-	W
VCC to VSS Voltage		-0.3	-	7	V
Other IOs to VSS Voltage Except VCC		-0.3	-	VCC	V

4.1.3 FT3207P

Table 4-3 Absolute Maximum Ratings of FT3207P

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature T_{STG}		-55	-	150	℃
Power Dissipation P_d		-	0.81	-	W
VCC to VSS Voltage		-0.3	-	7	V
Other IOs to VSS Voltage Except VCC		-0.3	-	VCC	V

4.2 Global Electrical Characteristics

4.2.1 FT3207N

Table 4-4 Global Electrical Characteristics of FT3207N

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1]		2	-	6	V
VCC Output Current I_{out}	T_A = 85℃ (Average)	-	-	0.8	A
VCC Operating Current $I_{VCC-work}$		-	3	5	mA
VCC Sleep-mode Current $I_{VCC-sleep}$		-	60	100	μA
Rdson (High-side MOS + Low-side MOS)	Sink Current = 1A Operating Junction Temperature T_J < 150℃	-	0.7	1	Ω

4.2.2 FT3207NA

Table 4-5 Global Electrical Characteristics of FT3207NA

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1]		2	-	6	V
VCC Output Current I_{out}	T_A = 85℃ (Average)	-	-	0.8	A
VCC Operating Current $I_{VCC-work}$		-	3	5	mA
VCC Sleep-mode Current $I_{VCC-sleep}$		-	60	100	μA
Rdson (High-side MOS + Low-side MOS)	Sink Current = 1A Operating Junction Temperature T_J < 150℃	-	0.7	1	Ω

4.2.3 FT3207P

Table 4-6 Global Electrical Characteristics of FT3207P

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1]		2	-	6	V
VCC Output Current I_{out}	T_A = 85℃ (Average)	-	-	0.7	A
VCC Operating Current $I_{VCC-work}$		-	3	5	mA
VCC Sleep-mode Current $I_{VCC-sleep}$		-	60	100	μA
Rdson (High-side MOS + Low-side MOS)	Sink Current = 1A Operating Junction Temperature T_J < 150℃	-	0.7	1	Ω

Note

[1] Depending on the sample batch, the VCC voltage rise rate ranges from 0.5 V/μs to 5 V/ms

4.3 Protection Electrical Characteristics

Table 4-7 Protection Electrical Characteristics

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC OVP Threshold Voltage V_{ovp}		6.8	7	7.2	V
TSD Threshold Temperature T_{TSD}		-	165	-	℃
OCP Threshold I_{OCP}		1.8	-	-	A
MLP Detection Time T_{on}		-	0.7	-	s
MLP Recover Time T_{off}		-	5	-	s

4.4 IO Electrical Characteristics (SPEED/FG)

Table 4-8 IO Electrical Characteristics (SPEED/FG)

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SPEED Pin High-level Input Voltage V_{IH}	VCC = 5V	1.8	-	V_{CC} + 0.3	V
	VCC = 2V	1.2	-	2	V
SPEED Pin Low-level Input Voltage V_{IL}	VCC = 5V	-0.3	-	0.8	V
	VCC = 2V	-0.3	-	0.4	V
FG Pin Low-level Output Voltage V_{FG}	I_{FG} = 5mA	-	0.1	0.3	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
FG Pin Leakage Current I_{FGL}	V_{FG} = 5V	-	< 0.1	1	μA

4.5 PWM Input Frequency

Table 4-9 PWM Input Frequency

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWM Input Frequency	MOD Pin Configuration by Default	0.3	-	62.5	kHz
	Input Voltage on MOD Pin: 3/8 VCC ~ 1/2 VCC	0.02	-	62.5	kHz

4.6 SVPWM Frequency

4.6.1 FT3207N

Table 4-10 SVPWM Frequency of FT3207N

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SVPWM Frequency		-	60	-	kHz

4.6.2 FT3207NA

Table 4-11 SVPWM Frequency of FT3207NA

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SVPWM Frequency		-	93.75	-	kHz

4.6.3 FT3207P

Table 4-12 SVPWM Frequency of FT3207P

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SVPWM Frequency		-	93.75	-	kHz

4.7 Package Thermal Resistance

4.7.1 FT3207N

Table 4-13 DFN10 Package Thermal Resistance

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	119	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	38	℃/W

4.7.2 FT3207NA

Table 4-14 DFN10 Package Thermal Resistance

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	119	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	38	℃/W

4.7.3 FT3207P

Table 4-15 DFN10 Package Thermal Resistance

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	155	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	85	℃/W

Note

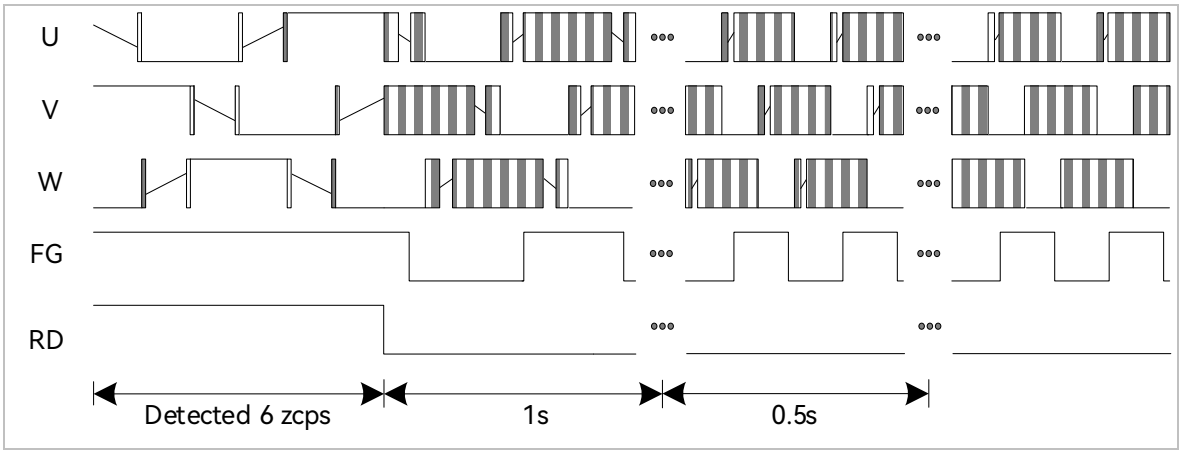
[1] The actual measurements may vary depending on the conditions

5 Function Descriptions

5.1 Startup

The chip supports full duty-cycle startup and soft startup. The former starts with a large output torque and a short starting period, while the latter limits start current to the desired level and is suitable for motors that required reduced current during startup.

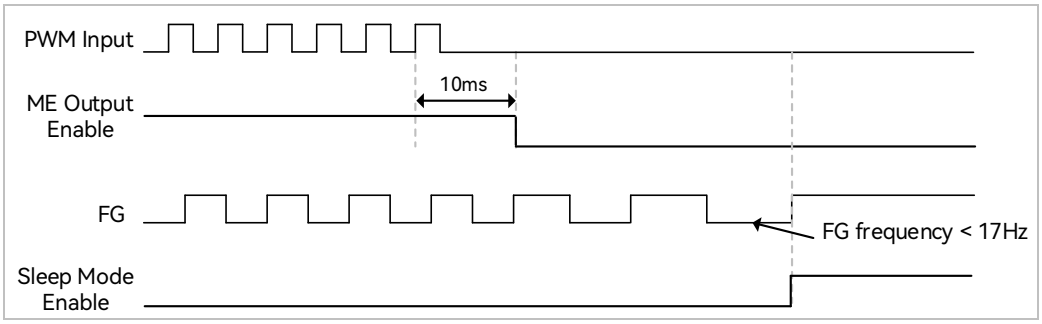
Figure 5-1 Full Duty-cycle Startup



5.2 Rapid Shutdown

During operation, if 20Hz (the low-frequency limit) is not selected for PWM input frequency via MOD pin, the chip turns off the output when it does not detect PWM input in 10ms, enters the sleep mode and low-side conduction brakes after its speed falls to 17Hz. The sleep-mode current of the chip is about 60μA.

Figure 5-2 Timing Diagram of Sleep Mode



5.3 DIR

DIR pin configuration decides motor rotation direction, startup mode and drive mode. See Table 5-1 for the mapping between R_{DIR} and motor functions.

Table 5-1 Mapping between R_{DIR} and Motor Functions

R_{DIR}	Motor Functions		
GND	Reverse Rotation	No Soft Startup	Five-segment SVPWM
20kΩ	Forward Rotation	Soft Startup	Five-segment SVPWM
51kΩ	Forward Rotation	No Soft Startup	Seven-segment SVPWM
Disconnected	Forward Rotation	No Soft Startup	Five-segment SVPWM

Note

Only FT3207N and FT3207NA supports seven-segment sine wave drive

5.4 CSEL

CSEL pin decides forced commutation time and lead angle mode. See Table 5-2 for Mapping between R_{CSEL}/C_{CSEL} and Forced Commutation Time/Lead Angle Mode.

Table 5-2 Mapping between R_{CSEL}/C_{CSEL} and Forced Commutation Time/Lead Angle Mode

R_{CSEL}	C_{CSEL}	Forced Commutation Time	Lead Angle Mode
Floating	4.7nF	149ms	Fixed Lead Angle (10°)
	3.3nF	105ms	
	2.2nF	70ms	
	1nF	32ms	
	Floating	120ms	
30kΩ	4.7nF	180ms	Automatic Lead Angle (Up to 45°)
	3.3nF	127ms	
	2.2nF	85ms	
	1nF	39ms	
	Floating	120ms	
GND	Floating	120ms	Automatic Lead Angle (Up to 45°)

5.5 MOD

MOD pin is used to configure FG frequency division coefficient and PWM input frequency. See Table

5-3 for the mapping between R_{MOD1}/R_{MOD2} and function parameters.

Table 5-3 Mapping between R_{MOD1}/R_{MOD2} and Function Parameters

MOD Pin Input Voltage	R_{MOD1}	R_{MOD2}	FG/RD	PWM Input	Special Functions
GND - 1/8 VCC	Disconnected	GND	1/3*FG	0.3kHz ~ 62.5kHz	-
1/8 VCC - 1/4 VCC	39kΩ	10kΩ	2/3*FG	0.3kHz ~ 62.5kHz	-
1/4 VCC - 3/8 VCC	30kΩ	15kΩ	1/2*FG	0.3kHz ~ 62.5kHz	-
3/8 VCC - 1/2 VCC	24kΩ	20kΩ	FG	20Hz ~ 62.5kHz	-
1/2 VCC - 5/8 VCC	20kΩ	24kΩ	FG	0.3kHz ~ 62.5kHz	50% duty cycle output after the motor is locked
5/8 VCC - 3/4 VCC	15kΩ	30kΩ	FG	0.3kHz ~ 62.5kHz	Run with 10% duty cycle if duty cycle is lower than 10%. The sleep mode is disabled.
3/4 VCC - 7/8 VCC	10kΩ	39kΩ	RD	0.3kHz ~ 62.5kHz	-
7/8 VCC - VCC	VCC	Disconnected	FG	0.3kHz ~ 62.5kHz	-

5.6 Short-circuit Protection

The chip detects U/V/W phases at the same time. If short circuit occurs when any phase is connected to the power supply or ground, the chip turns off the outputs immediately and restarts after 5s.

5.7 Over-voltage Protection (OVP)

When VCC pin voltage is higher than 7V, the chip enables OVP feature and enters the brake state. In this case, if the VCC pin voltage falls below 7V in a short period of time, the chip restores its output.

5.8 Over-current Protection (OCP)

When the phase current is higher than I_{OCP}, the chip enables OCP feature, stops output, and restart after 5s.

5.9 Motor Lock Protection (MLP)

The chip supports motor lock protection to prevent the motor from burning out. When motor lock fault occurs, the chip turns off the output and restarts after 5 seconds.

5.10 Temperature Sensor Detect (TSD)

The chip automatically turns off the output when the junction temperature exceeds 165°C, and resumes normal operation after the temperature drops below 140°C.

6 IO Equivalent Circuits

The IO equivalent circuits of FT3207 are shown as below.

Figure 6-1 Three-phase Output (U/V/W)

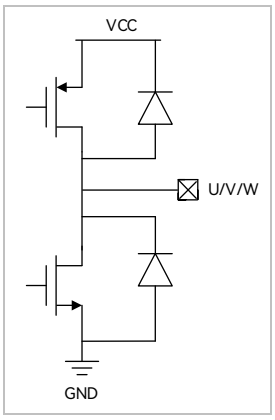


Figure 6-2 PWM Control Signal Input (SPEED)

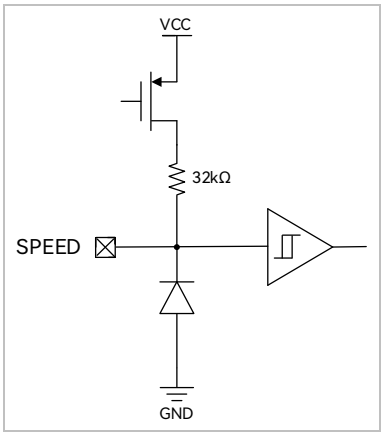


Figure 6-3 Speed Signal Output (FG)

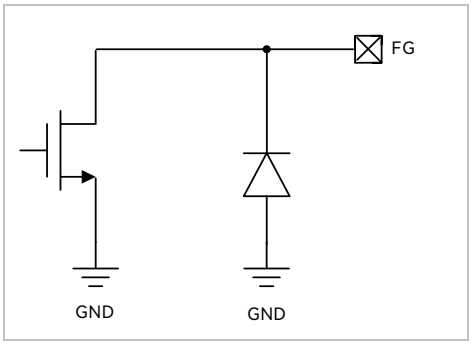


Figure 6-4 MOD Mode Selection (MOD)

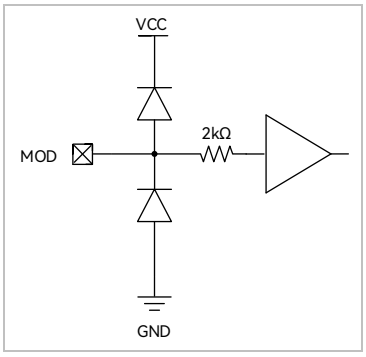


Figure 6-5 Motor Neutral Point Input (COM)

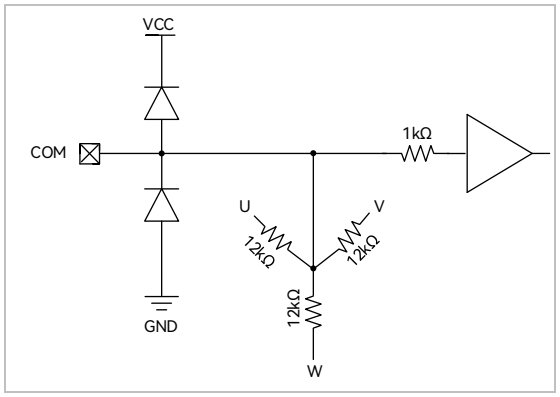


Figure 6-6 Forced Commutation Time Selection (CSEL)

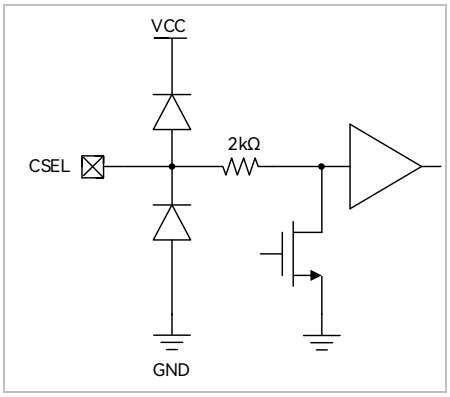


Figure 6-7 Motor Operation Mode Selection (DIR)

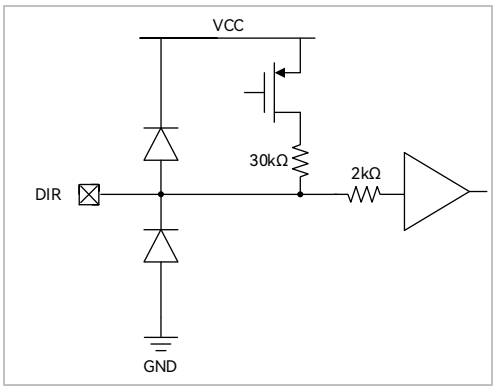
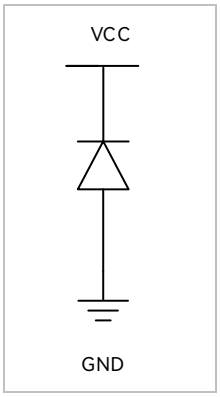


Figure 6-8 Power Supply (VCC)

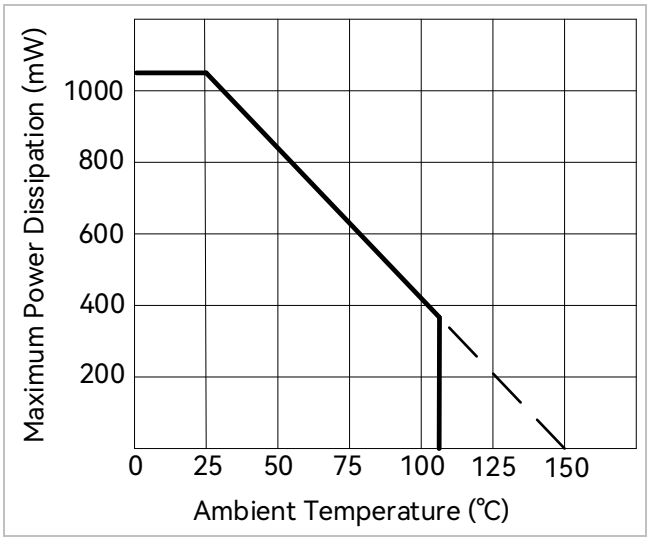


7 Maximum P_d VS. Ambient Temperature

7.1 FT3207N

The relation between maximum power dissipation of FT3207N and ambient temperature is shown as below.

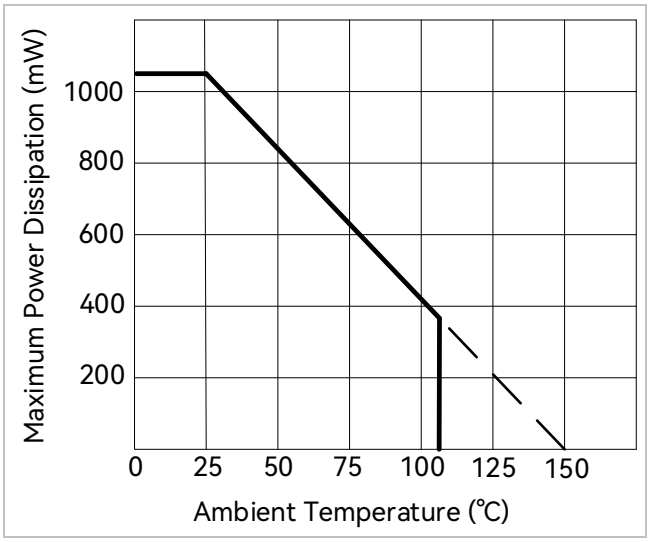
Figure 7-1 Maximum Power Dissipation VS. Ambient Temperature of FT3207N



7.2 FT3207NA

The relation between maximum power dissipation of FT3207NA and ambient temperature is shown as below.

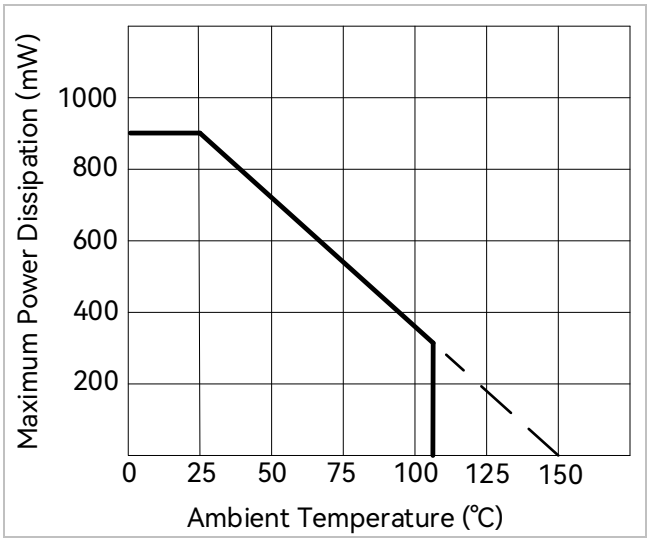
Figure 7-2 Maximum Power Dissipation VS. Ambient Temperature of FT3207NA



7.3 FT3207P

The relation between maximum power dissipation of FT3207P and ambient temperature is shown as below.

Figure 7-3 Maximum Power Dissipation VS. Ambient Temperature of FT3207P



8 Revision History

Rev.	Description	Date	Prepared By
V1.1	First release, translated from Chinese version 1.1	2024/09/24	Eric Deng
V1.2	1. Added product picture; 2. Added values of "PWM High-level Input Voltage V_{IH}" and "PWM Low-level Input Voltage V_{IL}" when VCC = 2V in Table 4-4 IO Electrical Characteristics (SPEED);	2024/11/13	Freya Fu
V1.3	1. Added short-circuit protection module in Figure 1-2 Functional Block Diagram of FT3207; 2. Added descriptions on short-circuit protection; 3. Modified "T_A = 25℃ (Average)" in Table 4-2 Global Electrical Characteristics as "T_A = 85 ℃ (Average)", deleted the parameter Peak Phase Current I_{PHASE}, and added test conditions "Sink Current = 1A" and Operating Junction Temperature T_J < 150℃" to the parameter Rdson (High-side MOS + Low-side MOS); 4. Updated the value of VCC OVP Threshold Voltage V_{ovp} in Table 4-3 Protection Electrical Characteristics.	2024/11/21	Freya Fu
V1.4	1. Added the parameter "Power Dissipation P_d" in Table 4-1 Absolute Maximum Ratings, and changed the parameter name "IO to VSS Voltage" as "Other IOs to VSS Voltage Except VCC" and modified its maximum value 7V as VCC; 2. Added "T_A = 25℃ unless otherwise specified" to table titles in section 4.1 Absolute Maximum Ratings ~ 4.6 SVPWM Frequency; 3. Added the parameters "FG Pin Low-level Output Voltage V_{FG}" and "FG Pin Leakage Current I_{FGL}" to Table 4-4 IO Electrical Characteristics, and changed the parameter name "PWM High-level Input Voltage V_{IH}" and "PWM Low-level Input Voltage V_{IL}" as " SPEED Pin High-level Input Voltage V_{IH}" and "SPEED Pin Low-level Input Voltage V_{IL}" respectively; 4. Updated "Automatic Mode" in section 5.4 CSEL as "Lead Angle Mode" and added its descriptions; 5. Added chapter 6 IO Equivalent Circuits; 6. Added chapter 7 Maximum P_d VS. Ambient Temperature.	2024/12/23	Eric Deng
V1.5	Updated the value 93℃/W of Junction-to-ambient Thermal Resistance θ_{JA} in section 4.7 Package Thermal Resistance as 119℃/W, and deleted the parameter Junction-to-case Thermal Resistance θ_{JC}	2024/12/31	Eric Deng

Rev.	Description	Date	Prepared By
V1.6	1. Updated minimum value 0.8V of SPEED Pin High-level Input Voltage V_{IH} (VCC = 2V) in section Table 4-4 IO Electrical Characteristics as 1.2V, and maximum value 0.6V of SPEED Pin Low-level Input Voltage V_{IL} (VCC = 2V) as 0.4V; 2. Updated descriptions in section 5.7 Over-voltage Protection (OVP).	2025/01/16	Eric Deng
V1.7	1. Added descriptions related to OCP; 2. Added parameters of "MLP Detection Time T_{on}" and "MLP Recover Time T_{off}" in 4.3 Protection Electrical Characteristics; 3. Added parameters of "Junction-to-case Thermal Resistance θ_{JC}" in 4.7 Package Thermal Resistance	2025/08/14	Freya Fu
V2.0	1. Added descriptions of FT3207NA and FT3207P; 2. Modified "auto field weakening control" as "auto lead angle"; 3. Added Note "Depending on the sample batch, the VCC voltage rise rate ranges from 0.5 V/μs to 5 V/ms" to 4.2 Global Electrical Characteristics	2025/09/26	Freya Fu
V2.1	1. Added Min. to "OCP Threshold I_{OCP}" and deleted its Test Conditions T_A and Typ. in 4.3 Protection Electrical Characteristics; 2. Modified "When the phase current is higher than 2A, the chip enables……" as "When the phase current is higher than I_{OCP}, the chip enables……" in 5.8 Over-current Protection; 3. Updated format.	2025/10/28	Freya Fu
V2.2	Updated the carrier frequency of SVPWM from "60kHz" to "93.75kHz" for FT3207P.	2025/12/30	Freya Fu

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