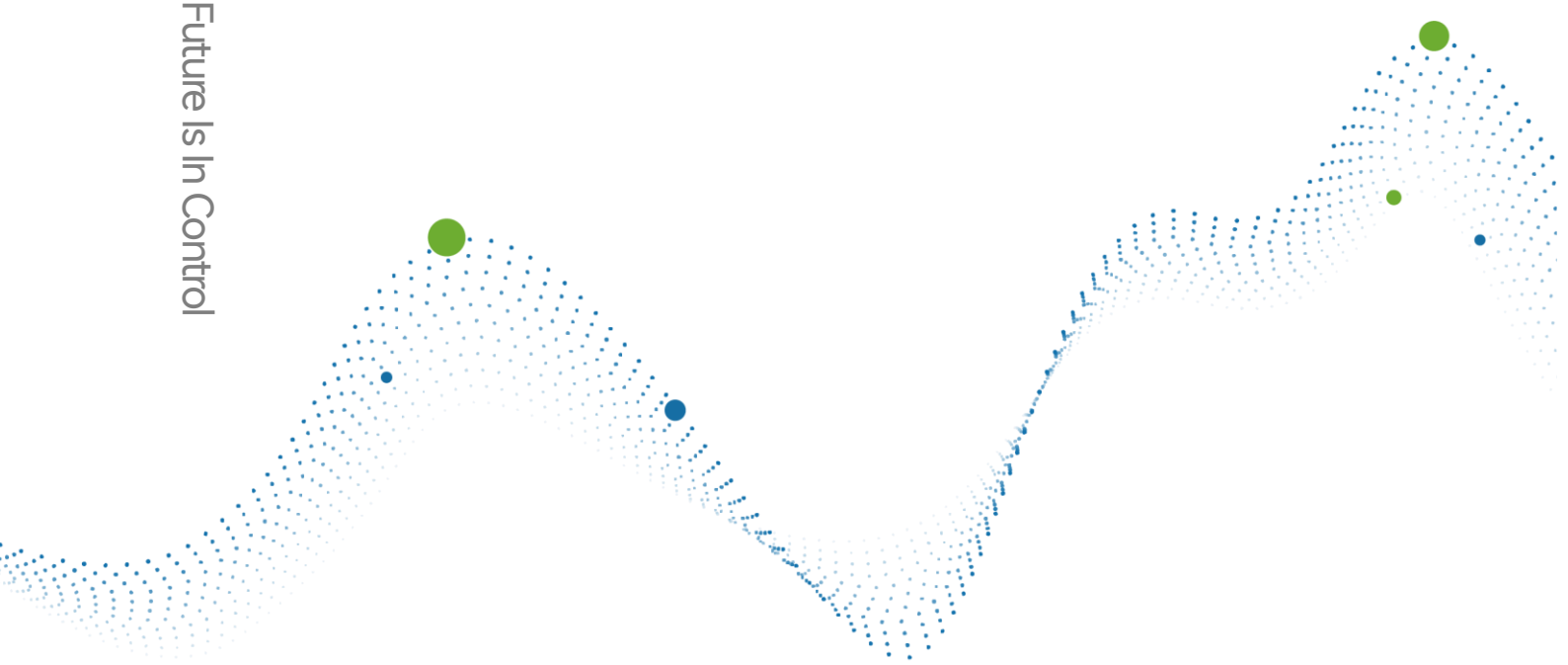
Fortior Tech

DATASHEET

FT8171Q

Three-phase BLDC Motor Controller with a Built-in Pre-driver

Future Is In Control



Version No.: V1.0

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1 System Introduction

1.1 Overview

FT8171Q is an IC with a built-in pre-driver designed for three-phase BLDC motor drive applications. Due to a high level of integration, few peripheral components are required. The chip supports sensored SVPWM and sensorless FOC to reduce audible noise and minimize torque ripple in motor drives. Motor parameters, startup control parameters, and speed control modes can be configured via GUI, and are stored in built-in EEPROM.

Analog voltage, PWM, CLOCK, or I²C interface mode is optional for motor speed control. Moreover, the chip integrates the speed indicator, which reads motor speed in real time via the FG/RD/SDA pin or I²C interface. FT8171Q provides multiple protection mechanisms, such as overcurrent, current limiting, undervoltage, thermal shutdown (TSD), stall, phase loss, speed limiting, VDC overvoltage protection (OVP) or undervoltage lockout (UVLO), Hall abnormality, and sleep mode. The chip also supports power closed-loop control.

1.2 Applications

Personal cooling garment (PCG), a wearable device that removes heat from the body to maintain thermal comfort in high-temperature environments.

Figure 1-1 FT8171Q



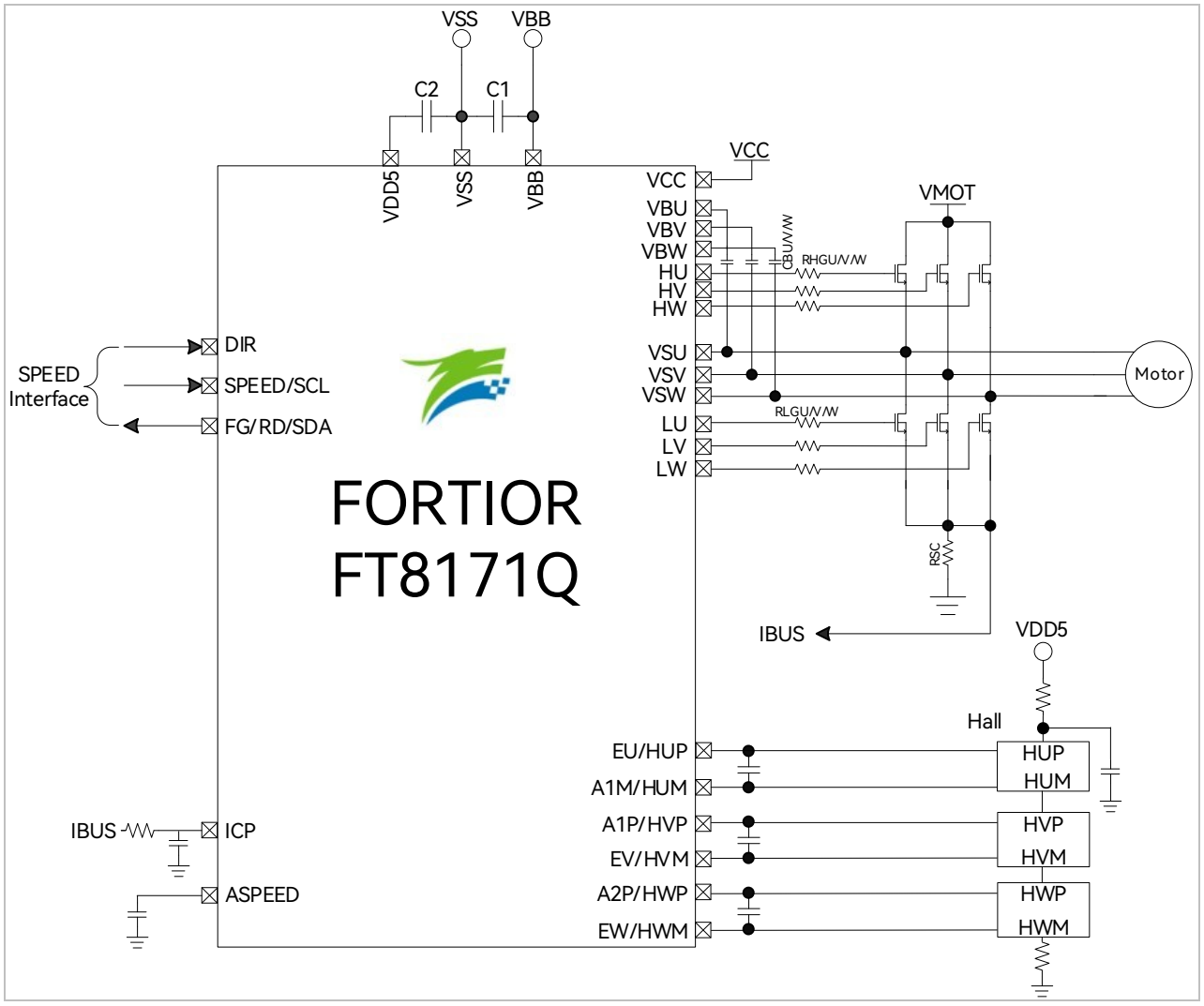
1.3 Features

- VCC voltage range: 5.5V ~ 42V
- Sensorless FOC
- Sensored FOC (Hall-IC or Hall-sensor)
- Sensored SVPWM (Hall-IC or Hall-sensor)
- 6N pre-driver with configurable deadtime
- Drive current: +0.2A or -0.2A
- Control modes: constant speed, constant current, and constant power
- Forward and reverse direction control
- FG and RD output
- Motor speed control modes: analog voltage, PWM, CLOCK, and I²C interface
- Multi-segment lead angle curve to fit motor characteristics
- Soft-on and soft-off functions for smooth motor start-up and shutdown, reducing operational noise
- Multiple protection mechanisms: overcurrent, current limiting, undervoltage, TSD, stall, phase loss, speed limiting, VDC UVLO/OVP, and Hall abnormality

1.4 Typical Application Diagram

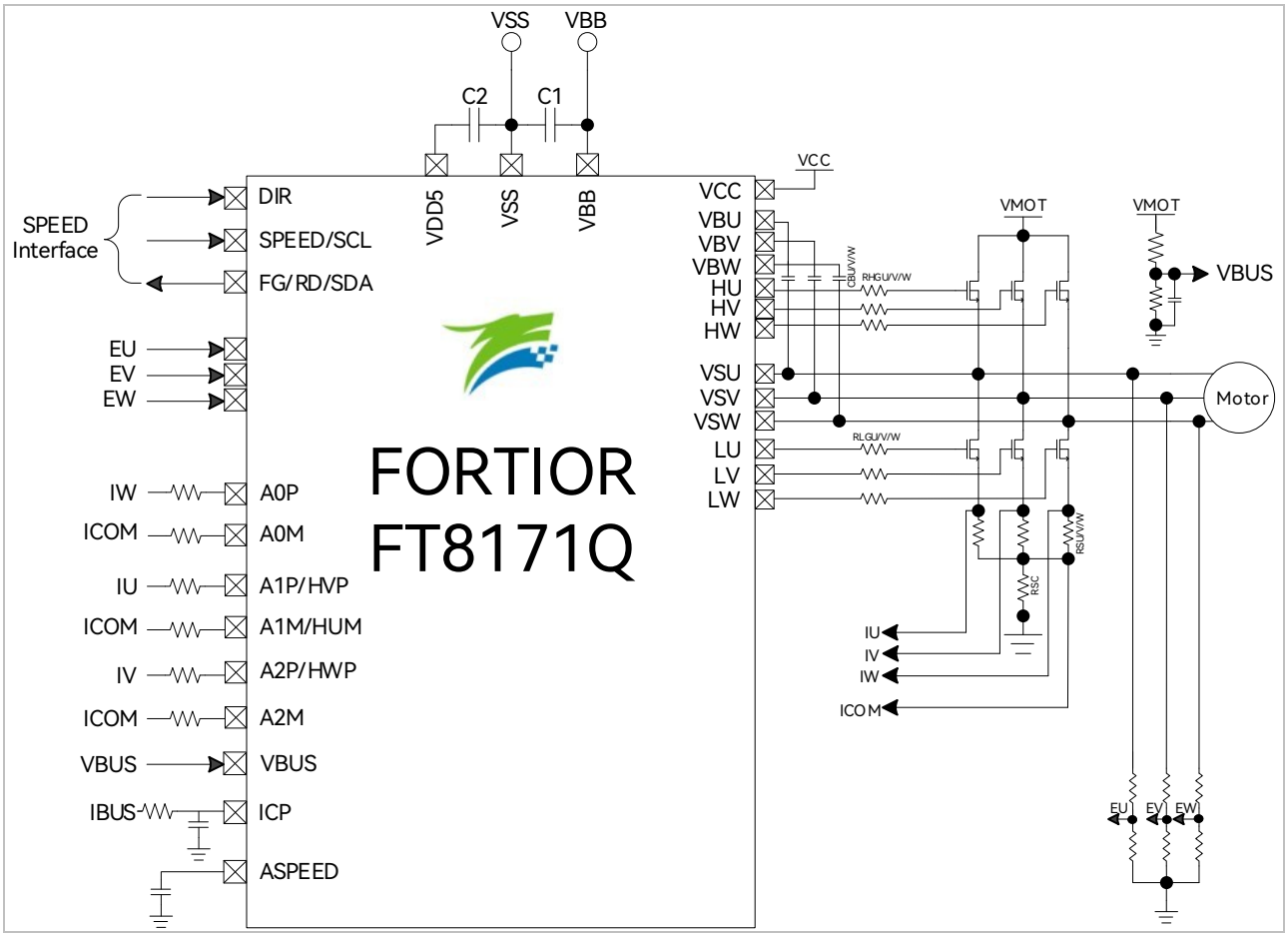
1.4.1 Sensored SVPWM Mode

Figure 1-2 Sensored SVPWM Mode



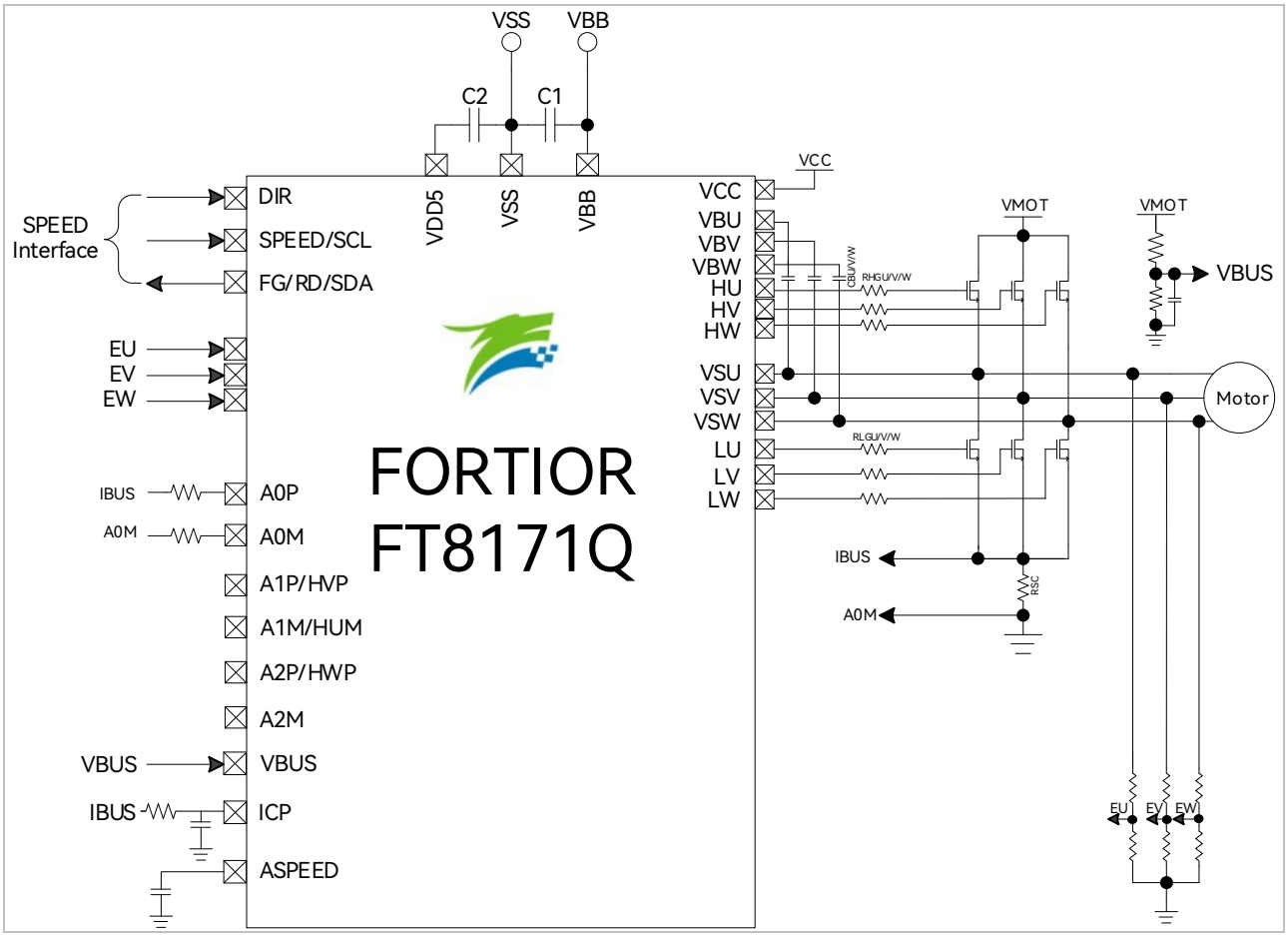
1.4.2 Sensorless FOC Mode with Dual-/Triple-shunt Current Sampling

Figure 1-3 Sensorless FOC Mode with Dual-/Triple-shunt Current Sampling



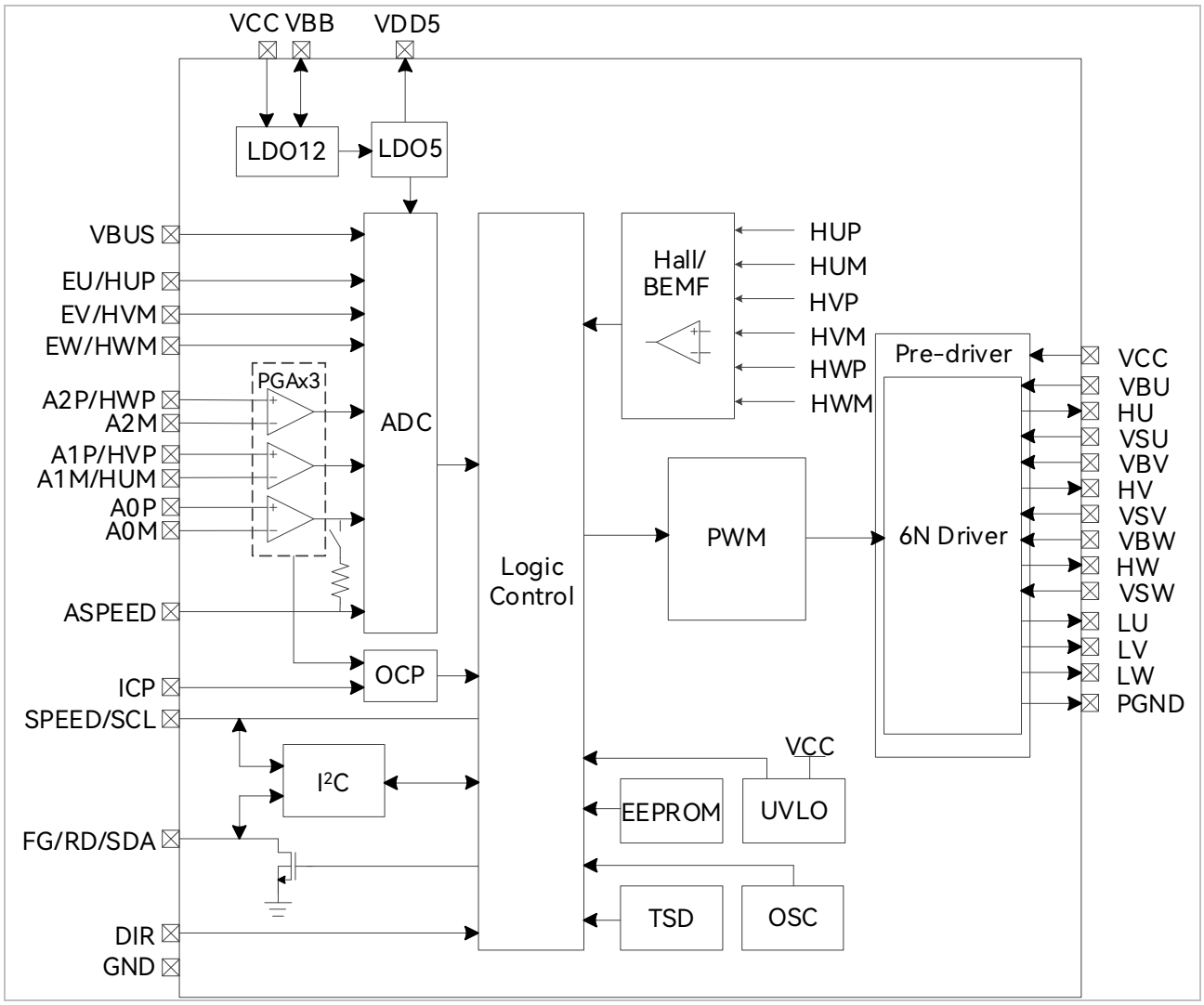
1.4.3 Sensorless FOC Mode with Single-shunt Current Sampling

Figure 1-4 Sensorless FOC Mode with Single-shunt Current Sampling



1.5 Functional Block Diagram

Figure 1-5 FT8171Q Functional Block Diagram



1.6 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DB = Digital Bidirectional
- DO = Digital Output
- AI = Analog Input
- AO = Analog Output
- P = Power Input/Output or Ground

1.6.1 QFN32 Pins

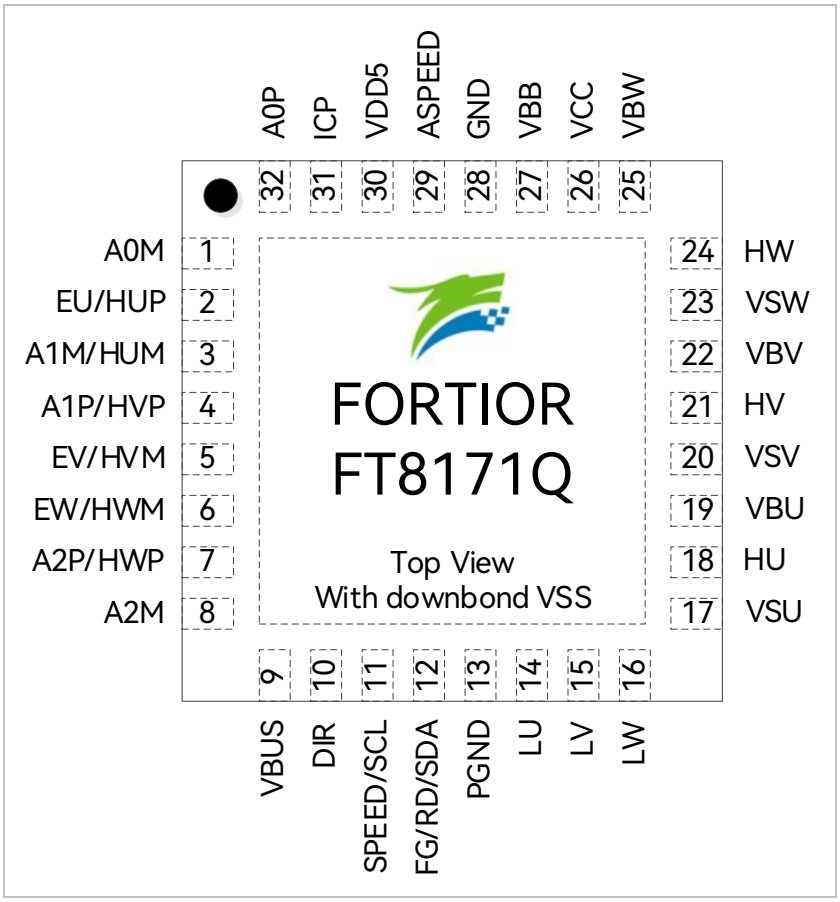
Table 1-1 QFN32 Pins

Pin	FT8171Q QFN32	IO Type	Function Descriptions
A0M	1	AI	AMP0 negative input
EU/ HUP	2	AI/ AI	U-phase BEMF voltage input Differential Hall sensor positive input for U-phase or Hall IC input for U-phase
A1M/ HUM	3	AI/ AI	AMP1 negative input Differential Hall sensor negative input for U-phase
A1P/ HVP	4	AI/ AI	AMP1 positive input Differential Hall sensor positive input for V-phase
EV/ HVM	5	AI/ AI	V-phase BEMF voltage input Differential Hall sensor negative input for V-phase or Hall IC input for V-phase
EW/ HWM	6	AI AI	W-phase BEMF voltage input Differential Hall sensor negative input for W-phase or Hall IC input for W-phase
A2P/ HWP	7	AI/ AI	AMP2 positive input Differential Hall sensor positive input for W-phase
A2M	8	AI	AMP2 negative input
VBUS	9	AI	VDC bus voltage input after voltage division
DIR	10	DI	Motor rotation control, with built-in pull-up resistor 1: Forward rotation. U --> V --> W. 0: Reverse rotation. U --> W --> V.
SPEED/ SCL	11	DI/ DB	Motor PWM/CLOCK speed control signal input, frequency range: 100Hz ~ 100kHz I^2C SCL

Pin	FT8171Q QFN32	IO Type	Function Descriptions
FG/RD/ SDA	12	DO/ DB	Motor speed signal or motor stall indication, with collector open-drain output I²C SDA, configured as collector open-drain output
PGND	13	P	Power Ground
LU	14	DO	6N pre-driver low-side U-phase output
LV	15	DO	6N pre-driver low-side V-phase output
LW	16	DO	6N pre-driver low-side W-phase output
VSU	17	P	6N pre-driver U-phase input, as GND reference for U-phase high-side bootstrap
HU	18	DO	6N pre-driver high-side U-phase output
VBU	19	P	6N pre-driver high-side U-phase bootstrap power supply
VSV	20	P	6N pre-driver V-phase input, as GND reference for V-phase high-side bootstrap
HV	21	DO	6N pre-driver high-side V-phase output
VBV	22	P	6N pre-driver high-side V-phase bootstrap power supply
VSW	23	P	6N pre-driver W-phase input, as GND reference for W-phase high-side bootstrap
HW	24	DO	6N pre-driver high-side W-phase output
VBW	25	P	6N pre-driver high-side W-phase bootstrap power supply
VCC	26	P	Power supply input, range: 5.5V ~ 42V
VBB	27	P	12V LDO output, connected to GND with a 1μF capacitor
GND	28	P	Digital ground
ASPEED	29	AI	Analog voltage input for motor speed control
VDD5	30	P	5V LDO output, connected to GND with a 1μF capacitor
ICP	31	AI	Overcurrent detection input
A0P	32	AI	AMP0 positive input

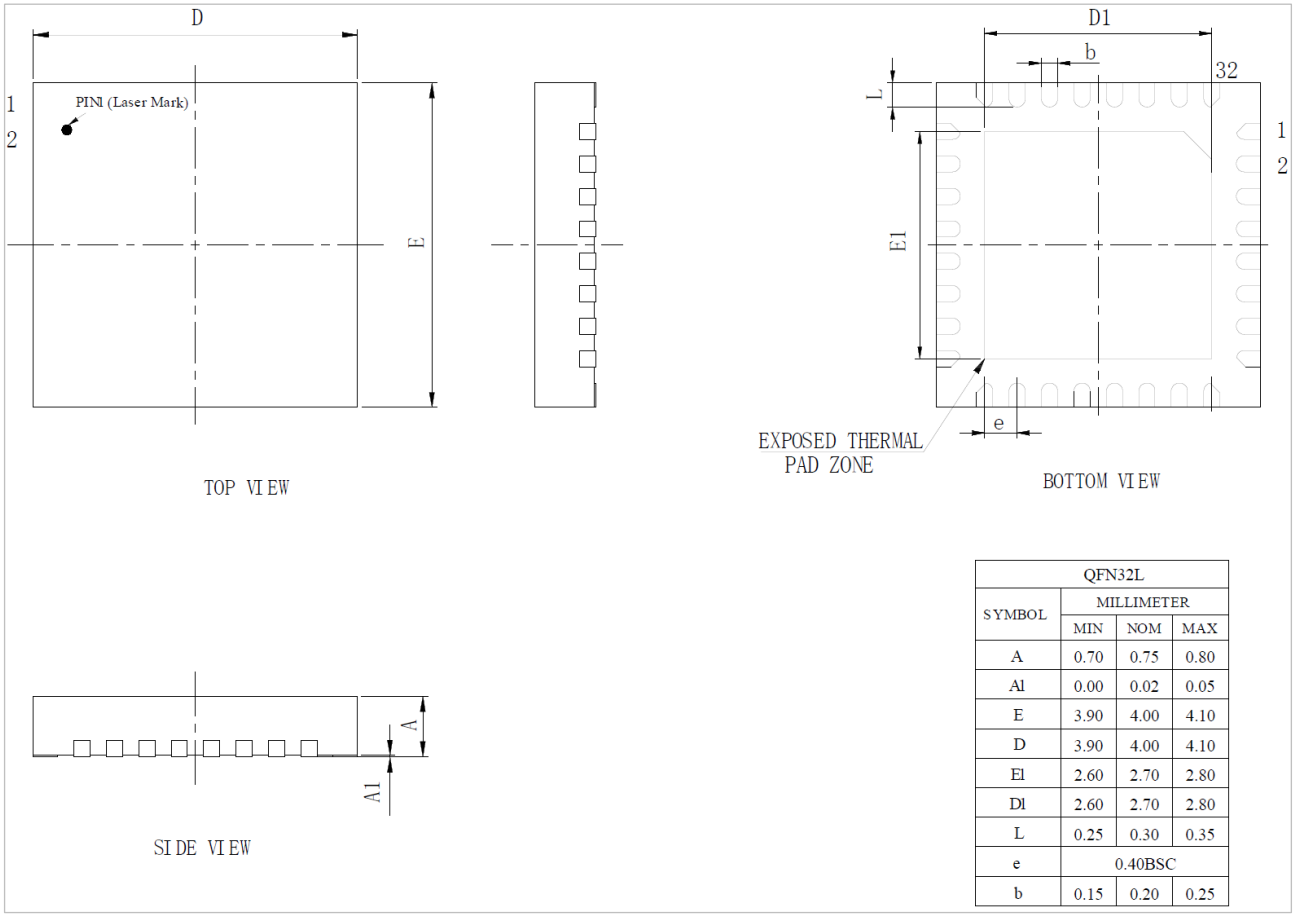
1.6.2 QFN32 Pinout Diagram

Figure 1-6 QFN32 Pinout Diagram



2 Package Information

Figure 2-1 FT8171Q Package Drawings and Dimensions



SYMBOL	QFN32L MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
E	3.90	4.00	4.10
D	3.90	4.00	4.10
E1	2.60	2.70	2.80
D1	2.60	2.70	2.80
L	0.25	0.30	0.35
e	0.40BSC		
b	0.15	0.20	0.25

3 Ordering Information

Table 3-1 Model Selections

Model	Power Supply (V)	Driver Interface	Control Features						Protection Features								Operating Junction Temperature T_J(°C)	Lead-free	Package
			Drive Type	Speed Control			Forward and Reverse Rotation	Initial Position Detection	Over-current Protection/Current Limiting Protection	UVLO	TSD	Motor Stall Protection	Phase Loss Protection	Configurable Maximum Speed Protection	VDC UVLO/OVP	HALLERR Protection			
				I²C	PWM/CLOCK	Analog Voltage													
FT8171Q	5.5 ~ 42	6N pre-driver	Sensored/ Sensorless Sine-wave	√	√	√	√	√	√	√	√	√	√	√	√	√	-40 ~ 150	√	QFN32 (4x4mm)

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stress values greater than Table 4-1 Absolute Maximum Ratings may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Table 4-1 Absolute Maximum Ratings

(T_A = 25℃ and VCC = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature		-55	-	150	℃
Operating Ambient Temperature T_A		-40	-	85	℃
VCC to GND Voltage		-0.3	-	45	V
VDD5 to GND Voltage		-0.3	5	6.5	V
High-side Bootstrap Voltage $V_{BU,BV,BW}$		-	65	-	V
High-side Floating Offset Voltage $V_{SU,SV,SW}$		-	55	-	V
High-side Output Voltage $V_{HU,HV,HW}$		-	65	-	V
Low-side Output Voltage $V_{LU,LV,LW}$		-1.3	-	20	V
Other IOs to GND Voltage		-0.3	-	VDD5 + 0.3	V
VBB to GND Voltage		-1.3	-	20	V

4.2 Global Electrical Characteristics

Table 4-2 Global Electrical Characteristics

(T_A = 25℃ and VCC = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage		5.5	-	42	V
VCC Operating Current I_{VCC}		-	15	25	mA
VCC Standby Current I_{VCC}		-	5	-	mA
VCC Sleep Current I_{VCC}		-	180	-	μA

4.3 IO Electrical Characteristics

Table 4-3 IO Electrical Characteristics

(T_A = 25°C and VCC = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Voltage V_{IH}(DIR/SPEED/FG)		0.6*VDD5	-	-	V
Low-level Input Voltage V_{IL}(DIR/SPEED/FG)		-	-	0.2*VDD5	V
SPEED/DIR/A1P Pull-up Resistor		-	33	-	kΩ
SPEED Pull-down Resistor		-	22	-	kΩ
EW/EV/EU/A2M Pull-up Resistor		-	5.6	-	kΩ
FG Pull-up Resistor		-	4.7	-	kΩ

4.4 6N Pre-driver Electrical Characteristics

Table 4-4 6N Pre-driver Electrical Characteristics

(T_A = 25°C and VCC = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	1nF load, from 10% to 90%	-	70	-	ns
Turn-off Fall Time	1nF load, from 90% to 10%	-	50	-	ns
Deadtime		-	120	-	ns
DRV High-level Output Voltage V_{OH}	I_O = 10mA	-	0.2	0.4	V
DRV Low-level Output Voltage V_{OL}	I_O = 10mA	-	0.15	0.25	V
DRV High-level Output Short-circuit Pulse Current I_{OH}	V_O = 0V	-	0.2	-	A
DRV Low-level Output Short-circuit Pulse Current I_{OL}	V_O = 15V	-	0.2	-	A
DRV High-side Passive Pull-down Resistor		-	50	-	kΩ
DRV Low-side Passive Pull-down Resistor		-	50	-	kΩ

4.5 LDO Electrical Characteristics

Table 4-5 LDO Electrical Characteristics

(T_A = 25°C and VCC = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VBB Voltage		11	12	13	V
VDD5 Operating Voltage		4.8	5	5.2	V

4.6 PWM/CLOCK Input Frequency

Table 4-6 PWM/CLOCK Input Frequency

(T_A = 25°C and VCC = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWM Input Frequency		0.1	-	100	kHz
CLOCK Input Frequency		20	-	1400	Hz

4.7 Speed Control in Analog Voltage Mode

Table 4-7 Speed Control in Analog Voltage Mode

(T_A = 25°C and VCC = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ASPEED Input Voltage		0	-	VDD5	V

4.8 Package Thermal Resistance

Table 4-8 QFN32 Package Thermal Resistance

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	47	°C/W
	JEDEC standard, 1S0P PCB	74	°C/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	20	°C/W

Note:

[1] The actual measurements may vary depending on the conditions.

5 Function Descriptions

5.1 DIR

Forward or reverse direction control (DIR) pin is used to reverse motor rotation by changing the DIR level. An internal pullup holds this pin "High" by default.

5.2 ASPEED

Analog voltage speed control (ASPEED) pin is used to input analog voltage for motor speed control.

5.3 SPEED/SCL

Speed control (SPEED/SCL) pin is used to input duty cycle or frequency for speed control depending on the settings. In addition, SPEED/SCL pin serves as the serial clock line (SCL) for I²C communication.

5.4 FG/RD/SDA

Speed feedback and fault indication (FG/RD/SDA) pin is an open-drain output. When this pin is set to FG, it outputs speed feedback signal to indicate rotation speed of the motor; when it is set to RD, it outputs high-level signal to indicate the fault state. In addition, this pin serves as the serial data line (SDA) for I²C communication.

5.5 Speed Control

5.5.1 Speed Control Modes

The chip supports PWM, analog voltage, I²C, and CLOCK modes for speed control, and only one of them can be chosen at a time. In analog voltage mode, the voltage value input to ASPEED pin controls the speed; in PWM or CLOCK mode, the duty cycle of the PWM or CLOCK signal input to SPEED/SCL pin controls the speed; in I²C mode, SPEED/SCL pin serves as the serial clock line (SCL) and FG/RD/SDA pin as the serial data line (SDA).

5.5.2 Speed Control Curve

The control waveform is presented as below, where the x-coordinate refers to the duty cycle of the PWM input (In I²C control and analog voltage control modes, the input can be converted to the corresponding PWM duty cycle), and the y-coordinate refers to the output duty cycle, which represents different physical quantities in different control modes.

The speed control curve is configured by setting the output duty cycle at the start and end points. The start point is determined by X_ON and Y_ON, and the end point by X_Max and Y_Max. The output of other points between them increases linearly as the input varies.

The y-coordinate represents Duty in voltage-loop control mode; Speed in speed-loop control mode; Current in current-loop control mode.

Figure 5-1 Curve in Speed-loop or Current-loop Control Mode (PwmOffMode = 0)

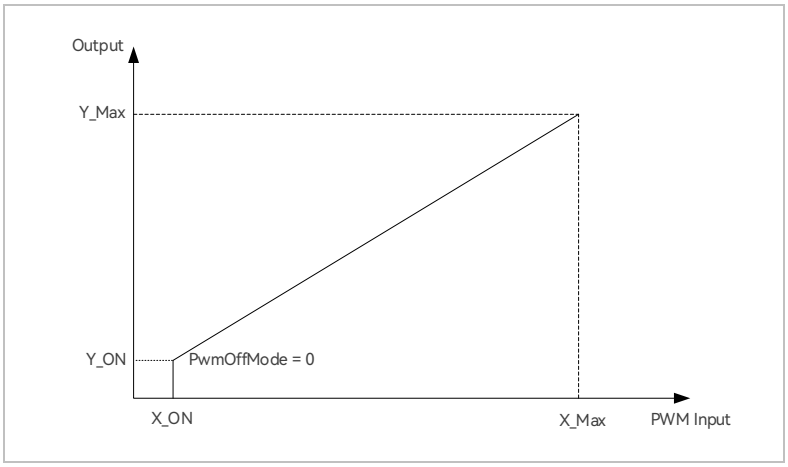
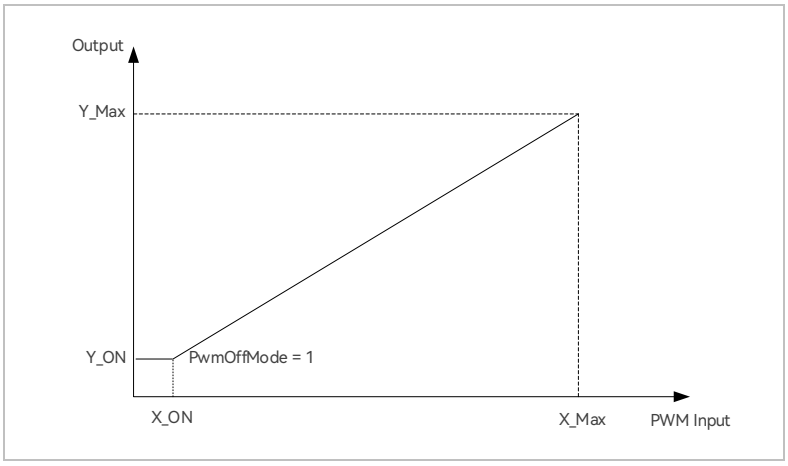


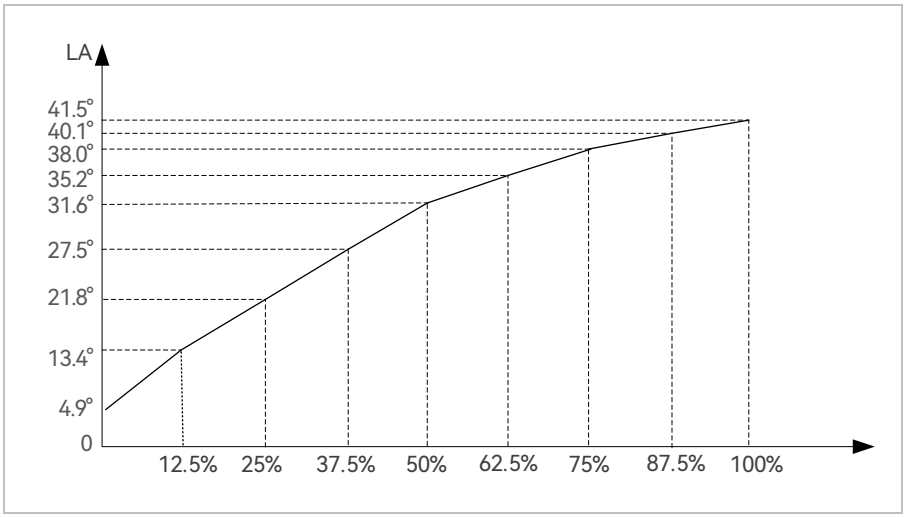
Figure 5-2 Curve in Speed-loop or Current-loop Control Mode (PwmOffMode = 1)



5.6 Lead Angle Curve

In sensored SVPWM control mode, lead angle curve corresponding to duty cycle of the voltage output is shown in Figure 5-3 Lead Angle Curve, where the x-coordinate denotes duty cycle of the PWM voltage output and the y-coordinate represents the lead angle. The multi-segment lead angle curve is developed by setting lead angle at 9 points, which better fits the motor characteristics. Such 9 points are 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, 87.5%, and 100%, respectively, and the maximum angle difference between each two adjacent points is 10.547°.

Figure 5-3 Lead Angle Curve



5.7 Sleep Mode

The motor enters sleep mode in 6s after ASPEED is set to 0V and SPEED pin is connected to GND.

Wakeup conditions: In I²C speed control mode, the chip exits sleep mode after receiving the matched I²C ID. In PWM or CLOCK control mode, the chip exits sleep mode when a high-level voltage is input to SPEED/SCL pin. In analog voltage control mode, the chip exits sleep mode when the voltage of ASPEED pin is greater than 1.5V or when a high-level voltage is input to SPEED/SCL pin.

5.8 Soft-on and Soft-off

Soft-on feature gradually increases the current during start-up, and soft-off feature gradually decreases the current during shut-down. The two features protect the motor from abrupt startup or shutdown and reduce noise during operation.

Figure 5-4 Soft-on Phase Current Waveform

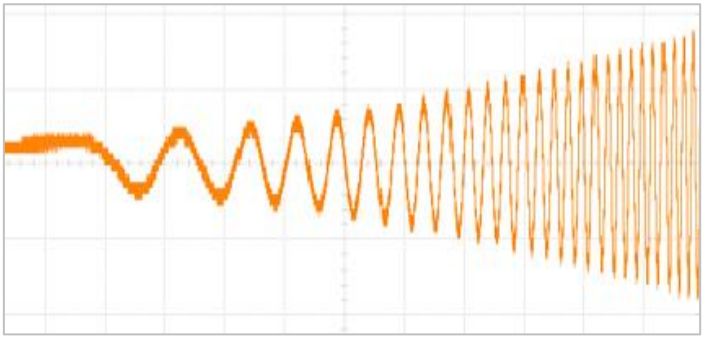
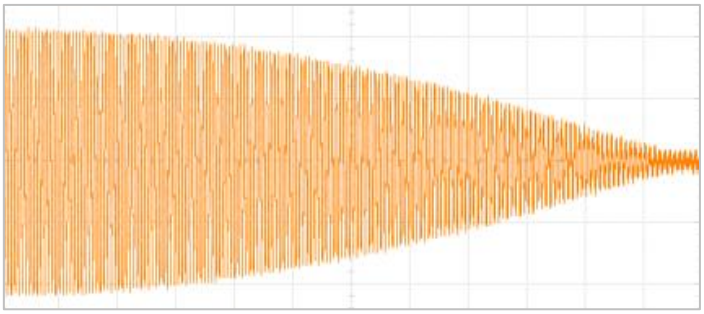


Figure 5-5 Soft-off Phase Current Waveform



5.9 Motor Stall Protection

The stall protection circuit monitors the motor operating state. When stall conditions are met, the chip disables the outputs. It then determines whether to restart based on the fault-restart setting in the program and the selected wait time (6s or 20s).

5.10 Phase Loss Protection

The phase loss protection circuit monitors the motor operating state. When phase loss conditions are met, the chip disables the outputs. It then determines whether to restart based on the fault-restart setting in the program and the selected wait time (6s or 20s).

5.11 Current Limiting Protection

The chip supports current limiting protection in sensored SVPWM mode, where cycle-by-cycle current limiting or average current limiting can be selected. Cycle-by-cycle current limiting is typically used due to its fast response, but excessive noise is generated. Average current limiting is slow to respond, but no noise is generated.

5.12 Overcurrent Protection

When the current exceeds the overcurrent protection threshold, the chip disables the outputs. It determines whether to restart after waiting for 6s based on the fault-restart setting in the program.

5.13 TSD

The internal junction temperature detection module triggers thermal shutdown (TSD) protection when the junction temperature reaches the set threshold. The chip disables the outputs until the junction temperature falls within the normal operating level.

5.14 Configurable Maximum Speed Protection

The maximum operating speed can be programmed. When the output speed exceeds the speed limiting threshold, the output is clamped at that threshold. In practice, some motors—especially in sensored SVPWM mode—may run at excessively high speeds under no-load conditions; limiting the maximum speed effectively protects the motor.

5.15 VCC UVLO

When VCC voltage falls below the UVLO threshold and ASPEED is greater than the startup voltage, the chip enters UVLO state and disables the outputs. It checks VCC voltage every 6s based on the fault-restart setting in the program until VCC voltage recovers to the normal operating level.

5.16 VDC UVLO/OVP

When VDC voltage (the voltage after the VBUS-detection divider) is below or above the VDC UVLO/OVP threshold and when ASPEED is greater than the startup voltage, the chip enters VDC UVLO/OVP state and releases this protection state until VDC voltage recovers to the normal operating level.

5.17 HALLERR Protection

The chip enters the HALLERR protection state and disables the outputs when it detects abnormal Hall input and ASPEED voltage is higher than the threshold voltage. It then determines whether to restart after waiting for 6s based on the fault-restart setting in the program.

5.18 Frequency Multiplication and Division of FG

Configuring FG/RD/SDA to FG outputs FG signal, that is, FG/RD/SDA pin is selected to output FG signal. The output frequency of FG signal is determined by FGDIV (frequency division coefficient) and FGMUL (frequency multiplication coefficient). FGMUL can be set as 1, 3, 4, and 12, while FGDIV as 1, 1/3, 1/4, and 1/5. The formula for the coefficient of output frequency is k = FGMUL*FGDIV.

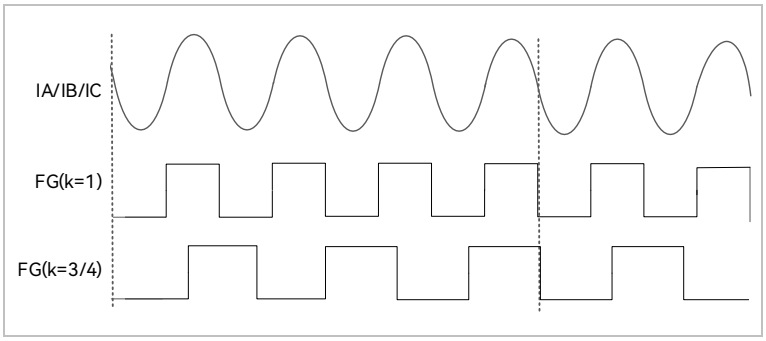
Table 5-1 FG Configurations

Coefficient of Output Frequency (k)		FGMUL			
		1	3	4	12
FGDIV	1	1	3	4	12
	1/3	1/3	3/3	4/3	12/3
	1/4	1/4	3/4	4/4	12/4
	1/5	1/5	3/5	4/5	12/5

The number of FG signals in one mechanical cycle is equal to pp*k (pp refers to the pole-pair number of the motor).

Example: For a 4-pole-pair motor, if FGMUL is set as 3 and FGDIV as 1/4, that is, k = 3/4, three FG signals are displayed in one mechanical cycle (4 * 3/4).

Figure 5-6 FG Output Waveforms at k = 1 and k= 3/4



In sensored mode, if FGx1 or FGx3 is selected, FG signals are output based on the corresponding setting. Otherwise, FG signals are generated based on the configured FGDIV and FGMUL values.

5.19 Speed Control in CLOCK Mode

In this mode, SPEED/SCL pin serves as the input of reference PWM frequency, and motor speed changes with reference PWM frequency. FGMUL and FGDIV are used to set the factor between motor speed and

reference PWM frequency: Motor Speed = (reference PWM frequency*60/pp)/(FGMUL*FGDIV).

Example: For a 5-pole-pair motor, if FGDIV is set as 1/3 and FGMUL as 2 (i.e., k = 2/3) and the reference PWM frequency is 100Hz, then motor speed = (100Hz*60/5) / (2/3) = 1800rpm. In this case, the output frequency from FG pin is determined by FGDIV and FGMUL.

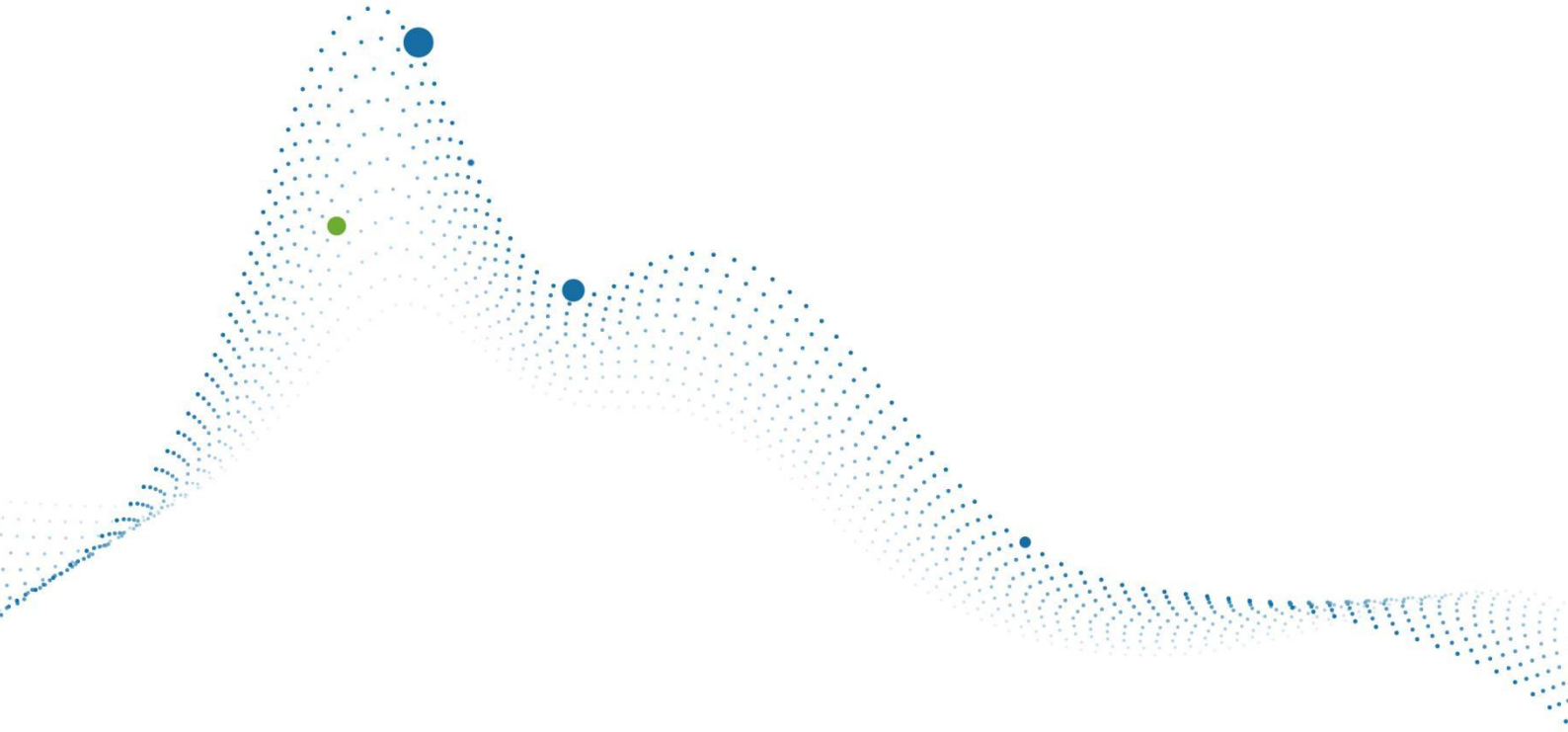
6 Revision History

Rev.	Description	Date	Prepared By
V1.0	First release, translated from Chinese version 1.0	2026/06/29	Joe Luo

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