Datasheet

Fully Integrated IPM for HV Three-phase BLDC Motors
FS92A6AS

Fortior Technology (Shenzhen) Co., Ltd

Contents

1 System Introduction

1.1 Overview

FS92A6AS is a fully integrated IPM for high-voltage three-phase motor drive applications, which integrates 180 sinusoidal commutation controller chip, high-voltage gate driver chip and high-voltage power IC. Due to a high level of integration, few peripheral components are required. The chip supports sensored SVPWM and sensorless FOC to reduce audible noise and minimize torque ripple in motor drives. Moreover, the chip is secured with a wide range of protection features, including over-current protection (OCP), current-limiting protection (CLP), under-voltage lockout (UVLO), temperature sensor detect (TSD), low temperature protection (LTP), motor lock protection (MLP), phase loss protection, configurable maximum speed protection, VDC OVLO/UVLO and abnormal Hall input detection (HALLERR) protection, and also supports sleep mode. With high thermal conductivity, low electromagnetic interference and strong insulation, the chip is housed in a compact package and suitable for built-in motors and other space constraint applications.

1.2 Applications

Air conditioners, air purifiers, water pumps, dishwashers, washing machines, etc.

FS92A6AS

1.3 Features

- 650V 6A Trench IGBT(TC = 100°C)
- VCC range: 13V ~ 20V
- Sensored SVPWM and sensorless FOC
- Support power closed-loop control
- Integrated control, drive and high-voltage power IC
- Forward and reverse direction control
- FG pulse output (support 8/10-pole motor or 4/12-pulse output)
- PWM, analog voltage input or I^2C interface for motor speed regulation
- Support multi-stage lead angle curve to fit motor characteristics
- Soft-on feature protects the motor from abrupt startup and reduces noise during operation
- Support protection features, including OCP, CLP, UVLO, TSD, LTP, MLP, phase loss protection, configurable maximum speed protection, VDC UVLO/OVLO, HALLERR protection, etc

1.4 Key Parameters

- IGBT VCE Voltage: 650V
- Single IGBT Drive Current (DC): ± 6A (Max.)
- Single IGBT Drive Current (Pulse): ± 12A (Max.)
- IGBT Saturation Voltage VCE (sat): 1.73V (Typ.)
- Max. Junction Temperature: +150°C
- Power Dissipation: 3.00W

1.5 Typical Application Diagram

1.5.1 Sensored (Three Hall-based Sensors) Differential Input Mode

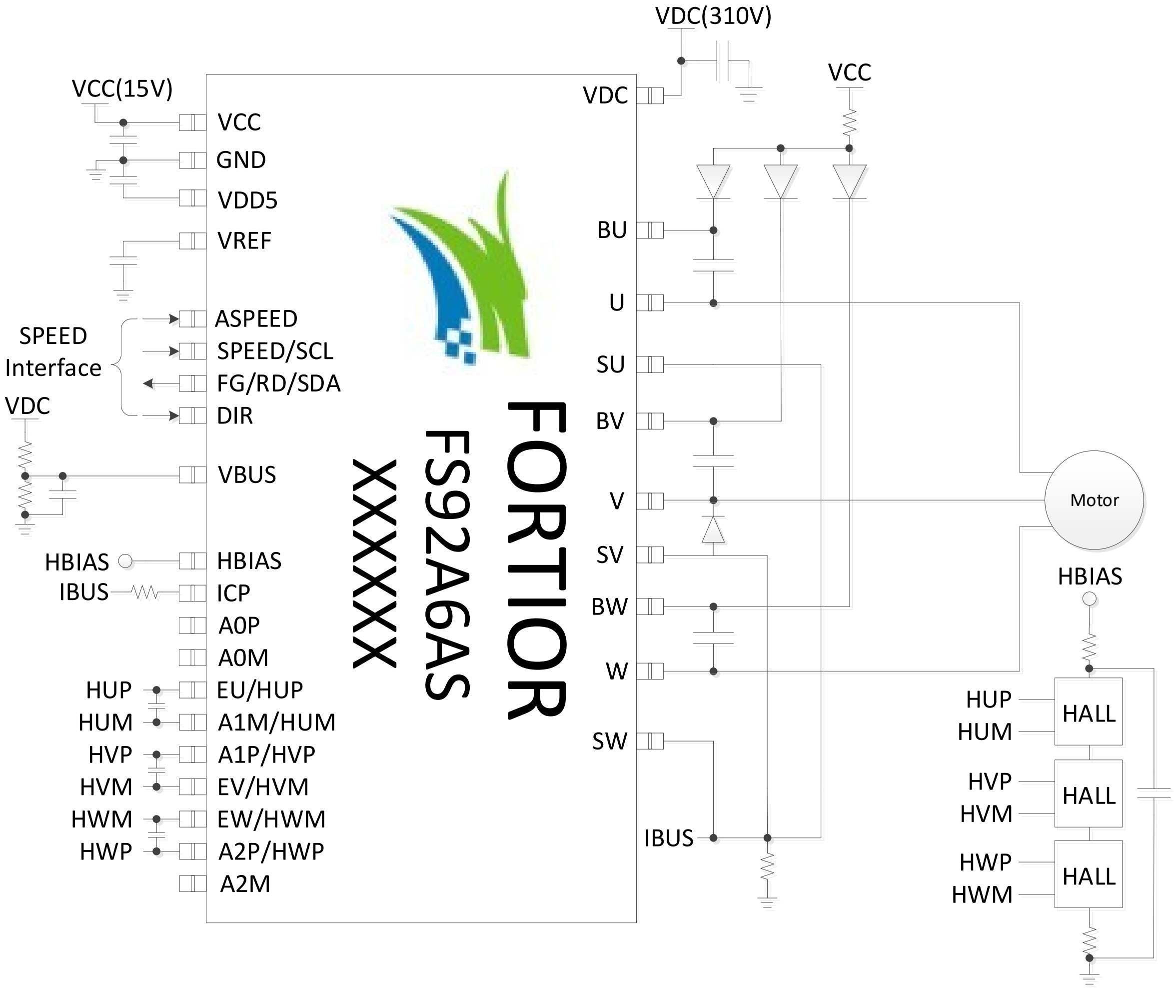


Figure 1-1 Sensored (Three Hall-based Sensors) Differential Input Mode

1.5.2 Sensored (Hall-based Sensor) FOC Mode with Dual-shunt Differential Sampling

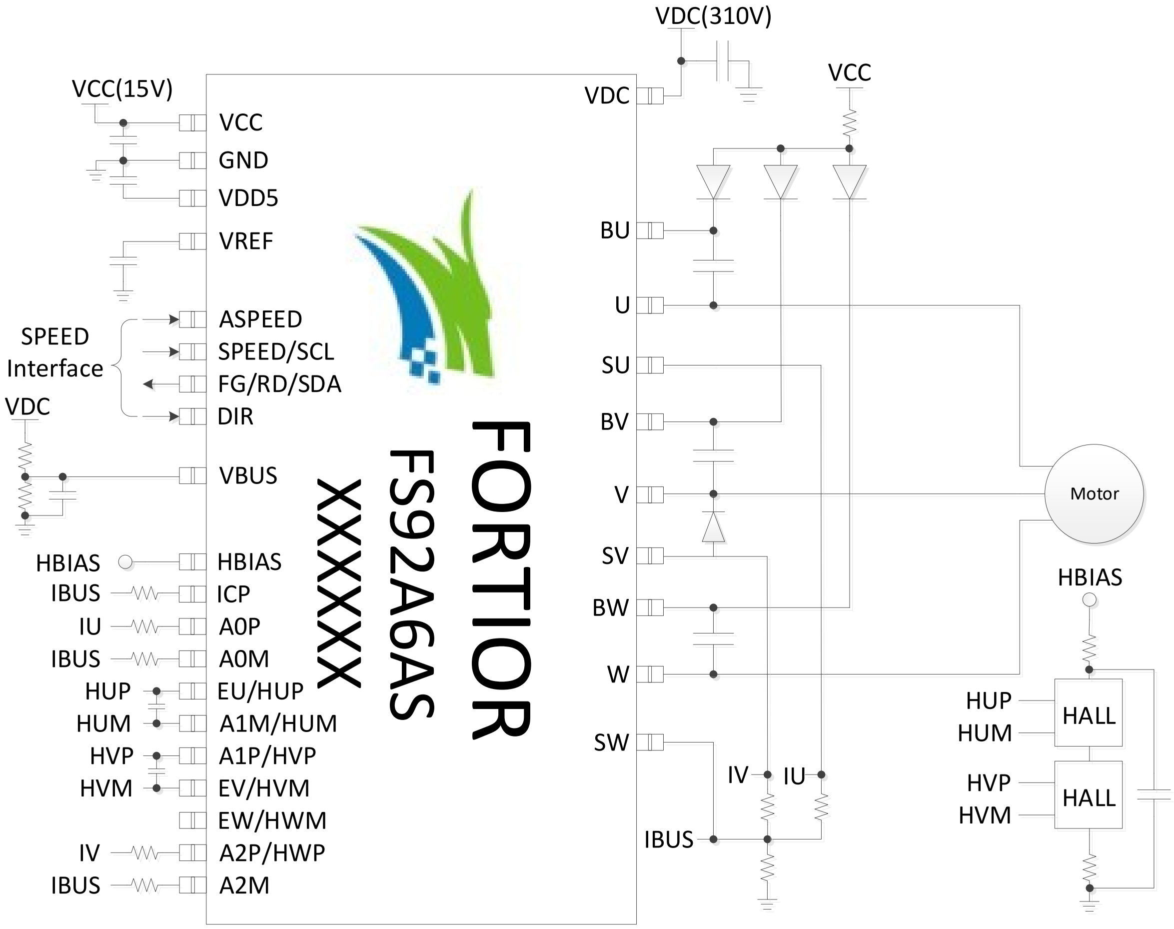


Figure 1-2 Sensored (Hall-based Sensor) FOC Mode with Dual-shunt Differential Sampling

1.5.3 Sensorless FOC Mode with Single-shunt Differential Sampling

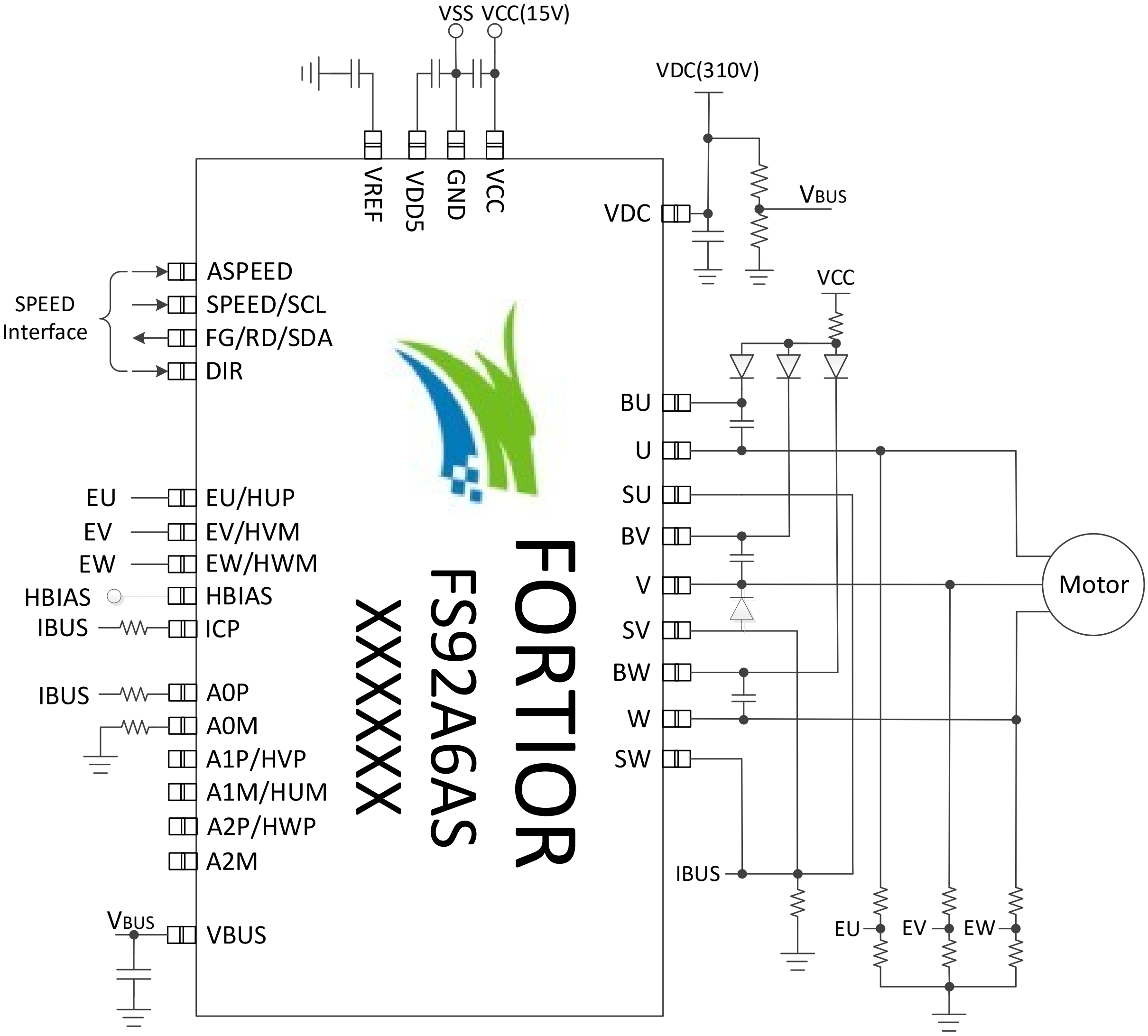


Figure 1-3 Sensorless FOC Mode with Single-shunt Differential Sampling

1.5.4 Sensorless FOC Mode with Dual-shunt Differential Sampling

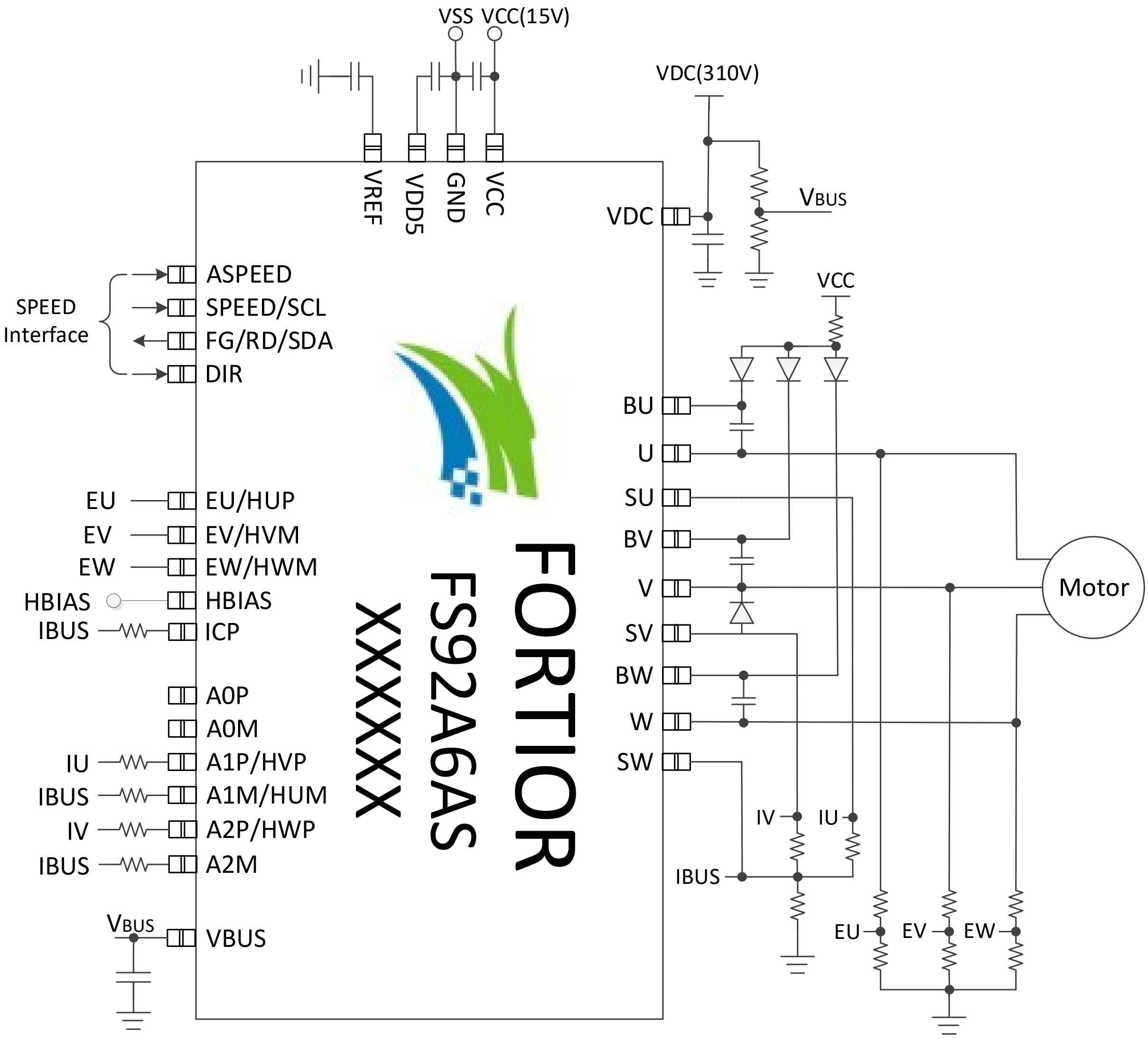


Figure 1-4 Sensorless FOC Mode with Dual-shunt Differential Sampling

1.5.5 Sensorless FOC Mode with Triple-shunt Differential Sampling

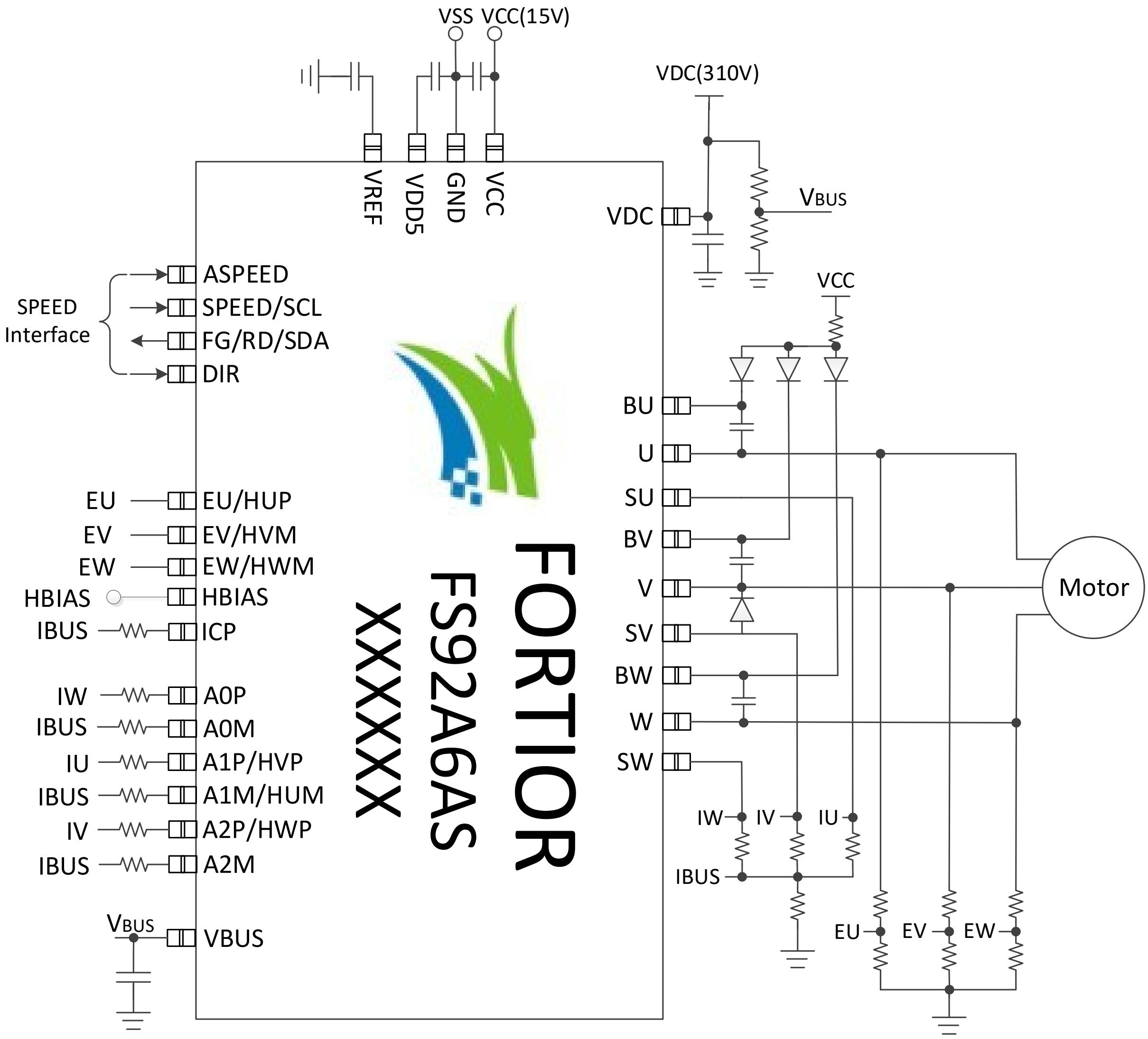


Figure 1-5 Sensorless FOC Mode with Triple-shunt Differential Sampling

1.6 Functional Block Diagram

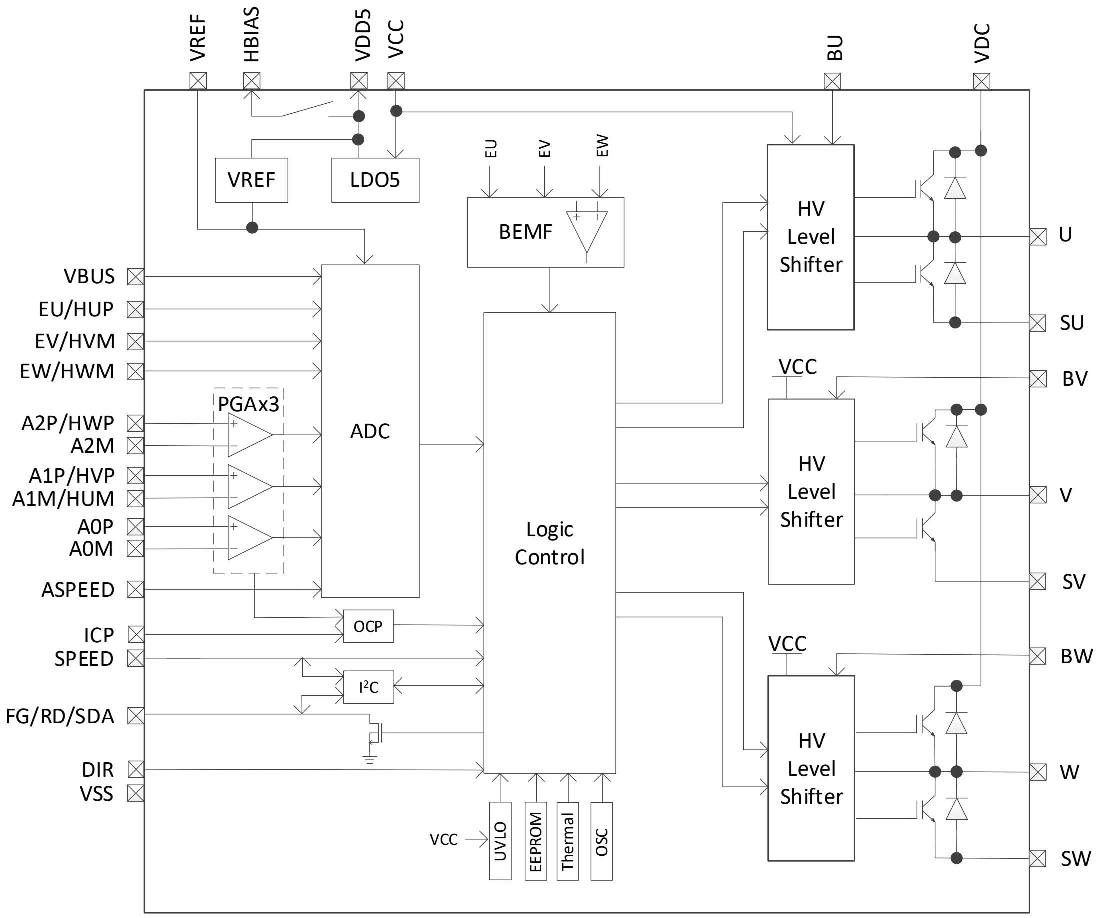


Figure 1-6 Functional Block Diagram of FS92A6AS

1.7 Pinout Diagram

1.7.1 FS92A6AS SSOP A54-38

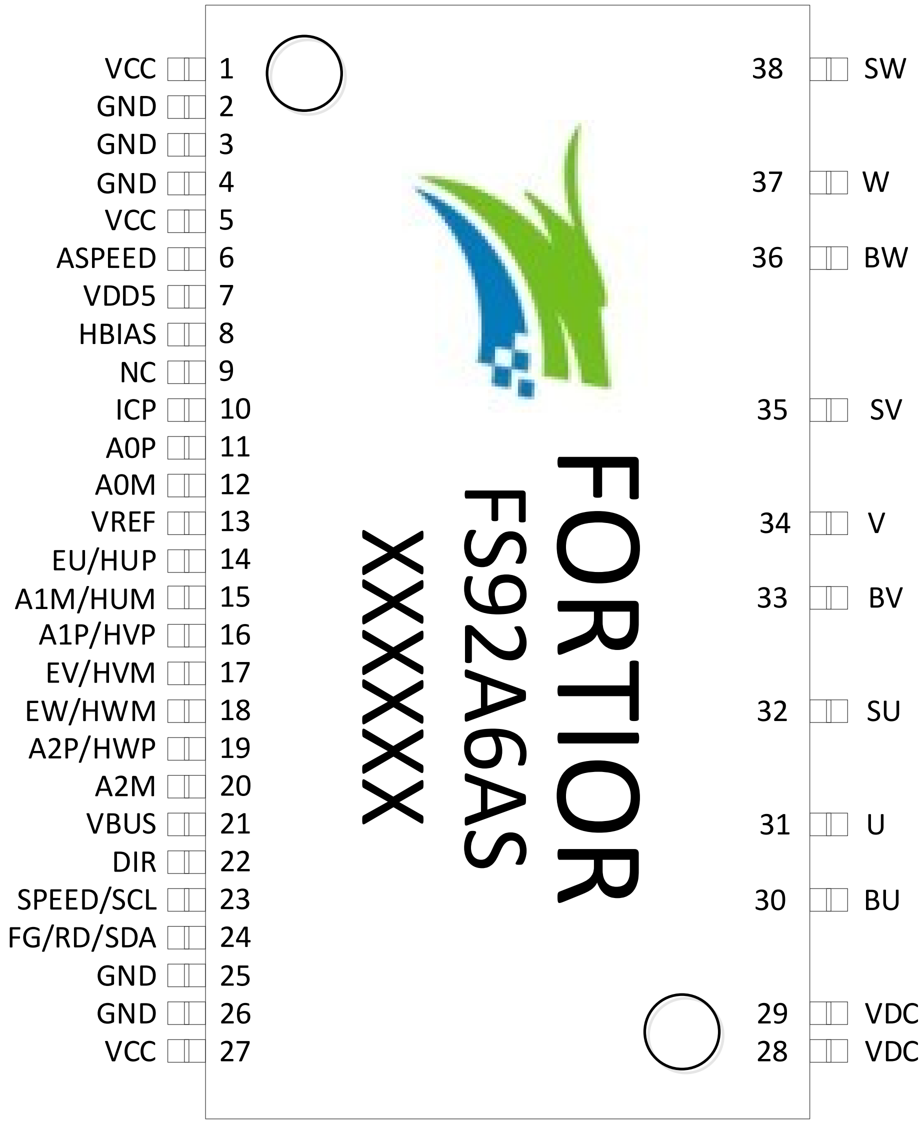


Figure 1-7 FS92A6AS SSOP A54-38 Pinout Diagram

1.8 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DB = Digital Bidirectional
- DO = Digital Output
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

1.8.1 FS92A6AS SSOP A54-38 Pins

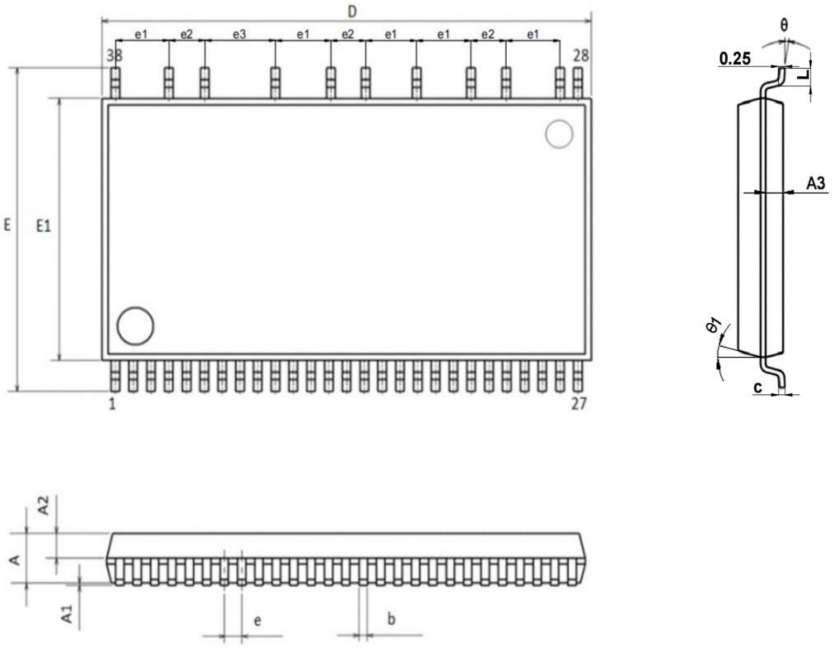
Table 1-1 FS92A6AS SSOP A54-38 Pin Descriptions

Pin	FS92A6AS SSOP A54-38	IO Type	Description
VCC	1	P	Power input
GND	2	P	Ground
GND	3	P	Ground
GND	4	P	Ground
VCC	5	P	Power input
ASPEED	6	AI	Analog voltage input for motor speed regulation
VDD5	7	P	5V LDO output
HBIAS	8	DO	Hall bias power supply, internally connected to VDD5 via a switch
NC	9	-	Not connected
ICP	10	AI	Over-current detection input
A0P	11	AI	AMP0 positive input
A0M	12	AI	AMP0 negative input
VREF	13	AO	ADC reference voltage output, with a 1μF external capacitor connected to ground
EU/ HUP	14	AI/ AI	U-phase BEMF voltage input Differential Hall sensor positive input for U-phase or Hall IC input for U-phase
A1M/ HUM	15	AI/ AI	AMP1 negative input Differential Hall sensor negative input for U-phase
A1P/ HVP	16	AI/ AI	AMP1 positive input Differential Hall sensor positive input for V-phase
EV/ HVM	17	AI/ AI	V-phase BEMF voltage input Differential Hall sensor negative input for V-phase or Hall IC input for V-phase
EW/ HWM	18	AI/ AI	W-phase BEMF voltage input Differential Hall sensor negative input for W-phase or Hall IC input for W-phase
A2P/	19	AI/	AMP2 positive input

Pin	FS92A6AS SSOP A54-38	IO Type	Description
HWP		AI	Differential Hall sensor positive input for W-phase
A2M	20	AI	AMP2 negative input
VBUS	21	AI	VDC bus voltage input after voltage division
DIR	22	DI	Motor rotation control, with built-in pull-up resistor 1: Forward output phase sequence: U --> V --> W. 0: Reverse output phase sequence: U --> W --> V.
SPEED/ SCL	23	DI/ DB	Speed control input; PWM speed regulation I^{2}C SCL
FG/ RD/ SDA	24	DO/ DO/ DB	Speed indication output, configured as collector open-drain output Motor block indication output, configured as collector open-drain output I^{2}C SDA, configured as collector open-drain output
GND	25	P	Ground
GND	26	P	Ground
VCC	27	P	Power input
VDC	28	P	High-voltage power supply
VDC	29	P	High-voltage power supply
BU	30	P	U-phase floating power supply. The voltage floats with respect to phase U.
U	31	DO	U-phase output
SU	32	P	U-phase ground
BV	33	P	V-phase floating power supply. The voltage floats with respect to phase V.
V	34	DO	V-phase output
SV	35	P	V-phase ground
BW	36	P	W-phase floating power supply. The voltage floats with respect to phase W.
W	37	DO	W-phase output
SW	38	P	W-phase ground

2 Package Information

2.1 FS92A6AS SSOP A54-38



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.00	2.10	2.20
A1	0.00	0.10	0.20
A2	0.95	1.05	1.25
A3	0.68	0.78	0.88
b	0.37	0.38	0.39
c	0.17	0.27	0.37
D	21.80	22.00	22.20
E	13.80	14.10	14.40
E1	11.20	11.40	11.60
e	0.80 (BSC)		
e1	2.40 (BSC)		
e2	1.60 (BSC)		
e3	3.20 (BSC)		
L	0.60	0.80	1.00
θ	0°	4°	10°
θ1	10°	11°	12°

Figure 2-1 FS92A6AS SSOP A54-38 Package Drawings and Dimensions

3 Ordering Information

Table 3-1 Model Selections

Model	Power Supply (V)	Saturation Voltage (High Side + Low Side) (V)	Single IGBT Average Drive Current (A)	Control Features						Protection Features									Operating Temperature T_j (℃)	Lead-free	Package
				Drive Type	Speed Regulation			Forward and Reverse Rotation	Initial Position Detection	OCP/CLP	TSD/LTP	Configurable Maximum Speed Protection	VDC OVP/UVP	VCC/ VB UVLO	MLP	Phase Loss Protection	HALLERR Protection				
					I^2C	PWM	Analog Voltage														
FS92A6AS	13 ~ 20	3.46	6	Sensored/Sensorless Sine-wave	√	√	√	√	√	√	√	√	√	√	√	√	√	-40 ~ 150	√	SSOP A54-38

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings[1]

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
IGBT Collector-to-Emitter Voltage V_{CEMAX}		650	-	-	V
Continuous Collector Current $I_{CMAX(DC)}$ of Single IGBT	T_C = 100°C	-	-	6[2]	A
Continuous Collector Current $I_{CMAX(PLUS)}$ of Single IGBT	T_C = 25°C	-	-	12[2][3]	A
Power Dissipation P_d		-	-	3[4]	W
High-side VDC Supply Voltage V_{DC}		-0.3	-	650[2]	V
U/V/W-phase Output Voltage V_U,V_V,V_W		-0.3	-	650[2]	V
High-side Floating Absolute Voltage V_{BU},V_{BV},V_{BW}		-0.3	-	650[2]	V
High-side Floating Supply Voltage V_{BU} - V_U, V_{BV} - V_V, V_{BW} - V_W		-0.3	-	20	V
Storage Temperature Tstg		-55	-	150	℃
VCC to VSS Voltage		-0.3	-	25	V
VDD5 to VSS Voltage		-0.3	5	6.5	V
Other IOs to VSS Voltage (except VCC pins)		-0.3	-	VDD5 + 0.3	V

Notes:

[1] Stress values greater than Table 4-1 listed above may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

[2] Power dissipation shall not exceed P_d or ASO.

[3] Pw ≤ 10μs and duty cycle ≤ 1%.

[4] The power dissipation is 24mW/°C at operating temperature of 25°C or above when the chip is mounted on a 70mm × 70mm × 1.6mm FR4 glass-epoxy circuit board with less than 3% copper foil.

4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

(T_A = 25°C unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage V_{DC}		-	310	400	V
High-side Floating Supply Voltage V_{BU} - V_U, V_{BV} - V_V, V_{BW} - V_W		13.5	15	16.5	V
Low-side Floating Supply Voltage V_{CC}		13.5	15	16.5	V
VREF/VDD5 Bypass Capacitance C_{VREG}		1.0	-	-	μF
Junction Temperature T_j		-	-	+125	°C

Note: All voltages are specified with respect to the corresponding GND pin.

4.3 Global Electrical Characteristics

Table 4-3 Global Electrical Characteristics

(T_A = 25°C and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Driver					
IGBT Output					
IGBT Collector-to-Emitter Breakdown Voltage BV_{CES}	PWM = 0V/ASPEED = 0	650	-	-	V
Collector-to-Emitter Leakage Current I_{CES}	PWM = 0V/ASPEED = 0, Single IGBT	-	-	100	μA
Collector-to-Emitter Saturation Voltage $V_{CE(sat)}$	I_D = 6A	-	1.73	2.2	V
Emitter-to-Collector Fast Recovery Diode Forward Voltage V_{SD}	I_D = 6A	-	1.9	2.4	V
Power Supply					
VB Quiescent Current I_{BBQ}	PWM = 0V/ASPEED = 0, Single IGBT	25	55	100	μA
VB Under-voltage Lockout (UVLO)					
VB UVLO Release Voltage V_{BUVH}	$V_{BX} - V_X$	9.5	10.1	10.7	V
VB UVLO Lockout Voltage V_{BUVL}	$V_{BX} - V_X$	8.5	9.1	9.7	V
Controller					
Power Supply					
VCC Operating Voltage		13	-	20	V
VDD5 Operating Voltage	T_A = -40°C ~ 85°C	4.8	5	5.2	V
VCC Operating Current I_{VCC}	T_A = -40°C ~ 85°C	-	15	25	mA
VDD5 Load Current	T_A = -40°C ~ 85°C	-	-	10	mA
VCC Sleep-mode Current $I_{VCC\text{-}sleep}$	PWM = 0V/ASPEED = 0	-	0.5	1.0	mA
VCC Idling Current I_{Idle}		5	7	10	mA
Voltage Regulator Output Voltage V_{REG}	I_O = -30mA	4.5	5.0	5.5	V
Hall-based Comparator					

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input Bias Current I_{HALL}	V_{IN} = 0V	-2	-	2	µA
Input Common-mode Voltage V_{HALLCM}	V_{IN} = 0V	0	-	VDD5 - 1.5	V
Minimum Input Voltage $V_{HALLMIN}$		50	-	-	mVp-p
Hysteresis Voltage V_{HALLHY}		-	-	=30	mV
Monitor Output – FG					
High-level Output Voltage V_{MONH}	I_O = -2mA	VDD5 – 0.4	-	VDD5	V
Low-level Output Voltage V_{MONL}	I_O = 2mA	0	-	0.4	V
Phase Control					
Minimum Lead Angle P_{MIN}		-	0	-	deg
Maximum Lead Angle P_{MAX}		-	95	-	deg
Carrier Oscillator					
Carrier Frequency F_{OSC}	Signal wave at 20k	18	20	22	kHz
Under-voltage Lockout (UVLO)					
VCC Release Voltage V_{CCUVH}		11.5	12.1	12.7	V
VCC Lockout Voltage V_{CCUVL}		10.5	11.1	11.7	V

4.4 Operational Amplifier Electrical Characteristics

Table 4-4 Operational Amplifier Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operational Amplifier Gain	2x	1.88	2	2.12	-
	4x	3.76	4	4.24	-
	6x	5.64	6	6.36	-
	8x	7.5	8	8.5	-

Note: The operational amplifier gain is measured when both positive and negative inputs of the operational amplifier are connected in series with 1KΩ resistors. The operational amplifier gain varies with external resistors.

4.5 IO Electrical Characteristics (DIR/SPEED/FG)

Table 4-5 IO Electrical Characteristics (DIR/SPEED/FG)

(T_A = 25°C and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Voltage V_{IH}		0.6*VDD5	-	-	V
Low-level Input Voltage V_{IL}		-	-	0.2*VDD5	V
SPEED/DIR Pull-up Resistor		-	33	-	kΩ
SPEED Pull-down Resistor		-	22	-	kΩ
EW/EV/EU Pull-up Resistor		-	5.6	-	kΩ

4.6 Speed Control with Analog Voltage

Table 4-6 Speed Control with Analog Voltage

(T_A = 25°C and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ASPEED Input Voltage		0	-	5	V

4.7 Package Thermal Resistance

Table 4-7 SSOP A54-38 Package Thermal Resistance

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]		42.5	°C/W
Junction-to-package-top Thermal Resistance Ψ_{JT}		12.5	°C/W

Note:

[1] The actual measurements may vary depending on the conditions.

5 Function Description

5.1 VREF

VREF is applied to internal digital logic and analog circuits only, and cannot be used for external circuits. A capacitor of 1μF or above shall be added at VREF pin to stabilize the power supply.

5.2 HBIAS

HBIAS is Hall bias power supply which is internally connected to VDD5 through a configurable switch. In sleep mode, the switch is open to cut off the power supplied to Hall sensors. HBIAS can supply a maximum current of 10mA.

5.3 DIR

Forward or reverse direction control (DIR) pin is used to reverse motor rotation by changing the DIR level. Pull-ups make the pin state as "High" (or "1") by default.

5.4 SPEED

Speed control (SPEED) pin is used to input duty cycle for speed regulation depending on the settings. In addition, SPEED pin serves as the clock line (SCL) for I^2C communication.

5.5 FG/RD/SDA

Speed detection and fault indication (FG/RD/SDA) pin is an open-drain output. When this pin is set to FG, it outputs speed feedback signal to indicate rotation speed of the motor, and when it is set to RD, it outputs high-level signal to indicate the fault state. In addition, the pin serves as the data line (SDA) for I^2C communication.

FG pin can implement FG4 (four pulses output in one mechanical cycle) and FG12 (12 pulses output in one mechanical cycle) as needed, and supports 4-pole-pair output conversion of 5-pole-pair motor.

Example: For a 5-pole-pair motor, 4 or 12 FG signals are displayed in one mechanical cycle.

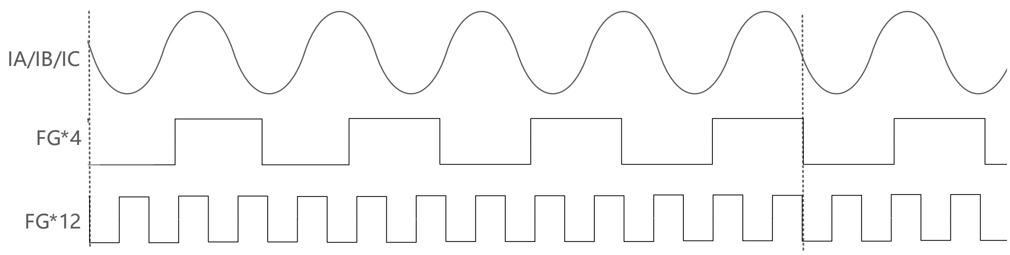


Figure 5-1 FG Output Diagram of 4-pole-pair Output of 5-pole-pair Motor

5.6 Speed Control

5.6.1 Speed Control Modes

The chip supports three types of speed control input interface: PWM, analog voltage and I^2C, and only one of them can be chosen at a time. If analog voltage is selected, voltage value input to the ASPEED pin controls the speed; if PWM is selected, duty cycle of the PWM signal input to the SPEED pin controls the speed; and if I^2C is selected, SPEED pin serves as the clock line (SCL) and FG pin as the data line (SDA).

5.6.2 Speed Control Curve

The control waveform is presented as below, where x-coordinate refers to the duty cycle of PWM input (In I^2C control and analog control modes, the input can be converted to the corresponding PWM duty cycle), and y-coordinate refers to the output duty cycle, which represents different physical quantities in different control modes.

The speed control curve is configured by setting the output duty cycle at the start and end points. The start point is determined by X_ON and Y_ON, and the end point by X_Max and Y_Max. The output of other points between them increases linearly as the input varies.

The y-coordinate represents Duty in voltage-loop control mode; Speed in speed-loop control mode; and Current in current-loop control mode.

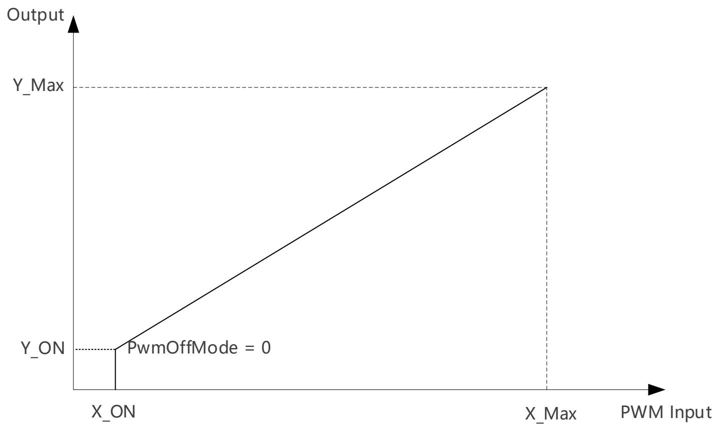


Figure 5-2 Output Curve in Speed-loop or Current-loop Control Mode (PwmOffMode = 0)

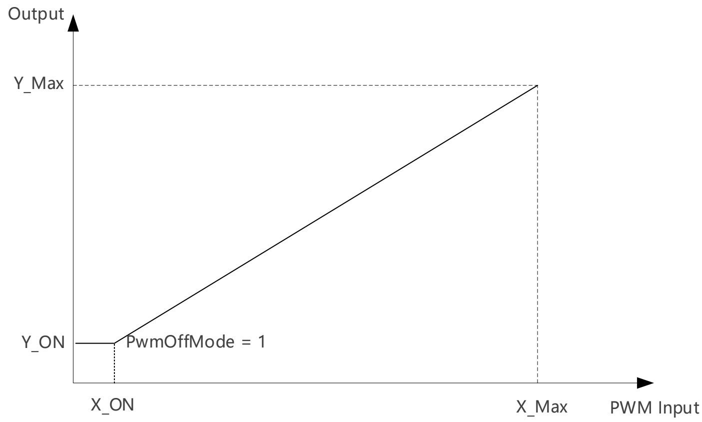


Figure 5-3 Output Curve in Speed-loop or Current-loop Control Mode (PwmOffMode = 1)

5.7 Sleep Mode

The motor enters sleep mode in 6s after ASPEED is set to 0V and SPEED pin is connected to GND.

Wakeup conditions: In I^2C speed control mode, the chip exits sleep mode after receiving the matched I^2C ID. In PWM speed control mode, the chip exits sleep mode when a high-level voltage is input to SPEED pin. In analog voltage control mode, the chip exits sleep mode when the voltage of ASPEED pin is greater than 1.5V or when a high-level voltage is input to SPEED pin.

5.8 Lead Angle Curve

In sensored SVPWM control mode, lead angle curve corresponding to duty cycle of the voltage output is shown in Figure 5-4, where x-coordinate denotes duty cycle of the PWM voltage and y-coordinate represents the lead angle. The multi-stage lead angle curve is developed by setting lead angle at 9 points, which better fits the motor characteristics. Such 9 points are 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, 87.5% and 100% respectively, and the maximum angle difference between each two adjacent points is 10.547°.

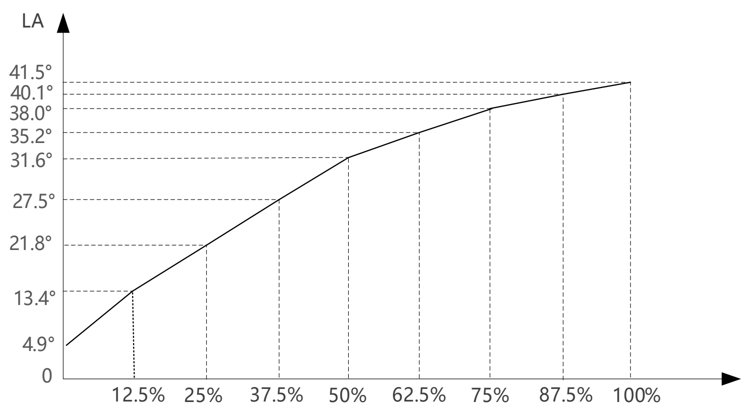


Figure 5-4 Lead Angle Curve

5.9 Soft-on

Soft-on feature gradually increases current during the start-up process, protecting the motor from abrupt startup and reducing noise during operation.

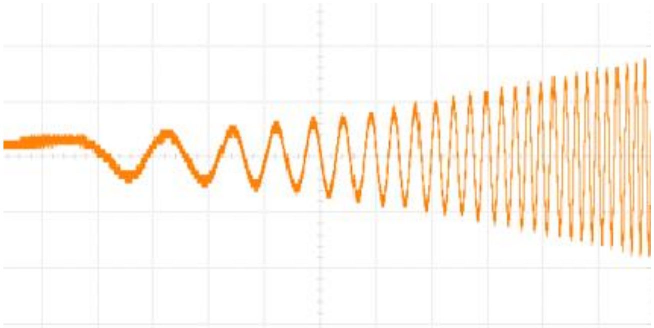


Figure 5-5 Soft-on Phase Current Waveform

5.10 Motor Lock Protection

Motor lock protection circuitry monitors operating state of the motor. When the conditions for motor lock are satisfied, the chip shuts down and waits for 20s to decide whether to restart (depending on software settings).

5.11 Phase Loss Protection

Phase loss protection circuitry monitors operating state of the motor. When the conditions for phase loss are satisfied, the chip shuts down and waits for 20s to decide whether to restart (depending on software settings).

5.12 Current Limiting Protection (CLP)

The chip supports current limiting protection in sensored SVPWM mode, where cycle-by-cycle current limiting can be selected. Cycle-by-cycle current limiting is typically used due to its fast response, but excessive noise is generated. In sensorless FOC and current-loop control mode, the chip limits the maximum output current. In this mode, the noise is basically the same as that in normal operation mode.

5.13 Over-current Protection (OCP)

When the sampling current exceeds the over-current protection threshold, the chip shuts down and waits for 6s to decide whether to restart (depending on software settings).

5.14 Low Temperature Protection (LTP)

The chip is provided with an internal junction thermal sensor. The LTP feature is triggered when the sensor detects junction temperature falls below the temperature threshold. You can also reduce the output torque to keep the temperature within the normal range.

5.15 Temperature Sensor Detect (TSD)

The chip is provided with an internal junction thermal sensor. When the sensor detects junction temperature exceeds the temperature threshold, the chip turns off the outputs until the junction temperature fall within the normal operating level.

5.16 Configurable Maximum Speed Protection

As a means of protection, the maximum running speed can be clamped at a configurable limit.

This is particularly useful as motors may run at a significantly high speed at no-load condition or sensored SVPWM mode. By limiting the running speed, the motor is effectively protected.

5.17 VCC Under-voltage Lockout (UVLO)

The chip turns off outputs and enters the under-voltage lockout state when VCC voltage is lower than VCC UVLO lock voltage and ASPEED voltage is higher than the threshold voltage. The chip detects VCC voltage every 6s and releases the protection state until VCC voltage recovers to the normal operating level.

5.18 VDC Under-voltage/Over-voltage Lockout (UVLO/OVLO)

The chip turns off outputs and enters the under-voltage lockout state or over-voltage protection state when VDC voltage (VDC bus voltage after voltage division) is lower than VDC UVLO lock voltage or higher than VDC OVLO lock voltage and input duty cycle at SPEED pin is greater than the threshold value. It releases the protection state until VDC voltage recovers to the normal operating level.

5.19 HALLERR Protection

The chip enters HALLERR protection state when it detects abnormal Hall input and ASPEED voltage is higher than the threshold voltage. It turns off outputs and waits for 6s to decide whether to restart (depending on software settings).

6 Revision History

Rev.	Description	Date	Prepared By
V0.1	Preliminary datasheet	2024/01/25	Eric Deng
V1.0	Final datasheet 1. Added descriptions on features related to Hall-based sensor; 2. Added descriptions on HALLERR; 3. Updated pinout diagram and some descriptions on pins; 4. Updated chapter 2 Package Information; 5. Modified the minimum value of VB Release Voltage V_{BUVH} from “11.5V” to “9.5V” and VB Lockout Voltage V_{BUVL} from “10.5V” to “8.5V”; 6. Added 4.4 Operational Amplifier Electrical Characteristics.	2024/09/11	Freya Fu
V1.1	1. Updated 2 Package Information; 2. Modified the Typ. of “Hysteresis Voltage V_{HALLHY}” as “-” and modified the Max. as “30mV” in 4.3 Global Electrical Characteristics.	2025/02/20	Freya Fu

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