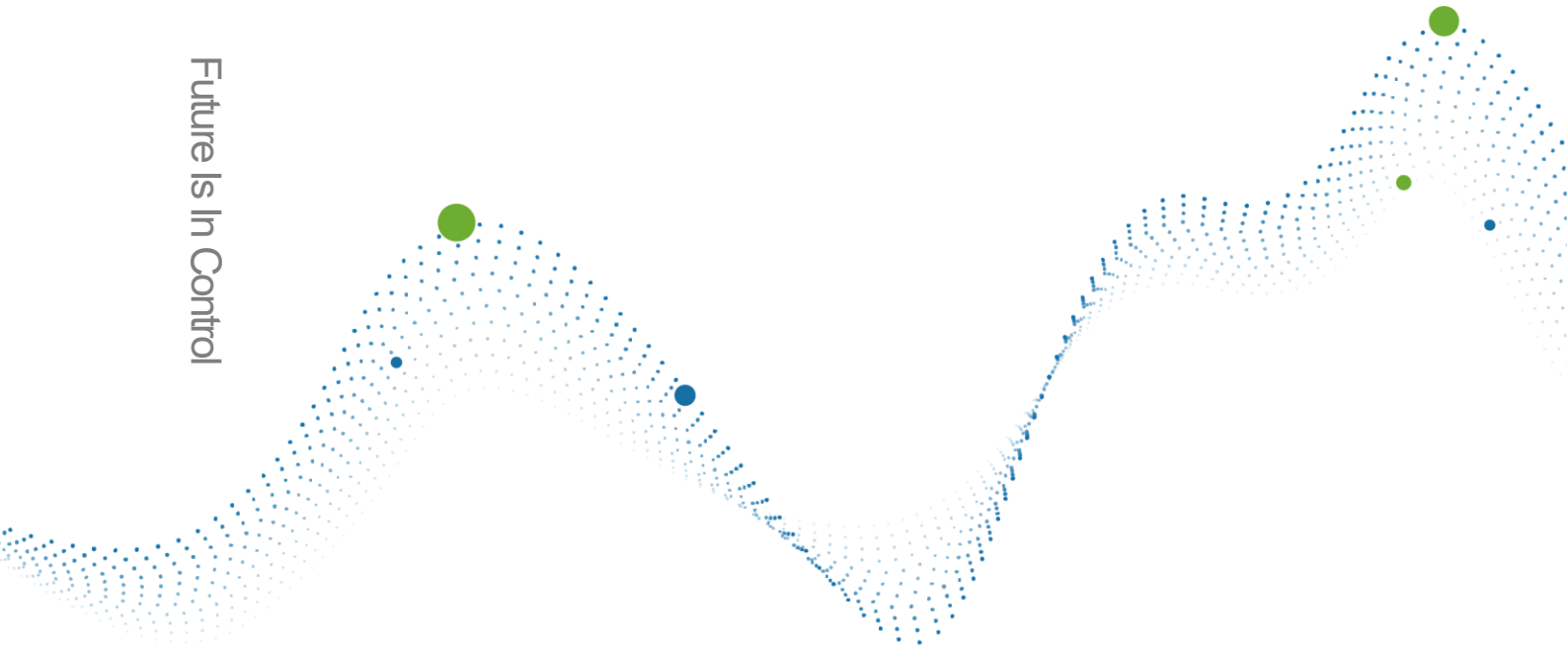
Fortior Tech

Datasheet

FF34061PAS

High-voltage Half-bridge Intelligent Power Module

Future Is In Control



Version No.: V1.0

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Contents

Copyright Notice 1
Disclaimer 2
Contents 3
1 System Introduction 5
1.1 Overview 5
1.2 Applications 5
1.3 Features 5
1.4 Key Parameters 5
1.5 Typical Application Diagram 6
1.6 Functional Block Diagram 7
1.7 FF34061PAS Functional Block Diagram 7
1.8 Pin Definitions 7
1.8.1 FF34061PAS TSOW10 Pins 8
1.8.2 FF34061PAS TSOW10 Pinout Diagram 8
2 Package Information 9
3 Ordering Information 10
4 Electrical Characteristics 11
4.1 Absolute Maximum Ratings 11
4.2 Recommended Operating Conditions 12
4.3 Global Electrical Characteristics 12
4.4 Package Thermal Resistance 13
5 Function Descriptions 14
5.1 Input and Output 14
5.2 Delay Matching Timing Diagram 14
5.3 VCC Under-voltage Lockout (UVLO) 15
5.4 VBS Under-voltage Lockout (UVLO) 15
5.5 Over-current Protection (OCP) 15

5.6 Thermal Shutdown Protection (TSD) 15
5.7 Fault Indication and Shutdown Output 15
5.8 Shoot-through Prevention 15
5.9 Deadtime 16
6 Revision History 17

1 System Introduction

1.1 Overview

FF34061PAS is a high-performance, highly reliable intelligent power module (IPM) integrating a high-voltage half-bridge gate driver with two 340mΩ silicon carbide (SiC) MOSFETs. Designed for low-power motor drive applications—such as range hoods, fans, water pumps, and outdoor fans—it delivers robust and efficient operation in compact systems.

To ensure safe operation, FF34061PAS integrates VCC and VBS undervoltage lockout (UVLO) to prevent insufficient gate drive voltage, along with shoot-through prevention and built-in deadtime to avoid cross-conduction of the high-side and low-side MOSFETs. For system-level protection, it features over-current detection, a fault output indicator, and a shutdown input for external control.

FF34061PAS features over-current detection, and offers fault output and shutdown input for system monitoring and protection.

FF34061PAS is housed in a compact TSOW10 package and is suitable for built-in motor applications and other space-constrained installations.

1.2 Applications

Range hoods, fans, water pumps, outdoor fans, etc.

1.3 Features

- 650V 340mΩ SiC MOSFETs
- High-voltage gate driver circuit
- VCC range: 10V ~ 20V
- Active-high logic, compatible with 3.3V/5V inputs
- VCC/VBS UVLO
- Over-current detection
- Fault output and shutdown input
- Thermal shutdown protection (TSD)
- Shoot-through prevention and deadtime

1.4 Key Parameters

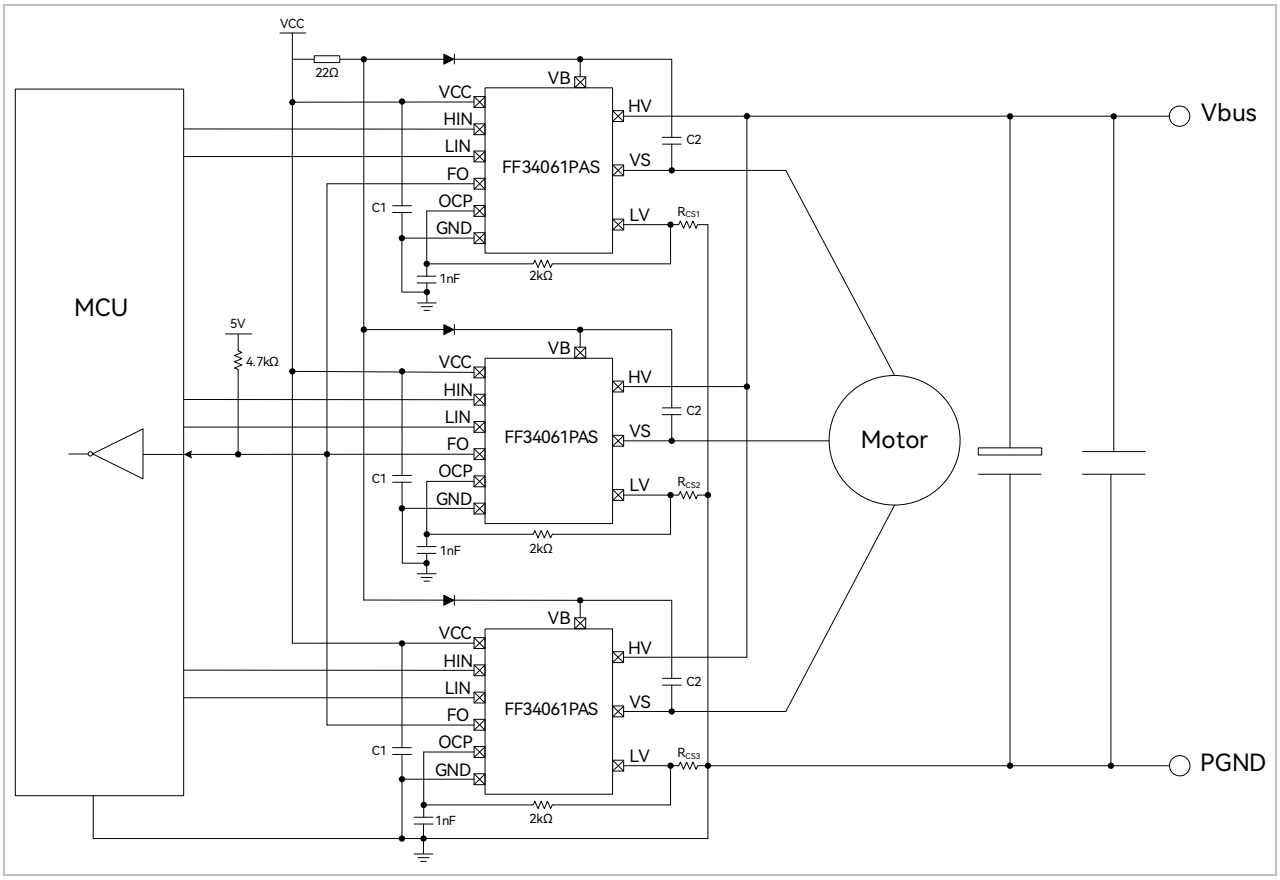
- MOSFET Output Voltage: 650V
- Single MOS Drive Current (DC): ±10A (Max.)
- Single MOS Drive Current (Pulse): ±18A (Max.)
- MOS DC Output Resistance: 340mΩ (Typ.)
- Max. Junction Temperature: +150°C
- Power Dissipation: 5W

Figure 1-1 FF34061PAS



1.5 Typical Application Diagram

Figure 1-2 Typical Application Diagram

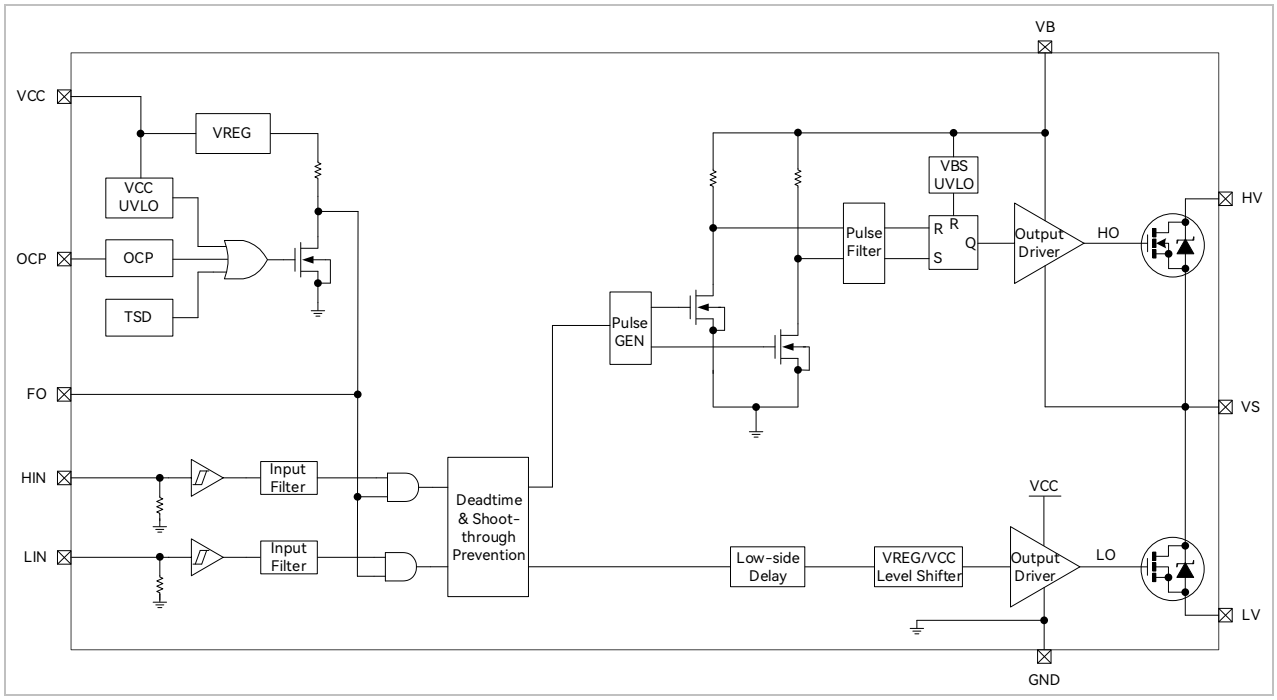


1. A filter capacitor C1 with a capacitance 7 times that of the bootstrap capacitor is recommended for the VCC pin; 10μF is recommended. Place it as close to the chip pin as possible.
2. An 18V Zener diode is recommended for the VCC pin, and it shall be placed as close to the chip pin as possible.
3. Keep input traces as short as possible. An RC filter is recommended at the input to suppress input noise.
4. A high-frequency capacitor above 1μF is preferred for the bootstrap capacitor C2, and it shall be placed as close to the chip pin as possible.
5. A 0.1μF ~ 0.22μF low-frequency filter capacitor is recommended between HV and PGND to prevent surge noise.

1.6 Functional Block Diagram

1.7 FF34061PAS Functional Block Diagram

Figure 1-3 Functional Block Diagram of FF34061PAS



1.8 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- DB = Digital Bidirectional
- AI = Analog Input
- AO = Analog Output
- P = Power Input/Output or Ground

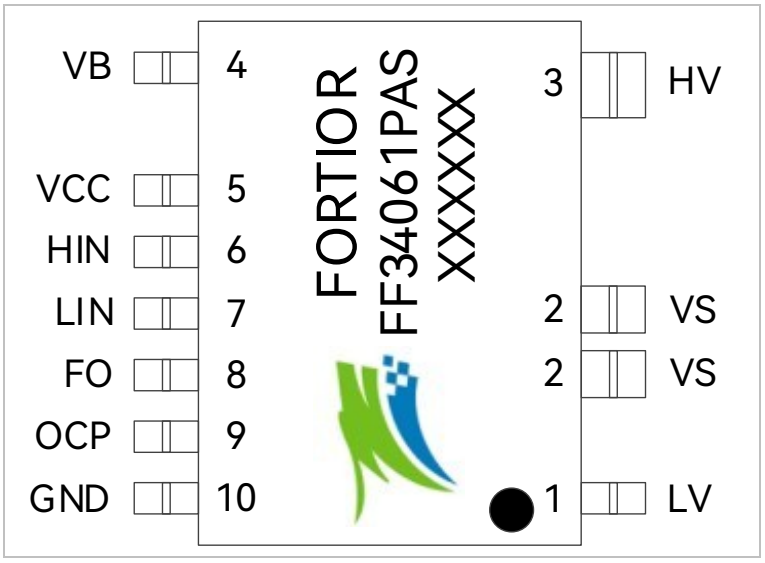
1.8.1 FF34061PAS TSOW10 Pins

Table 1-1 FF34061PAS TSOW10 Pin Descriptions

Pin	FF34061PAS TSOW10	IO Type	Function Descriptions
LV	1	P	Source of low-side MOSFET (negative terminal of high-voltage input)
VS	2	DO	Switching phase output
HV	3	P	Drain of high-side MOSFET (positive terminal of high-voltage input)
VB	4	P	High-side floating absolute voltage
VCC	5	P	Low-side supply voltage
HIN	6	DI	High-side input (positive logic)
LIN	7	DI	Low-side input (positive logic)
FO	8	DB	Fault Output and Shutdown Input
OCP	9	AI	Over-current detection. If this function is not used, this pin shall be shorted to GND
GND	10	P	Ground

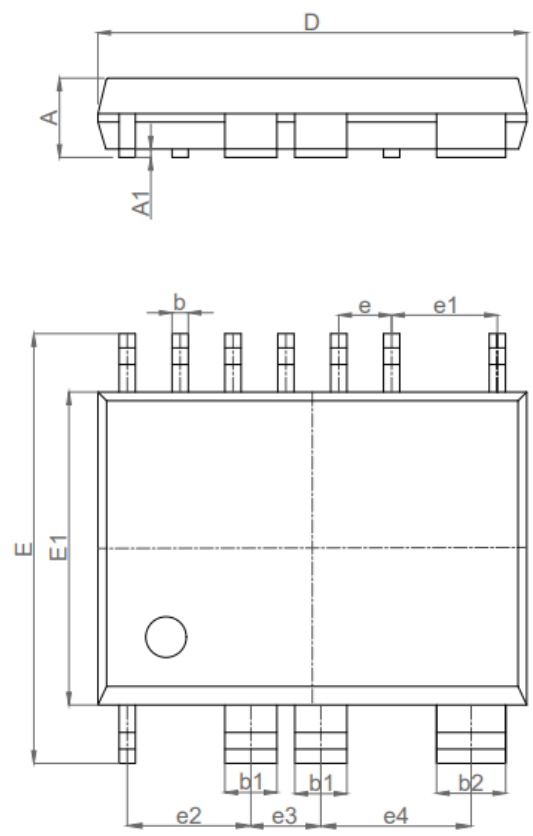
1.8.2 FF34061PAS TSOW10 Pinout Diagram

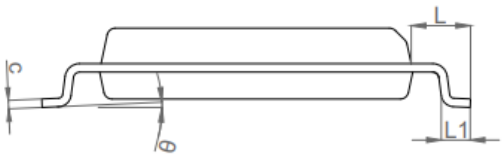
Figure 1-4 FF34061PAS TSOW10 Pinout Diagram



2 Package Information

Figure 2-1 FF34061PAS TSOW10 Package Drawings and Dimensions





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.10
A1	0.10	0.20	0.30
b	0.35	—	0.43
b1	1.21	—	1.29
b2	1.62	—	1.70
c	0.20	—	0.25
D	10.20	10.30	10.40
E	10.00	10.30	10.60
E1	7.40	7.50	7.60
e	1.27BSC		
e1	2.54BSC		
e2	2.97BSC		
e3	1.68BSC		
e4	3.61BSC		
L	—	1.40	—
L1	0.40	0.65	0.90
θ	0	—	8°

3 Ordering Information

Table 3-1 Model Selections

Model	Power Supply (V)	R_{DSON} (High Side + Low Side) (Ω)	Single MOS Continuous Drain Current (A)	Control Features	Protection				Operating Temperature T_J (℃)	Lead-free	Package	Packaging Method	Quantity
				Drive Type	UVLO Protection	Over-current Protection	Thermal Shutdown Protection	Shoot-through prevention					
FF34061PAS	10 ~ 20	0.68	10	N + N	√	√	√	√	-40 ~ 150	√	TSOW10 (10.3x7.5mm)	Tape & Reel	1500

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stress values greater than "Absolute Maximum Ratings" listed in Table 4-1 may permanently damage the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Prolonged exposure to absolute maximum rating conditions may affect device reliability.

Table 4-1 Absolute Maximum Ratings

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Power MOSFET					
MOSFET Drain-to-Source Voltage BV_{DSS}		650	-	-	V
Continuous Drain Current $I_{DMAX(DC)}$ of Single MOS	T_C = 25℃	-	-	10[1]	A
Continuous Drain Current $I_{DMAX(DC)}$ of Single MOS	T_C = 100℃	-	-	8.5[1]	A
Pulsed Drain Current $I_{DMAX(PLS)}$ of Single MOS	T_C = 25℃	-	-	18[1][2]	A
Controller					
High-side Floating Absolute Voltage V_B		-0.3	-	650[1]	V
High-side Floating Offset Voltage V_S		V_B -25	-	V_B + 0.3	V
Low-side Supply Voltage V_{CC}		-0.3	-	25	V
Logic Input Voltage (HIN, LIN) V_{IN}		-0.3	-	6.5	V
FO Input Voltage V_{FO}		-0.3	-	6.5	V
Slew Rate of Offset Voltage dVs/dt		-	≤50	-	V/ns
System					
Storage Temperature T_{STG}		-40	-	150	℃
Junction Temperature T_J[3]		-40	-	150	℃
Power Dissipation P_D		-	-	5[4]	W

Note:

[1] The continuous drain current I_D is limited by the maximum junction temperature determined by P_D and the ASO. Under any circumstances, I_D shall not be chosen such that T_J exceeds T_J (max).

[2] Pw ≤ 10μs and duty cycle ≤ 1%.

[3] The maximum junction temperature T_J for the IPM is 150℃ (@case temperature T_C ≤ 100℃). However, it shall be

limited to $T_{J(av)} \leq 125℃$ (@case temperature $T_C \leq 100℃$) to ensure the IPM operates safely and reliably.

[4] The power dissipation derating factor above 25℃ is 24mW/℃, when the device is mounted on a 70mm × 70mm × 1.6mm FR4 glass-epoxy board with less than 3% copper foil coverage.

4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-side Floating Absolute Voltage V_B		V_s + 10	-	V_s + 20	V
High-side Floating Offset Voltage V_S		-4.5	-	600	V
Low-side Supply Voltage V_{CC}		10	-	20	V
Logic Input Voltage (HIN, LIN) V_{IN}		0	-	5.5	V
Ambient Temperature T_A		-40	-	85	℃

Note:

All voltages are specified with respect to the corresponding GND pin.

4.3 Global Electrical Characteristics

Table 4-3 Global Electrical Characteristics

(T_A = 25℃ and V_{CC} = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
MOSFET Output					
Drain-to-Source Breakdown Voltage BV_{DSS}		650	-	-	V
Drain-to-Source Leakage Current with Gate Shorted to Source I_{DSS}	VDC = 650V, Single MOS	-	0.1	100	μA
Static Drain-to-Source On Resistance $R_{DS(ON)}$	I_D = 5A	-	0.34	-	Ω
	T_J = 150℃, I_D = 5A	-	0.36	-	
Source-to-Drain Diode Forward Voltage V_{FSD}	I_D = 2.5A	-	3.5	-	V
	T_J = 150℃, I_D = 2.5A	-	3	-	
Reverse Recovery Time T_{rr}	I_S = 4A, di/dt = 1.2kA/μs	-	9.2	-	ns
Power Supply Current					
V_{CC} Quiescent Current I_{QCC}	HIN = 0V, LIN = 5V	135	190	220	μA
V_{BS} Quiescent Current I_{QBS}	HIN = 5V, LIN = 0V	25	38	50	μA
HIN/LIN Input					
HIN/LIN High-level Input Voltage V_{IH}		2.7	-	-	V
HIN/LIN Low-level Input Voltage V_{IL}		-	-	0.9	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Bias Current I_{IN+}	V_{IN} = 5V	17	25	36	μA
Low-level Input Bias Current I_{IN-}	V_{IN} = 0V	-	0	1	μA
Under-voltage Lockout (UVLO)					
V_{CC} UVLO Release Voltage V_{CCUV+}		8.3	8.8	9.8	V
V_{CC} UVLO Threshold Voltage V_{CCUV-}		7.5	7.9	8.8	V
V_{CC} UVLO Hysteresis Voltage V_{CCUVH}		0.8	0.9	1.0	V
V_{BS} UVLO Release Voltage V_{BSUV+}		6.3	8.0	9.5	V
V_{BS} UVLO Threshold Voltage V_{BSUV-}		5.5	7.0	8.4	V
V_{BS} UVLO Hysteresis Voltage V_{BSUVH}		0.7	1.0	1.2	V
Over-current Protection (OCP)					
OCP Threshold Voltage V_{OCP}		0.40	0.44	0.48	V
OCP Hold Time T_{HOLD}		-	87	120	μs
OCP Input Filter Time T_{OCP_FLT}		-	0.9	-	μs
Thermal Shutdown Protection (TSD)					
TSD Threshold Temperature T_{TSD}		115	125	135	℃
TSD Hysteresis Temperature T_{TSD_HYS}		-	20	-	℃
FO Fault Output and Shutdown Input					
FO Fault Output Voltage V_{FO}	V_{OCP} = 1V, I_{FO} = 5mA	-	0.28	0.64	V
FO Floating Voltage V_{FO_Float}		-	4.9	-	V
FO Turn-on Threshold Voltage V_{FO_ON}		3	-	-	V
FO Turn-off Threshold Voltage V_{FO_OFF}		-	-	0.9	V
FO Internal Pull-up Resistor R_{FO_PU}		500	590	860	kΩ
Time Parameters					
High-low Side Delay Matching MT		-	-	50	ns
Deadtime DT		-	200	-	ns

4.4 Package Thermal Resistance

Table 4-4 Package Thermal Resistance

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 1S0P PCB	28.1	°C/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 1S0P PCB	10.0	°C/W

Note:

[1] The actual measurements may vary depending on the conditions.

5 Function Descriptions

5.1 Input and Output

Figure 5-1 Input and Output

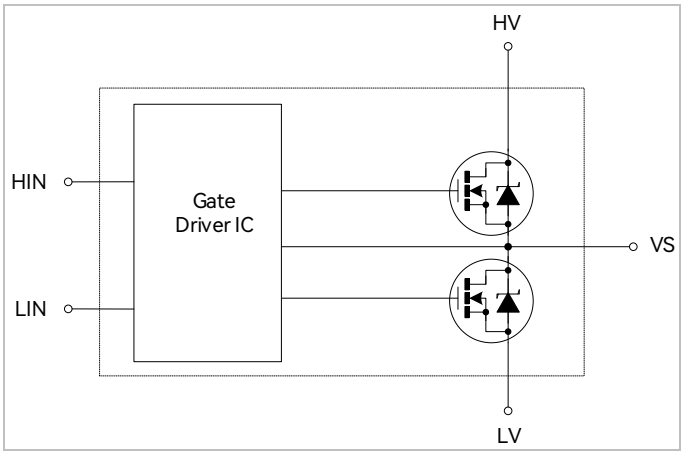


Table 5-1 HIN/LIN to VS Relation

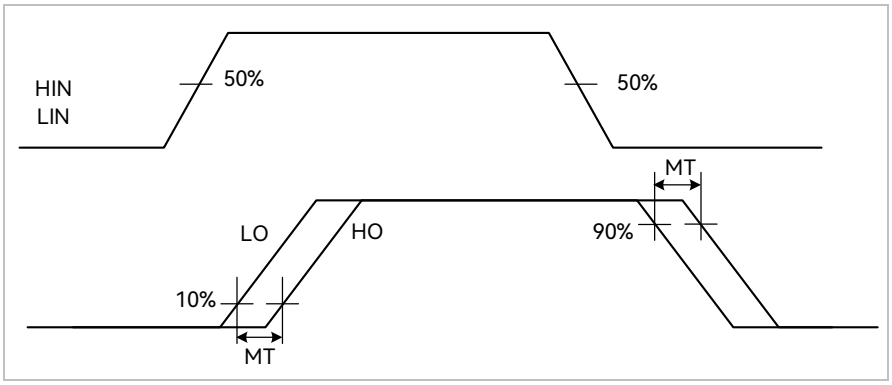
HIN	LIN	VS Voltage
High Level	Low Level	HV
Low Level	High Level	LV
Low Level	Low Level	High Impedance
High Level	High Level	High Impedance[1]

Note:

[1] Shoot-through prevention state

5.2 Delay Matching Timing Diagram

Figure 5-2 Delay Matching Timing Diagram



5.3 VCC Under-voltage Lockout (UVLO)

If VCC voltage falls below VCC UVLO threshold voltage (V_{CCUV-}), the chip enters an under-voltage protection state and disables its output. When the VCC voltage rises above VCC UVLO release voltage (V_{CCUV+}), the chip resumes normal operation.

5.4 VBS Under-voltage Lockout (UVLO)

If the voltage between VB and VS pins falls below VBS UVLO threshold voltage (V_{BSUV-}), the chip enters an under-voltage protection state and disables its output. When the voltage between VB and VS pins rises above VBS UVLO release voltage (V_{BSUV+}), the chip resumes normal operation.

5.5 Over-current Protection (OCP)

The OCP pin detects the voltage across the current sensing resistor. When the OCP pin voltage exceeds V_{OCP}, the chip triggers over-current protection, disables the output and pulls the FO pin low for approximately 87μs. If this function is not used, the OCP pin shall be shorted to GND.

5.6 Thermal Shutdown Protection (TSD)

The chip automatically turns off the output when its junction temperature rises above the TSD threshold temperature (T_{TSD}), and will resume operation after the temperature drops 20°C below T_{TSD}.

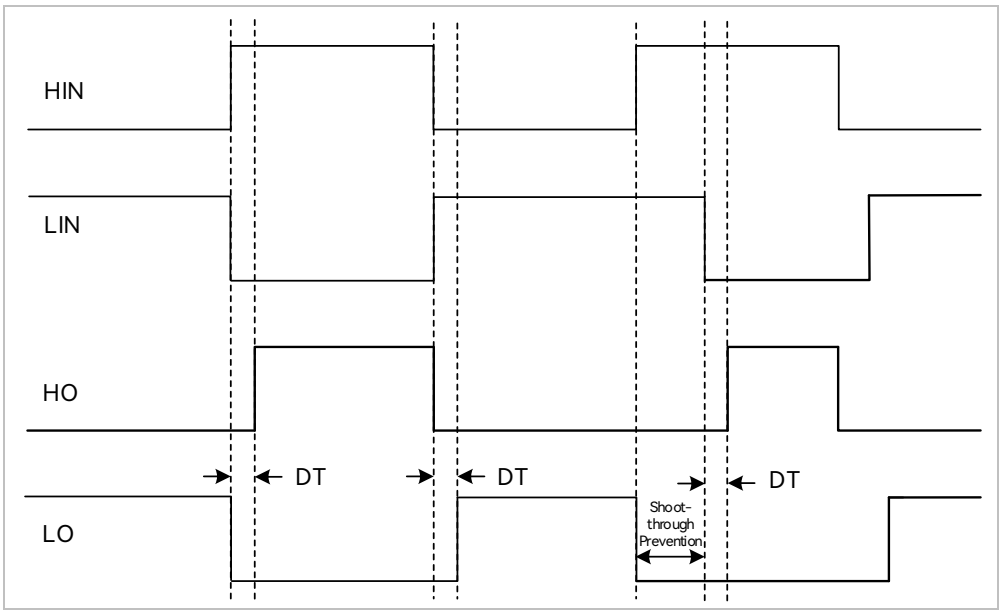
5.7 Fault Indication and Shutdown Output

When the chip enters a fault state (for example, when VCC UVLO, TSD, OCP is triggered), the FO pin outputs a low level and the chip output is disabled.

5.8 Shoot-through Prevention

The chip integrates a shoot-through prevention circuit to effectively prevent cross-conduction of the power switches when high-side and low-side input signals are disturbed. The figure below shows how the protection circuit works.

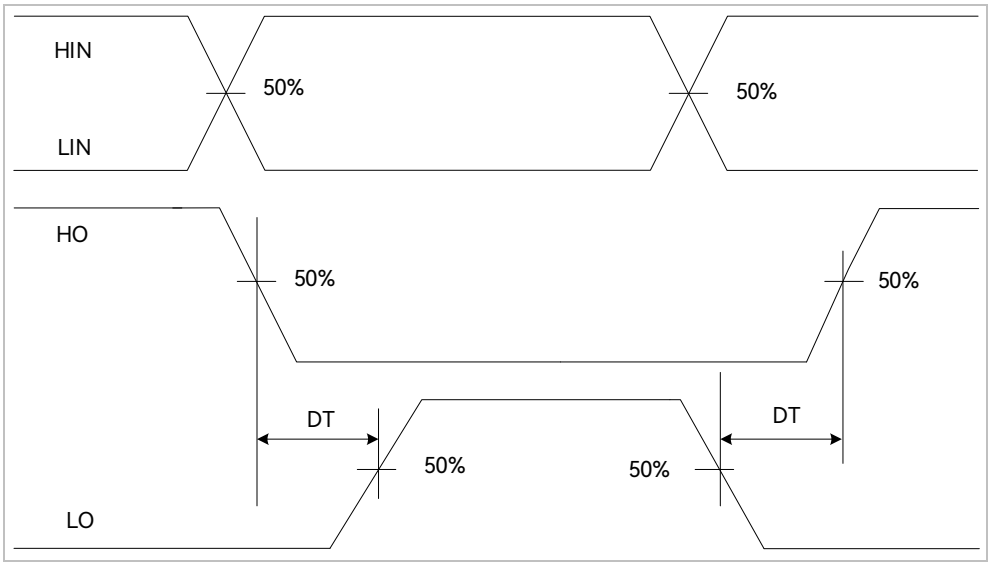
Figure 5-3 Shoot-through Prevention Diagram



5.9 Deadtime

The chip incorporates a fixed deadtime protection circuit. During the deadtime, both the high-side and low-side outputs are held LOW. The deadtime ensures that one power MOSFET is turned off before the other is turned on, effectively preventing shoot-through between the high-side and low-side power MOSFETs.

Figure 5-4 Deadtime Protection



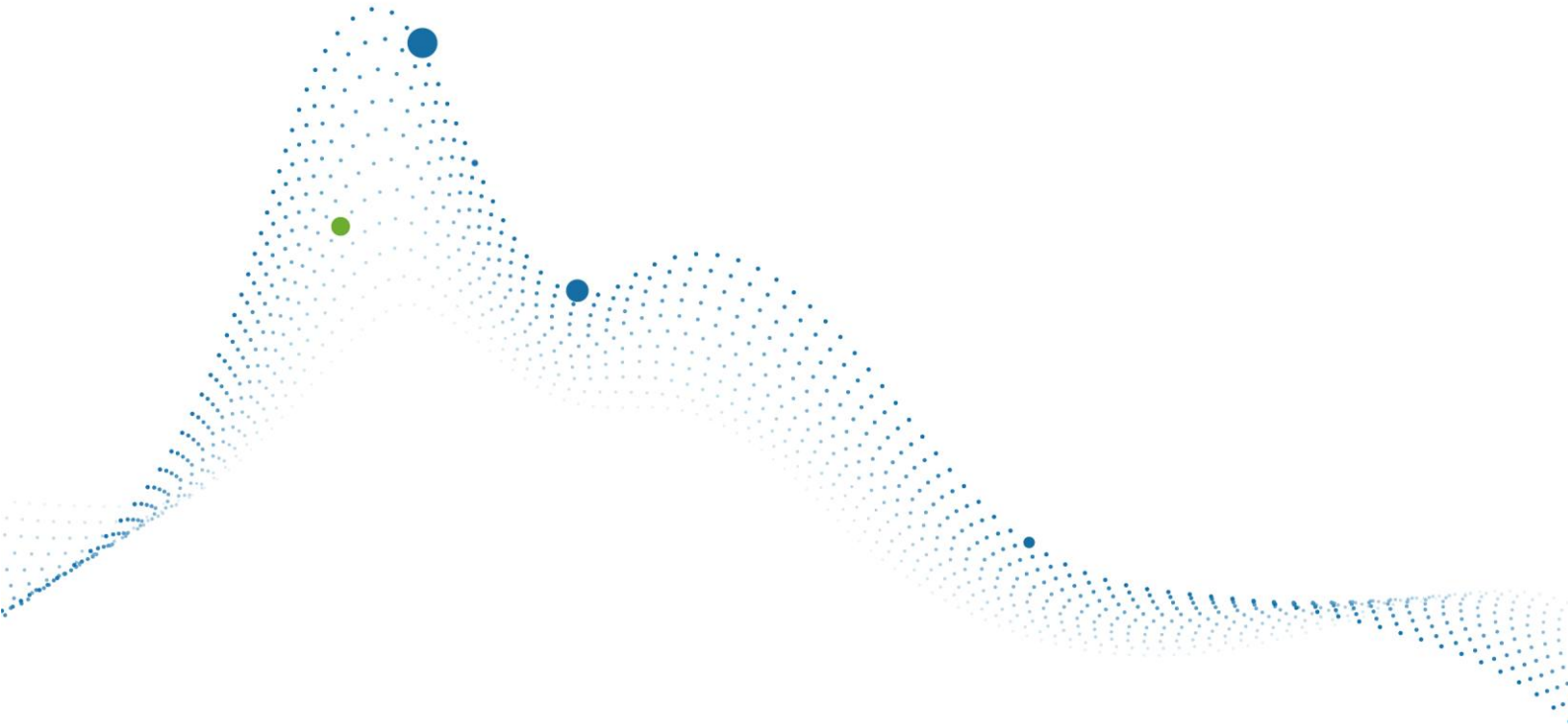
6 Revision History

Rev.	Description	Date	Prepared By
V0.1	Preliminary datasheet	2026/04/09	Eric Deng
V1.0	1. Added product photo; 2. Updated the maximum Continuous Drain Current $I_{DMAX(DC)}$ of Single MOS at T_C = 100℃ from 7.5A to 8.5A, deleted 85 from Continuous Drain Current of Single MOS $I_{DMAX(DC)85,}$ Updated max. value of High-side Floating Absolute Voltage V_B to 650V, modified Note 1 in section 4.1 Absolute Maximum Ratings; 3. Modified Drain-to-Source Leakage Current I_{DSS} to Drain-to-Source Leakage Current with Gate Shorted to Source I_{DSS}, and updated the maximum value of it from 20μA to 100μA; updated the test conditions and typical values of Static Drain-to-Source On Resistance $R_{DS(ON)}$ to I_D = 5A, 0.34Ω, and T_J = 150℃, I_D = 5A, 0.36Ω; updated the test condition for Source-to-Drain Diode Forward Voltage V_{FSD} to I_D = 2.5A and the typical value at T_J = 150℃ to 3V in section 4.3 Global Electrical Characteristics; 4. Modified PGND to LV in Figure 5-1 and Table 5-1.	2026/09/11	Lydia Zhu

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