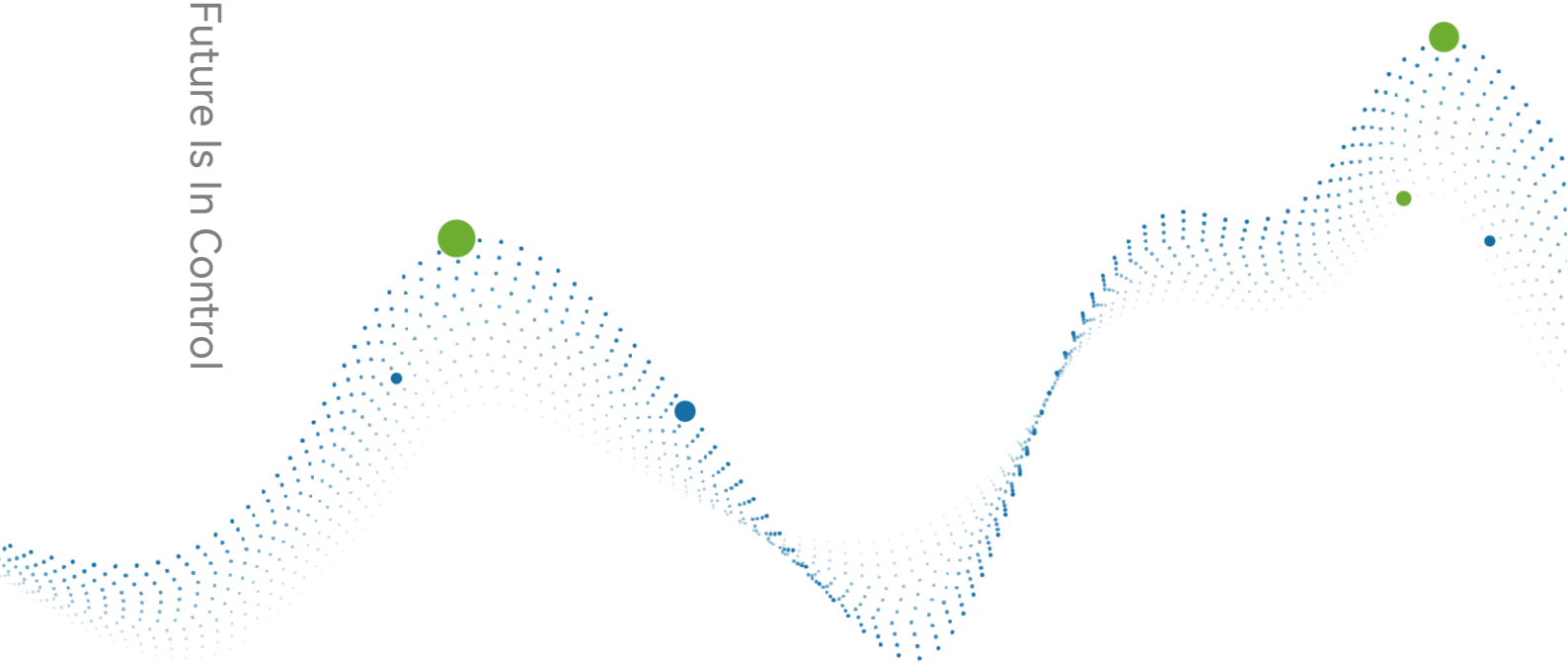
Fortior Tech

DATASHEET

FF50061PAS

High-voltage Half-bridge Intelligent Power Module

Future Is In Control



Version No.: 1.0

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1 System Introduction

1.1 Overview

FF50061PAS is a high-performance, highly reliable high-voltage half-bridge power module integrating two 500m Ω silicon carbide (SiC) MOSFETs and a high-voltage half-bridge gate driver circuit. It is mainly used for low-power motor drive applications such as range hoods, duct fans and industrial fans.

FF50061PAS integrates VCC/VBS under-voltage lockout (UVLO) protection to prevent the power switches from operating at excessively low voltage. It also integrates shoot-through prevention and deadtime to prevent cross-conduction of the high-side and low-side MOSFETs, effectively protecting the power devices.

FF50061PAS supports over-current detection and provides a fault output and shutdown input for system monitoring and protection.

FF50061PAS is housed in a TSOW10 package. Its compact structure makes it suitable for built-in motor applications and other space-constrained installations.

1.2 Applications

Range hoods, duct fans, industrial fans, etc.

1.3 Features

- 650V 500mΩ SiC MOSFET
- Built-in high-voltage gate driver circuit
- VCC range: 10V ~ 20V
- Active-high logic, compatible with 3.3V/5V inputs
- VCC/VBS UVLO
- Over-current detection
- Fault output and shutdown input
- Thermal shutdown protection (TSD)
- Shoot-through prevention and deadtime

1.4 Key Parameters

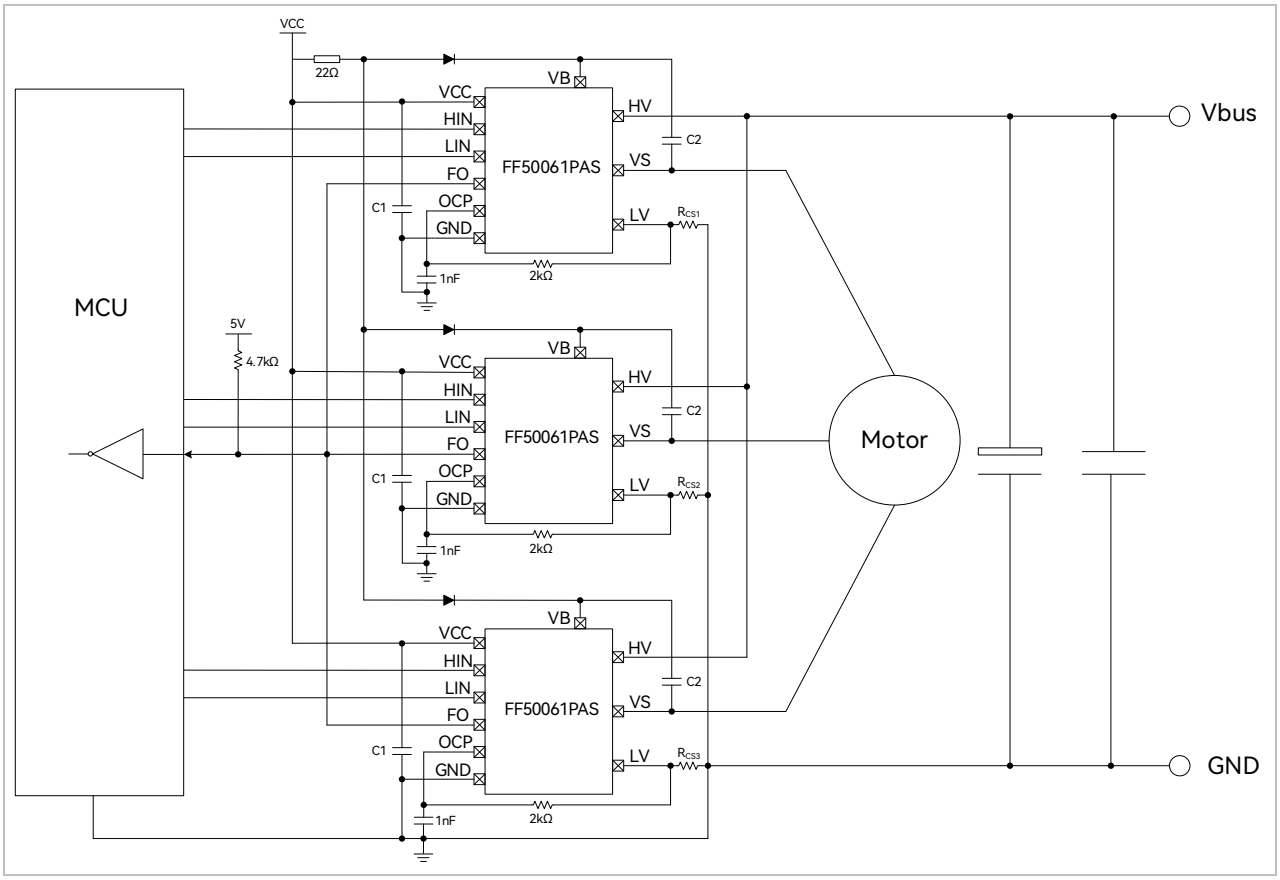
- MOSFET Output Voltage: 650V
- Single MOS Drive Current (DC): ±7A (Max.)
- Single MOS Drive Current (Pulse): ±12A (Max.)
- MOS DC Output Resistance: 500mΩ (Typ.)
- Max. Junction Temperature: +150℃
- Power Dissipation: 5W

Figure 1-1 FF50061PAS



1.5 Typical Application Diagram

Figure 1-2 Typical Application Diagram

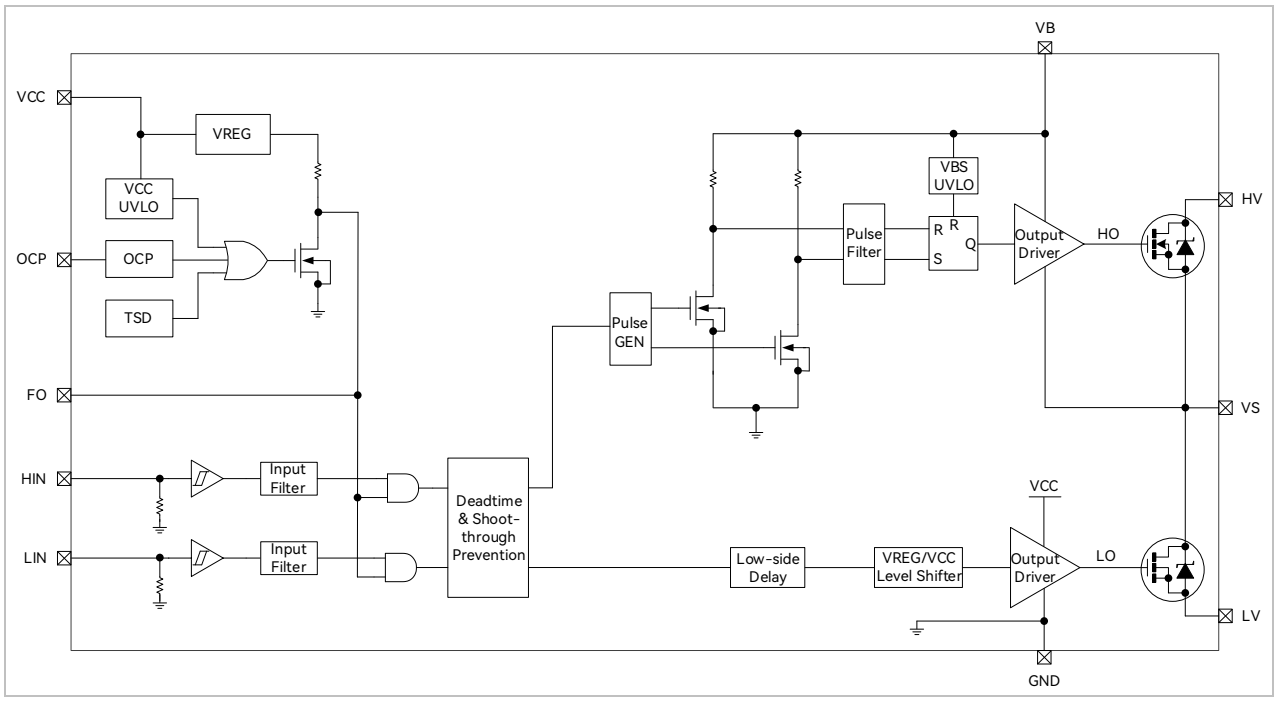


1. A filter capacitor C1 of 7 times the bootstrap capacitance is recommended at VCC; 10μF is suggested. Locate it as close to the chip pin as possible.
2. An 18V Zener diode is recommended for the VCC pin, and it shall be located as close to the chip pin as possible.
3. Keep input traces as short as possible. An RC filter is recommended at the input to suppress input noise.
4. A high-frequency capacitor above 1μF is preferred for the bootstrap capacitor C2, and it shall be placed as close to the chip pin as possible.
5. A 0.1μF ~ 0.22μF low-frequency filter capacitor is recommended between HV and GND to prevent surge noise.

1.6 Functional Block Diagram

1.6.1 FF50061PAS Functional Block Diagram

Figure 1-3 Functional Block Diagram of FF50061PAS



1.7 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- DB = Digital Bidirectional
- AI = Analog Input
- AO = Analog Output
- P = Power Input/Output or Ground

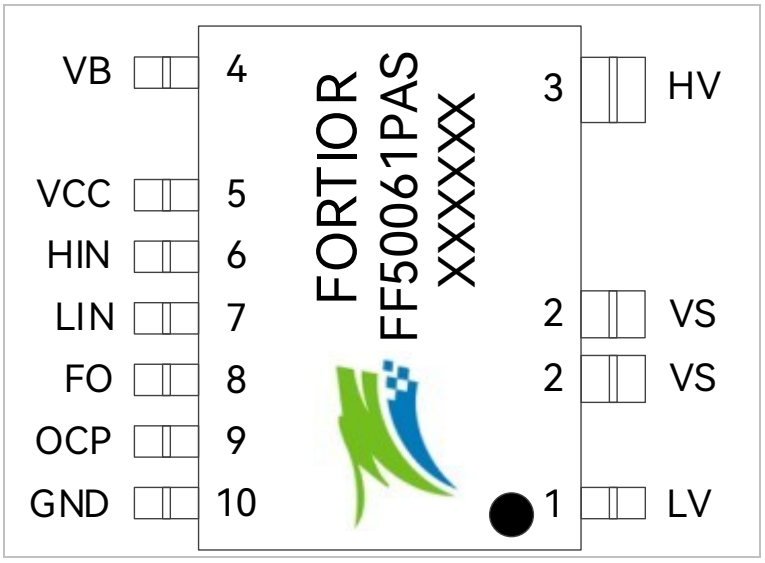
1.7.1 FF50061PAS TSOW10 Pins

Table 1-1 FF50061PAS TSOW10 Pin Descriptions

Pin	FF50061PAS TSOW10	IO Type	Function Descriptions
LV	1	P	Source of low-side MOSFET (negative terminal of high-voltage input)
VS	2	DO	Switching phase output
HV	3	P	Drain of high-side MOSFET (positive terminal of high-voltage input)
VB	4	P	High-side floating absolute voltage
VCC	5	P	Low-side supply voltage
HIN	6	DI	High-side input (positive logic)
LIN	7	DI	Low-side input (positive logic)
FO	8	DB	Fault Output and Shutdown Input
OCP	9	AI	Over-current detection. If this function is not used, this pin shall be shorted to GND
GND	10	P	Ground

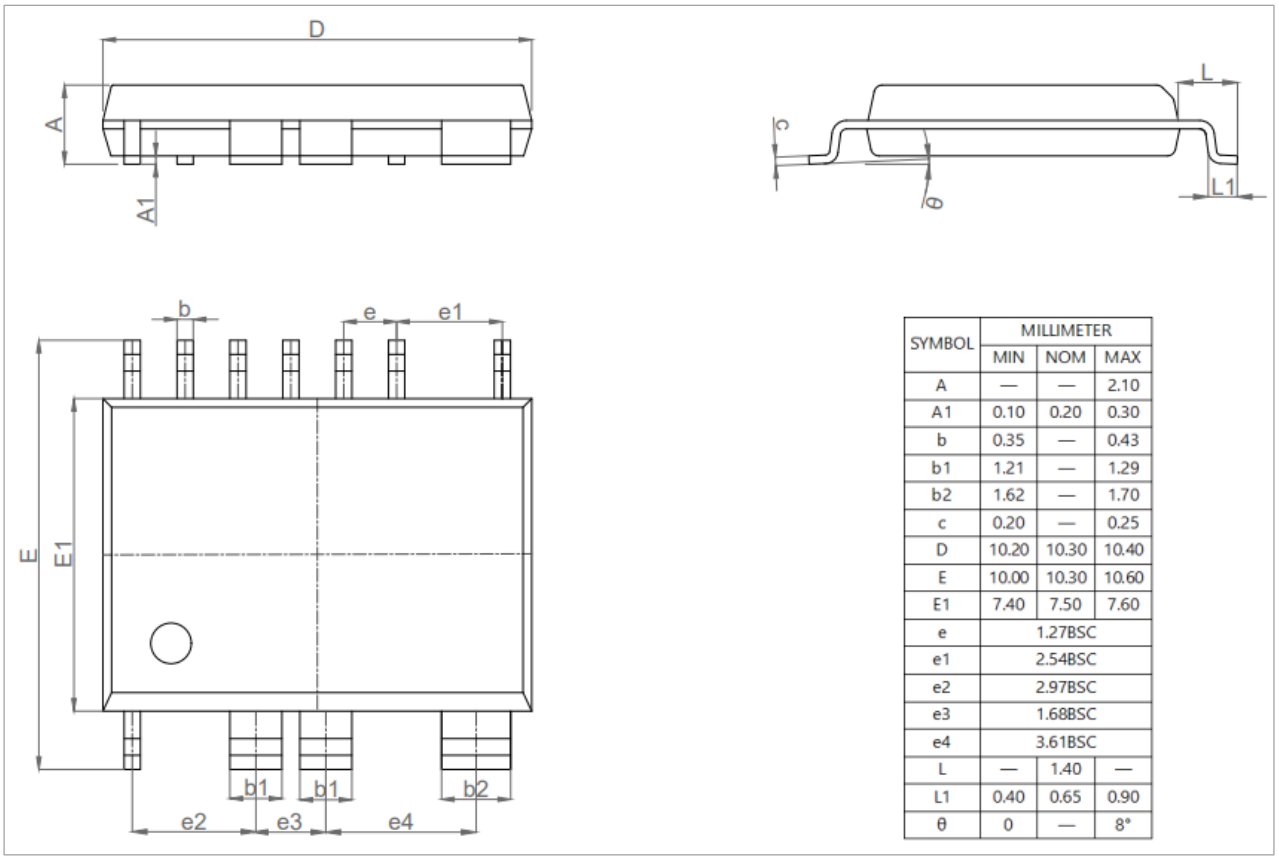
1.7.2 FF50061PAS TSOW10 Pinout Diagram

Figure 1-4 FF50061PAS TSOW10 Pinout Diagram



2 Package Information

Figure 2-1 FF50061PAS TSOW10 Package Outline Drawing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.10
A1	0.10	0.20	0.30
b	0.35	—	0.43
b1	1.21	—	1.29
b2	1.62	—	1.70
c	0.20	—	0.25
D	10.20	10.30	10.40
E	10.00	10.30	10.60
E1	7.40	7.50	7.60
e	1.27BSC		
e1	2.54BSC		
e2	2.97BSC		
e3	1.68BSC		
e4	3.61BSC		
L	—	1.40	—
L1	0.40	0.65	0.90
θ	0	—	8°

3 Ordering Information

Table 3-1 Product Model Selection

Model	Power Supply (V)	R_{DSON} (High Side + Low Side) (Ω)	Single MOS Continuous Drain Current (A)	Control Feature	Protection				Operating Temperature T_J(℃)	Packing Type	Minimum Packing Quantity	Lead -free	Package
				Driver Type	UVLO Protection	OCP Protection	TSD Protection	Shoot-through prevention					
FF50061PAS	10 ~ 20	1	7	N + N	√	√	√	√	-40 ~ 150	Tape & Reel	1500 pcs / Tape	√	TSOW10 (10.3x7.5mm)

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 4-1 Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation outside this range is not recommended. Long-term exposure to absolute maximum conditions may affect device reliability.

Table 4-1 Absolute Maximum Ratings

(T_A = 25℃ and V_{CC} = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Power MOSFET					
MOSFET Drain-to-Source Voltage B_{VDSS}		650	-	-	V
Continuous Drain Current of Single MOS $I_{DMAX(DC)}$	T_C = 25℃	-	-	7[1]	A
Continuous Drain Current of Single MOS $I_{DMAX(DC)}$	T_C = 100℃	-	-	5.7[1]	A
Pulsed Drain Current of Single MOS $I_{DMAX(PLS)}$	T_C = 25℃	-	-	12[1][2]	A
Controller					
High-side Floating Absolute Voltage V_B		-0.3	-	625[1]	V
High-side Floating Offset Voltage V_S		VB -25	-	VB + 0.3	V
Low-side Supply Voltage V_{CC}		-0.3	-	25	V
Logic Input Voltage (HIN, LIN) V_{IN}		-0.3	-	6.5	V
FO Input Voltage V_{FO}		-0.3	-	6.5	V
Slew Rate of Offset Voltage dVs/dt		-	≤50	-	V/ns
System					
Storage Temperature T_{STG}		-40	-	150	℃
Junction Temperature T_J[3]		-40	-	150	℃
Power Dissipation P_D		-	-	5[4]	W

Note:

[1] Do not exceed P_D or ASO.

[2] Pw ≤ 10μs and duty cycle ≤ 1%.

[3] The maximum rated junction temperature of the IPM power chip is 150℃ (@case temperature TC ≤ 100℃). However, to ensure the IPM operates safely, the junction temperature shall be limited to TJ(av) ≤ 125℃ (@case

temperature TC ≤ 100℃).

[4] When mounted on a 70mm X 70mm X 1.6mm FR4 glass-epoxy board with less than 3% copper foil coverage, the power dissipation derating factor above 25℃ is 24mW/℃.

4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

(T_A = 25℃ and V_{CC} = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-side Floating Absolute Voltage V_B		Vs + 10	-	Vs + 20	V
High-side Floating Offset Voltage V_S		-4.5	-	600	V
Low-side Supply Voltage V_{CC}		10	-	20	V
Logic Input Voltage (HIN, LIN) V_{IN}		0	-	5.5	V
Ambient Temperature T_A		-40	-	85	℃

Note:

All voltages are specified with respect to the corresponding GND pin.

4.3 Global Electrical Characteristics

Table 4-3 Global Electrical Characteristics

(T_A = 25℃, V_{CC} = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
MOSFET Output					
Drain-to-Source Breakdown Voltage B_{VDSS}		650	-	-	V
Drain-to-Source Leakage Current with Gate Shorted to Source I_{DSS}	VDC = 650V, Single MOS	-	1	100	μA
Static Drain-to-Source On Resistance $R_{DS(ON)}$	I_D = 4A, T_J = 25℃	-	0.5	0.65	Ω
	I_D = 4A, T_J = 150℃	-	0.59	-	Ω
Source-to-Drain Diode Forward Voltage V_{FSD}	I_D = 2A	-	3.8	-	V
Reverse Recovery Time T_{rr}	I_S = 4A, di/dt = 1.2kA/μs	-	9.2	-	ns
Power Supply Current					
VCC Quiescent Current I_{QCC}	HIN = 0V, LIN = 5V	135	190	220	μA
VBS Quiescent Current I_{QBS}	HIN = 5V, LIN = 0V	25	38	50	μA
HIN/LIN Input					
HIN/LIN High-level Input Voltage V_{IH}		2.7	-	-	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HIN/LIN Low-level Input Voltage V_{IL}		-	-	0.9	V
High-level Input Bias Current I_{IN+}	V_{IN} = 5V	17	25	36	μA
Low-level Input Bias Current I_{IN-}	V_{IN} = 0V	-	0	1	μA
Under-voltage Lockout (UVLO)					
VCC UVLO Exit Voltage V_{CCUV+}		8.3	8.8	9.8	V
VCC UVLO Trigger Voltage V_{CCUV-}		7.5	7.9	8.8	V
VCC UVLO Hysteresis Voltage V_{CCUVH}		0.8	0.9	1.0	V
VBS UVLO Exit Voltage V_{BSUV+}		6.3	8.0	9.5	V
VBS UVLO Trigger Voltage V_{BSUV-}		5.5	7.0	8.4	V
VBS UVLO Hysteresis Voltage V_{BSUVH}		0.7	1.0	1.2	V
Over-current Protection (OCP)					
OCP Threshold Voltage V_{OCP}		0.40	0.44	0.48	V
OCP Hold Time T_{HOLD}		-	87	120	μs
OCP Input Filter Time T_{OCP_FLT}		-	0.9	-	μs
Thermal Shutdown Protection (TSD)					
TSD Threshold Temperature T_{TSD}		115	125	135	℃
TSD Hysteresis Temperature T_{TSD_HYS}		-	20	-	℃
FO Fault Output and Shutdown Input					
FO Fault Output Voltage V_{FO}	V_{OCP} = 1V, I_{FO} = 5mA	-	0.28	0.64	V
FO Floating Voltage V_{FO_Float}		-	4.9	-	V
FO Turn-on Threshold Voltage V_{FO_ON}		3	-	-	V
FO Turn-off Threshold Voltage V_{FO_OFF}		-	-	0.9	V
FO Internal Pull-up Resistor R_{FO_PU}		500	590	860	kΩ
Time Parameters					
High-low Side Delay Matching MT		-	-	50	ns
Deadtime DT		-	200	-	ns

4.4 Package Thermal Resistance

Table 4-4 TSOW10 Package Thermal Resistance

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 1S0P PCB	28.1	C/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 1S0P PCB	10.0	C/W

Note:

[1] The actual measurements may vary depending on the conditions.

5 Function Descriptions

5.1 Input and Output

Figure 5-1 Input and Output

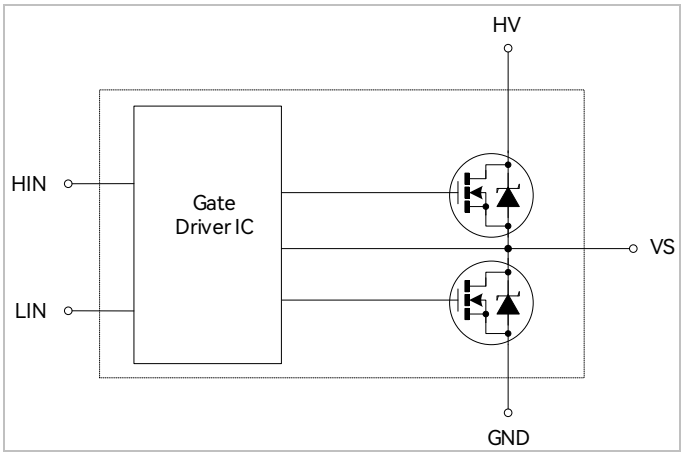


Table 5-1 HIN and LIN vs. VS Voltage Relationship

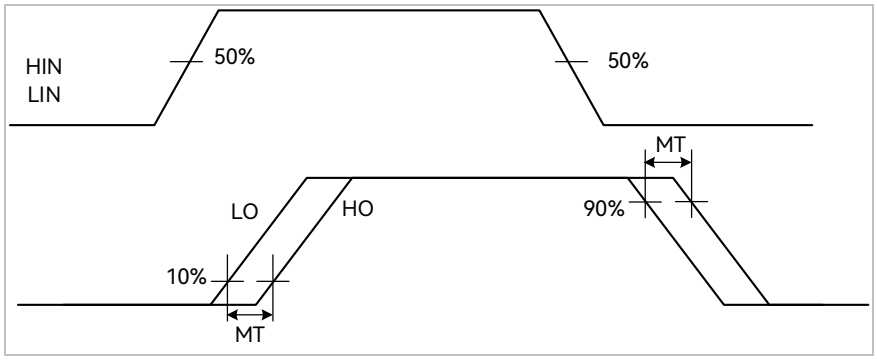
HIN	LIN	VS Voltage
High Level	Low Level	HV
Low Level	High Level	GND
Low Level	Low Level	High Impedance
High Level	High Level	High Impedance[1]

Note:

[1] Shoot-through prevention state

5.2 Delay Matching Timing Diagram

Figure 5-2 Delay Matching Timing Diagram



5.3 VCC Under-voltage Lockout (UVLO)

If VCC voltage falls below VCC UVLO trigger voltage (V_{CCUV-}), the chip enters an under-voltage protection state and disables its output. When the VCC voltage rises above VCC UVLO exit voltage ($_{VCCUV+}$), the chip resumes normal operation.

5.4 VBS Under-voltage Lockout (UVLO)

If the voltage between VB and VS pins falls below VBS UVLO trigger voltage (V_{BSUV-}), the chip enters an under-voltage protection state and disables its output. When the voltage between VB and VS pins rises above VBS UVLO exit voltage (V_{BSUV+}), the chip resumes normal operation.

5.5 Over-current Protection (OCP)

The OCP pin detects the voltage across the current sensing resistor. When the OCP pin voltage exceeds V_{OCP}, the chip triggers over-current protection, disables the output and pulls the FO pin low for approximately 87μs. If this function is not used, the OCP pin shall be shorted to GND.

5.6 Thermal Shutdown Protection (TSD)

The chip automatically turns off the output when its junction temperature rises above the TSD threshold temperature (T_{TSD}), and will resume operation after the temperature drops 20℃ below T_{TSD}.

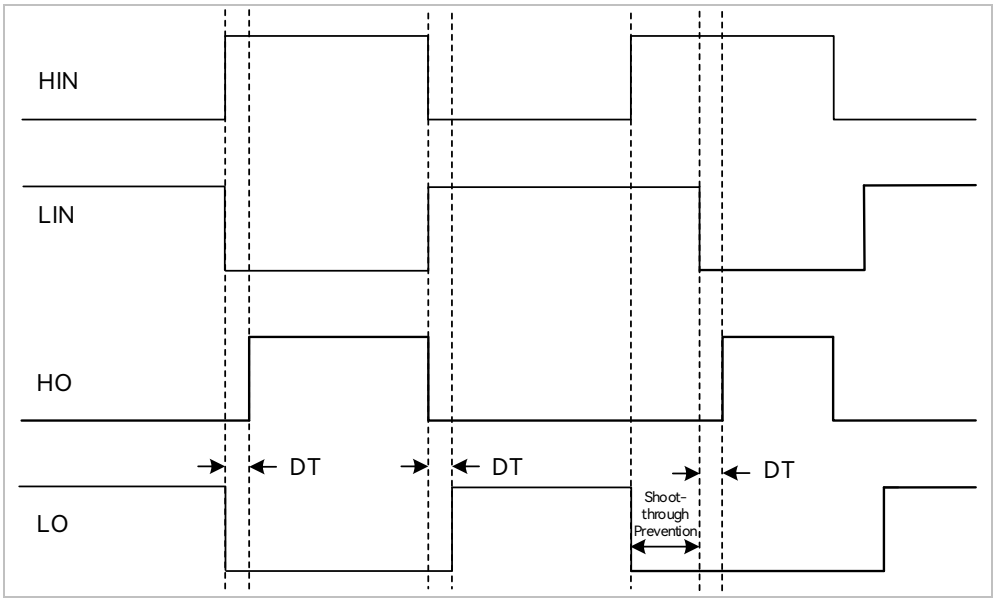
5.7 Fault Indication and Output Shutdown

When the chip enters a fault state (for example, when VCC UVLO, TSD, OCP is triggered), the FO pin outputs a low level and the chip output is disabled.

5.8 Shoot-through Prevention

The chip integrates a shoot-through prevention circuit to effectively prevent cross-conduction of the power switches when high-side and low-side input signals are disturbed. The figure below shows how the protection circuit works.

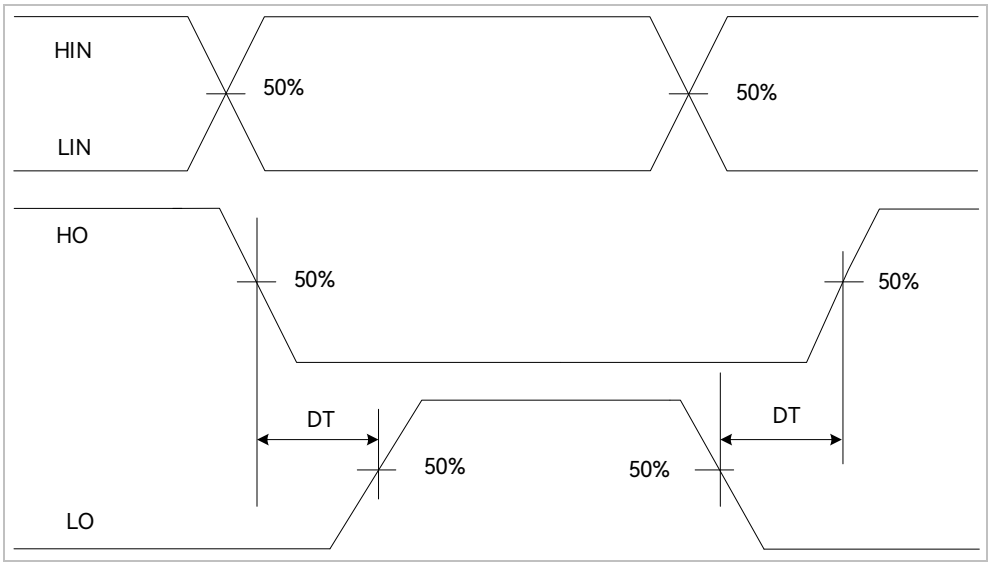
Figure 5-3 Shoot-through Prevention Diagram



5.9 Deadtime

The chip incorporates a fixed deadtime protection circuit. During the deadtime, both the high-side and low-side outputs are held LOW. The deadtime ensures that one power MOSFET is turned off before the other is turned on, effectively preventing shoot-through between the high-side and low-side power MOSFETs.

Figure 5-4 Deadtime Protection



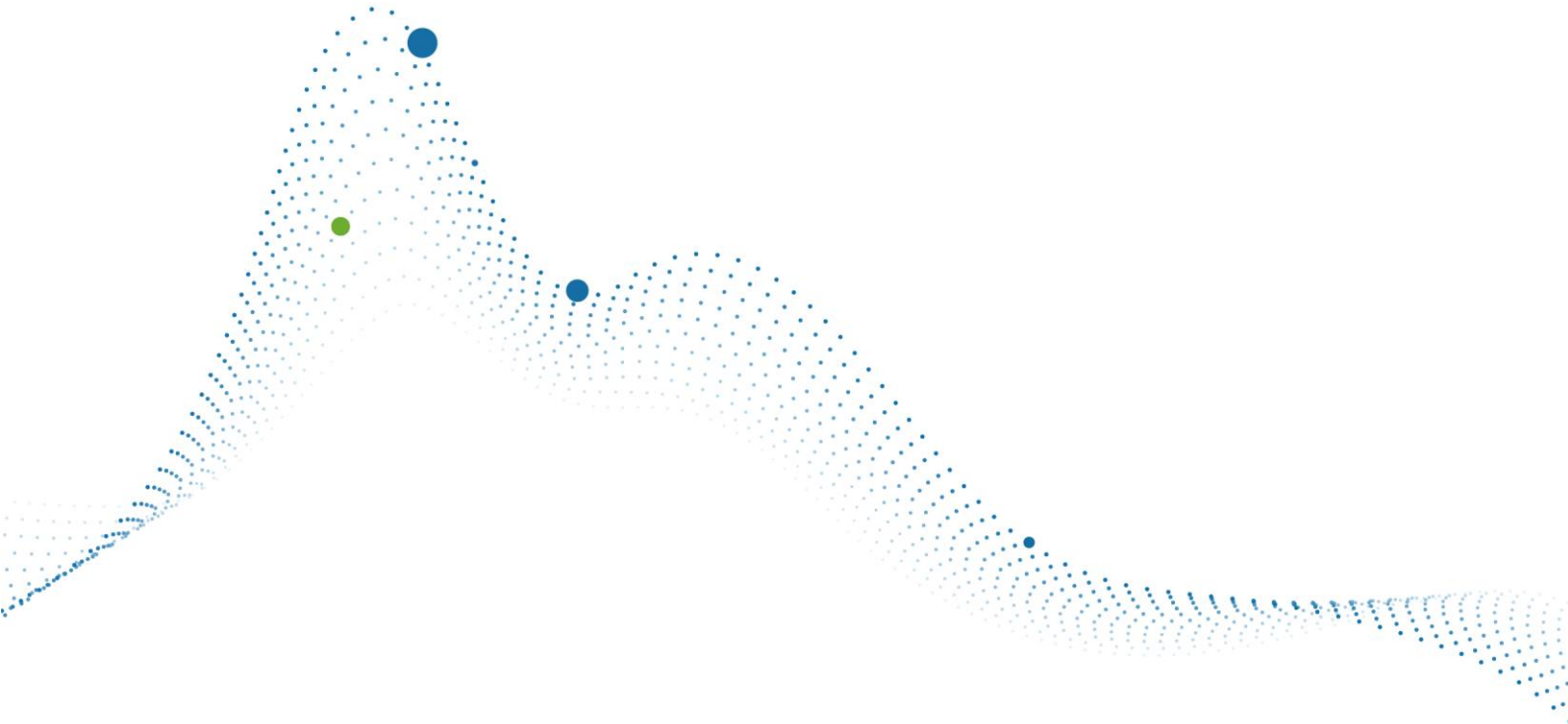
6 Revision History

Rev.	Description	Date	Prepared By
V0.1	Preliminary datasheet	2026/05/09	Eric Deng
V1.0	1. Added a product photo; 2. Added the condition VCC = 15V to Table 4-1 Absolute Maximum Ratings and Table 4-2 Recommended Operating Conditions; 3. Updated the typical value of the Drain-to-Source Leakage Current with Gate Shorted to Source to 1μA and the maximum value to 100μA; removed V_{GS} = 15V from the test conditions of the Static Drain-to-Source On Resistance in 4.3 Global Electrical Characteristics.	2026/10/16	Lydia Zhu

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