Fortior Tech

DATASHEET

Future Is In Control

FU6812x2_61x2_62_72

Three-phase Motor Control MCU

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Contents

Explanation of Symbols

- The symbol "[ ]" following a register indicates a bit in the register. For example, ABCD[XY] indicates the XY bit in ABCD register.
- The symbol "x" in a register name indicates similar registers. For example, TIMx_CR0 indicates TIM3_CR0 and TIM4_CR0.
- [m:n] indicates a range of bits. For example, [3:0] means the bits from bit3 to bit0.
- Pm.n indicates the nth port of the Portm. P0.0 indicates the 0th port of Port0.
- Register read and write symbols:
  - R: Read only
  - W: Write only
  - R/W: Read/write
  - W0: Only 0 can be written
  - W1: Only 1 can be written
- The symbol "-" indicates an uncertainty value or invalid value.
- The RMW instruction cannot be used for registers with different read and written representations.
- Q (number) format is to store floating-point numbers using fixed-point numbers. MSB is the sign bit, followed by integer bits and fraction bits, where lower Q bits are assigned to the fractional part and the remaining bits are assigned to the integer part. For example, for Q12, bit15 is the sign bit, bit14 ~ bit12 represent the integer part and bit11 ~ bit0 represent the fraction part. The Q12 format has a decimal range -8 ~ 7.9998 (corresponding to 0x8000 ~ 0x7FFF).

Abbreviations

ADC	Analog to Digital Convertor
BEMF	Back Electromotive Force
BLDC	Brushless Direct Current
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Convertor
DMA	Direct Memory Access
FG	Frequency Generator
FICE	Fortior Interactive Connectivity Establishment
FOC	Field Oriented Control
FOSC	Fast Oscillator
GPIO	General Purpose Input Output
IC	Integrated Circuit
I^2C	Inter Integrated Circuit
IDE	Integrated Development Environment
IRAM	Internal RAM
LDO	Low Dropout Regulator
LPF	Low Pass Filter
LVD	Low Voltage Detection
MDU	Multiplication Division Unit
ME	Motor Engine
MSB	Most Significant Bit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
Not connected	Not Connected
PGA	Programmable Gain Amplifier
PI	Proportional Integral 比例积分
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
QEP	Quadrature Encoder Pulse
RAM	Random Access Memory

RMW	Read Modified Write
ROM	Read Only Memory
RSD	Rotating State Detection
RTC	Real Time Clock
SAR	Successive Approximation Register
SCL	Serial Clock Line
SDA	Serial Data Line
SFR	Special Function Register
SMO	Sliding Mode Observer
SOSC	Slow Oscillator
SPI	Serial Peripheral Interface
SVPWM	Space Vector PWM
TSD	Temperature Sensor Detect
UART	Universal Asynchronous Receiver/Transmitter
WDT	Watch Dog Timer
XRAM	External RAM
XSFR	External SFR

1 System Introduction

1.1 Features

- Power supply:
  - FU6812L2
    - Single-power supply mode: VCC_MODE = 0, VCC = 5V ~ 24V
    - Dual-power supply mode: VCC_MODE = 1, VCC ≥ VDD5 VCC = 5V ~ 36V， VDD5 = 5V
    - Low-voltage single-power supply mode： VCC_MODE = 1, VCC = VDD5 = 3V ~ 5.5V
  - FU6812N2/FU6812S2/FU6812V
    - High-voltage single-power supply mode: VCC = 5V ~ 24V
    - Low-voltage single-power supply mode： VCC = VDD5 = 3V ~ 5.5V
  - FU6862L/FU6862Q
    - Single-power supply mode: When VCC_MODE = 0, external power supply 12V~20V is connected to VCC pin, and internal LDO supplies VDD5 voltage.
  - FU6872P
    - Single-power supply mode: When Vexternal power supply 15V~17 V is connected to VCC pin, internal BUCK supplies VREG and internal LDO supplies VDD5 voltage.
  - FU6861Q2
    - Mode 1: VCC_MODE = 0, VCC = 5V ~ 24V, VDRV = 7V ~ 18V
    - Mode 2: VCC_MODE = 1, VCC = VDD5 = 3V ~ 5.5V, VDRV = 7V ~ 18V
  - FU6861N2/FU6861NF2/FU6861L2
    - Mode 1: VCC = 5 ~ 24V, VDRV = 7V ~ 18V
- Dual core: 8051 core and ME core. ME core achieves automatic calculation of FOC or square-wave control for BLDC motors, and 8051 core is used for parameter configuration and routine processing.
- An instruction cycle mostly takes 1 or 2 system clock cycle(s)
- 16kB Flash with CRC, self-program and code protection
- 256 bytes IRAM and 768 bytes XRAM
- ME: Core integrating LPF module, PI regulator, BLDC module, FOC module, MDU auxiliary computing

module

- 1T 16x16 multiplier, 16T 32/16 divider
- 16 interrupt sources with 4 configurable priority levels
- GIPO
  - FU6812L2: 34
  - FU6812N2: 20
  - FU6812S2: 12
  - FU6861Q2: 32
  - FU6861N2: 19 (P0.7/P1.1 multiplexed)
  - FU6861NF2: 19 (P0.7/P1.1 multiplexed)
  - FU6861L2: 27
  - FU6812V: 13
  - FU6862L: 20
  - FU6862Q: 20
  - FU6872P: 18 (P0.0/P3.3 multiplexed, P0.1/P3.4 multiplexed, P0.5/P1.1 multiplexed, P0.6/P0.7 multiplexed, and P1.3/P1.4 multiplexed)
- Timers:
  - 2*Programmable timers with capture feature
  - 1*QEP decoding programmable timer
  - 1*BLDC motor dedicated timer
  - 1*General-purpose timer
  - 1*RTC
- Communication interfaces:
  - 1*I^2C (for FU6812L2 / FU6812N2 / FU6861Q2 / FU6861L2 / FU6861N2 / FU6861NF2 / FU6872P)
  - 1*SPI (for FU6812L2 / FU6812N2 / FU6861Q2 / FU6861L2 / FU6861N2 / FU6861NF2) supporting 3-wire mode (for FU6812S2 / FU6862L / FU6862Q)
  - 1*UART (for FU6812L2 / FU6812N2 / FU6861Q2 / FU6861L2 / FU6861N2 / FU6861NF2) supporting 3-wire mode (for FU6812S2 / FU6862L / FU6862Q)
  - Dual-channel DMA: supporting data transmission via I^2C/SPI/UART (Different models support different

communication interfaces. For details, please refer to the above description)

- Analog peripherals:
  - 12-bit ADC, operating with 1μs conversion time and internal VREF or external VREF selectable as reference voltage (external VREF is available for FU6812L2/FU6812N2, FU6861Q2/FU6861L2/FU6861N2/FU6861NF2 and FU6862L/FU6862Q only)
  - Number of ADC channels:
    - FU6812L2: 12
    - FU6812N2: 7
    - FU6812S2: 6
    - FU6812V: 7
    - FU6861Q2: 12
    - FU6861L2: 11
    - FU6861N2: 9
    - FU6861NF2: 9
    - FU6862L: 10 (AD0/AD1 are the internal channels)
    - FU6862Q: 10 (AD0/AD1 are the internal channels)
    - FU6872P: 10 (AD0/AD1 are the internal channels)
  - Internal VREF. 3V, 4V, 4.5V and VDD5 can be selected as the internal reference (FU6872P only supports VDD5)
  - Internal VHALF (VREF/2) as the internal reference
  - 3*Standalone operational amplifiers (1*standalone operational amplifier for FU6812N2/FU6812S2, FU6861N2/6861NF2)
  - 3-channel analog comparator (2-channel analog comparator for FU6812N2/FU6812S2/FU6812V/FU6872P)
  - 8-bit DAC
- Drive Type
  - FU6812L2/FU6812N2/FU6812S2/FU6812V: PWM output
  - 6N Pre-driver Output (for FU6861Q2/FU6861N2/FU6861NF2/FU6861L2/FU6862L/FU6862Q/FU6872P)
- Automatic commutation, cycle-by-cycle current limiting and Hall/BEMF-based position sensing for BLDC motor control

- FOC module supports single/dual/triple-shunt current sampling (For FU6812N2/FU6812S2, FU6861N2/FU6861NF2, FOC module supports single-shunt current sampling)
- FOC module supports overmodulation
- System clock
  - Built-in 24MHz high-speed RC oscillator
  - Built-in 32.8kHz low-speed RC oscillator
- WDT
- LVD
- TSD
- Two-wire FICE protocol based in-circuit emulation

1.2 Applications

The chip can be used for the drive of sensorless or sensored BLDC/PMSM motors, single-phase/three-phase induction motors and servo motors.

- FU6812L2: Refrigerators, range hoods, air conditioner indoor units, ceiling fans, hair dryers, high-voltage pedestal fans, high-voltage vacuum cleaners, industrial fans, water pumps, compressors, angle grinders, air compressors etc.
- FU6812N2: Refrigerators, range hoods, air conditioner indoor units, ceiling fans, hair dryers, high-voltage pedestal fans, high-voltage vacuum cleaners, industrial fans, high-voltage water pumps, compressors, angle grinders, air compressors etc.
- FU6812S2: Refrigerators, range hoods, air conditioner indoor units, ceiling fans, hair dryers, high-voltage pedestal fans, high-voltage vacuum cleaners, industrial fans, high-voltage water pumps, compressors, angle grinders, air compressors etc.
- FU6812V: Refrigerators, range hoods, air conditioner indoor units, ceiling fans, hair dryers, high-voltage pedestal fans, high-voltage vacuum cleaners, industrial fans, high-voltage water pumps, compressors, angle grinders, air compressors etc.
- FU6861Q2: Vacuum cleaners, power tools, gardening tools, low-voltage ceiling fans, water pumps, compressors, electric vehicles, low-voltage industrial fans, drones, etc.
- FU6861L2: Vacuum cleaners, power tools, gardening tools, low-voltage ceiling fans, water pumps,

compressors, electric vehicles, low-voltage industrial fans, drones, etc.

- FU6861N2: Vacuum cleaners, power tools, gardening tools, low-voltage ceiling fans, water pumps, compressors, electric vehicles, low-voltage industrial fans, drones, etc.
- FU6861NF2: Vacuum cleaners, power tools, gardening tools, etc.
- FU6862L: Refrigerators, range hoods, air conditioner indoor units, ceiling fans, hair dryers, high-voltage pedestal fans, high-voltage vacuum cleaners, industrial fans, high-voltage water pumps, compressors, etc.
- FU6862Q: Refrigerators, range hoods, air conditioner indoor units, ceiling fans, hair dryers, high-voltage pedestal fans, high-voltage vacuum cleaners, industrial fans, high-voltage water pumps, compressors, etc.
- FU6872P: Cooling fan

1.3 Overview

The high-performance motor drive chip incorporates ME core and 8051 core. ME core integrates FOC, MDU, LPF, PI and SVPWM modules that allow for automatic calculation of FOC or square-wave control by the hardware for sensored/sensorless BLDC/PMSM motors. 8051 core is used for parameter configuration and routine processing. Most of 8051 core instruction cycle takes 1T or 2T clock cycle(s). The dual cores work in parallel to achieve high-performance motor control. The chip integrates high-speed operational amplifiers, comparators, high-speed ADC, multiplier/divider, CRC, SPI, I^2C, UART, Timers, PWM modules, built-in high-voltage LDO, which are suitable for FOC or square-wave based BLDC/PMSM motors.

The above are the general descriptions on the product family. The features vary by models. For details, see section 2 Pin Definitions and 4 Ordering Information.2Pin Definitions4Ordering Information

For concise description and easy differentiation, if it is specified that a feature is applied to a specific model, the feature is exclusive to this model. Otherwise, the feature is a common feature of the product family.

FU6812 includes FU6812L2(LQFP48), FU6812N2(QFN32), FU6812S2(SSOP24) and FU6812V(SSOP24).

FU6861 includes FU6861Q2(QFN56), FU6861N2/FU6861NF2(QFN40) and FU6861L2(LQFP48).

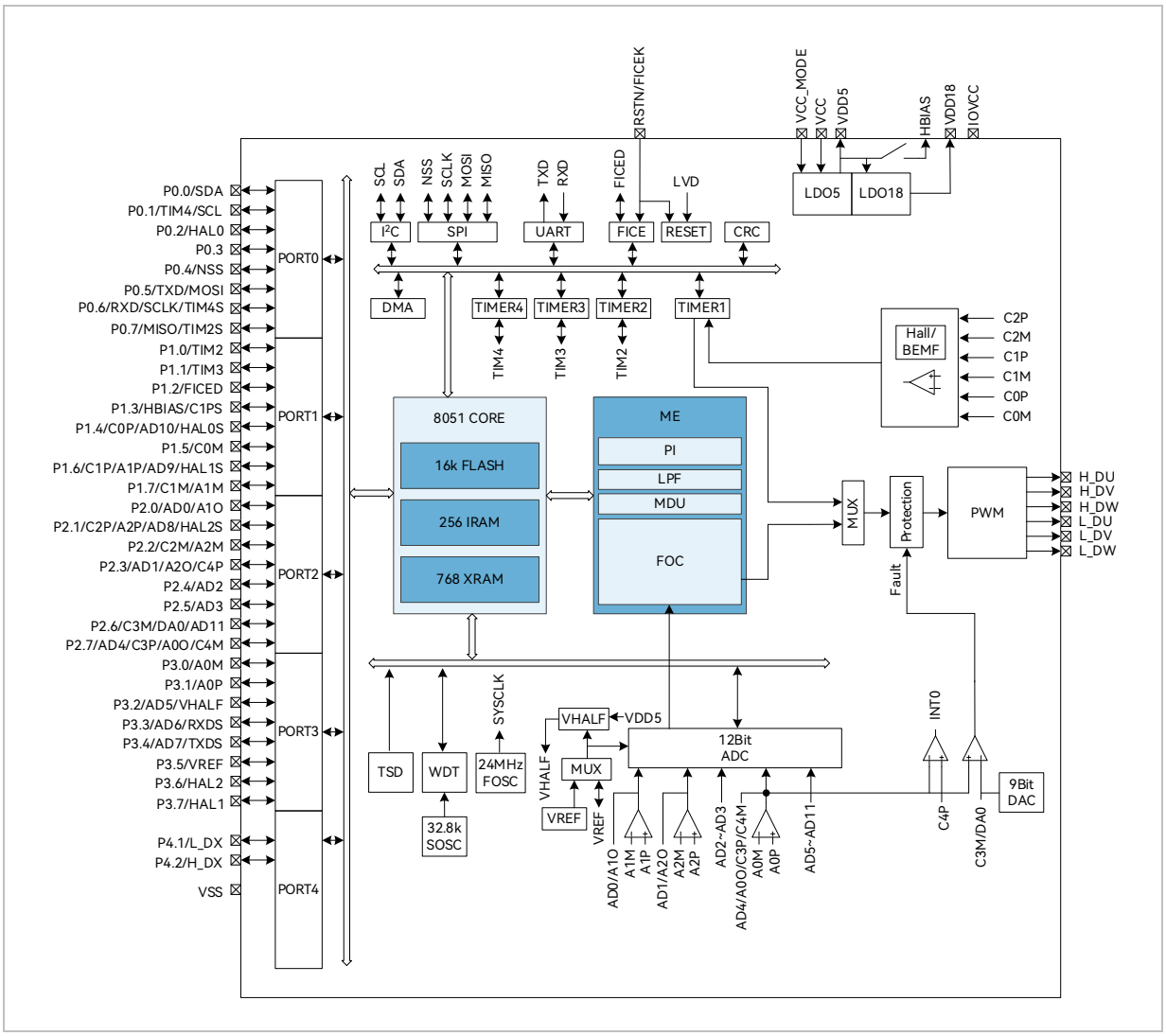
FU6862 includes FU6862L(LQFP48) and FU6862Q(QFN48-38).

Package type of FU6872: FU6872P(PLQFN32)

1.4 Functional Block Diagram

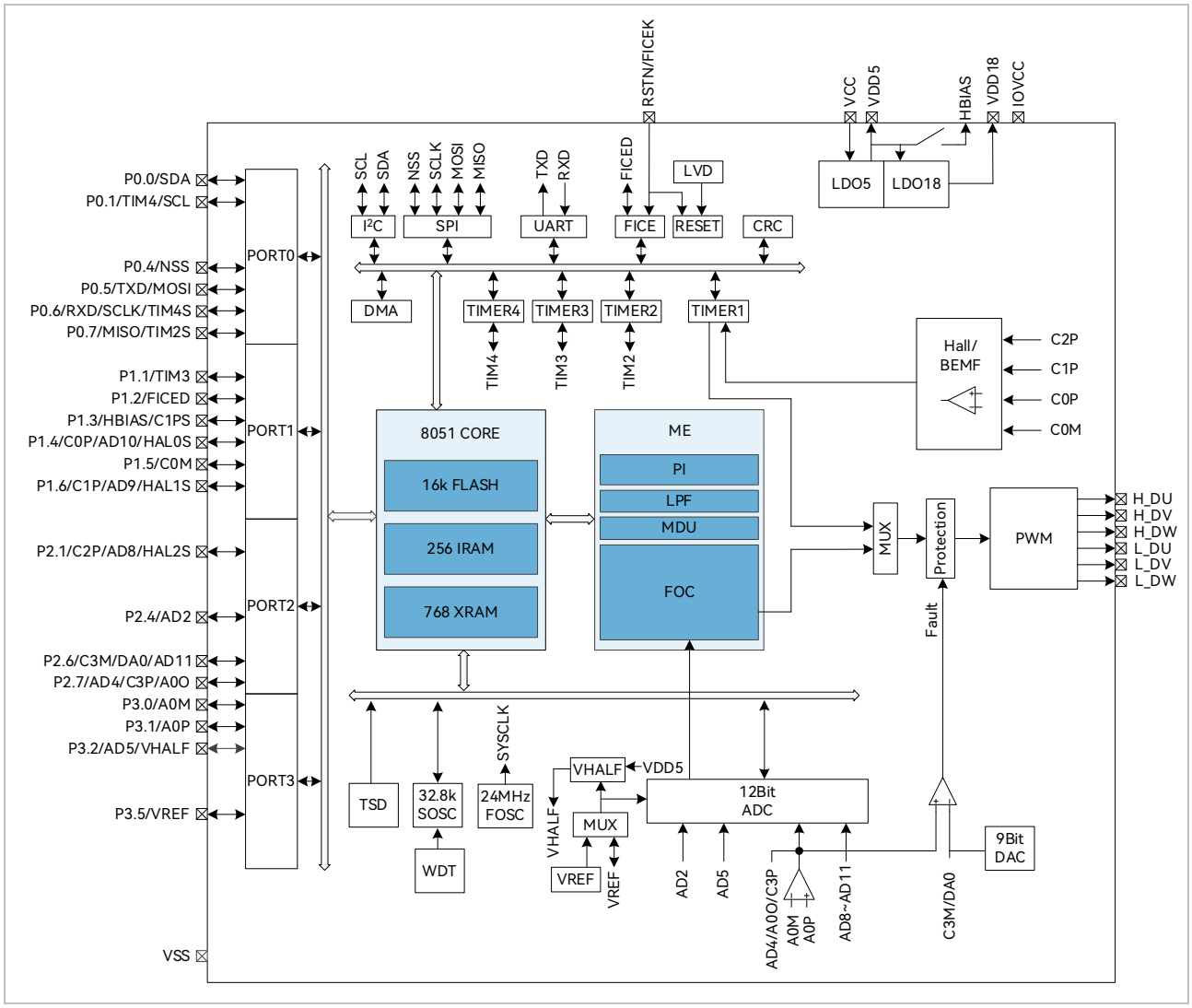
1.4.1 FU6812L2

Figure 1-1 Functional Block Diagram of FU6812L2



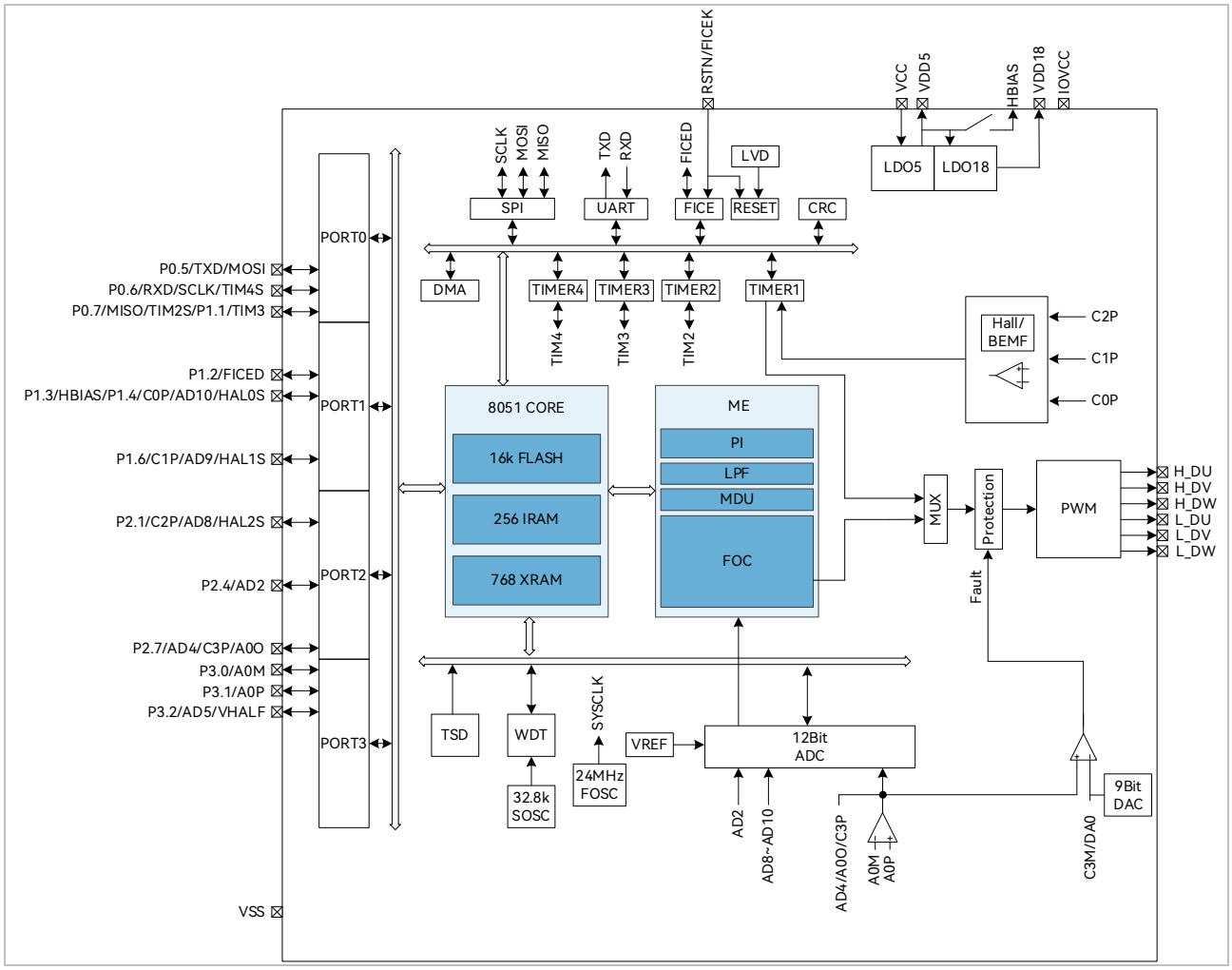
1.4.2 FU6812N2

Figure 1-2 Functional Block Diagram of FU6812N



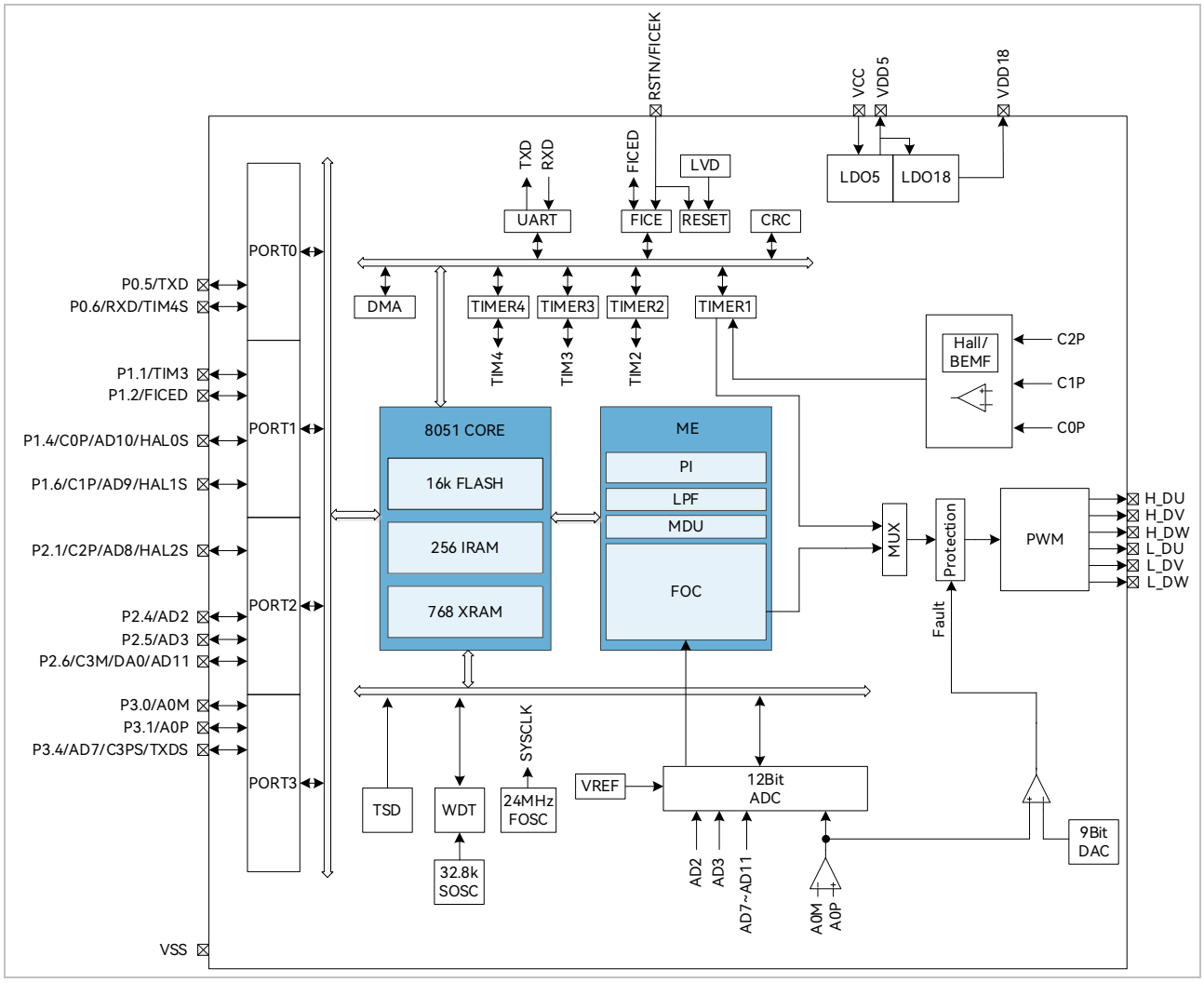
1.4.3 FU6812S2

Figure 1-3 Functional Block Diagram of FU6812S2



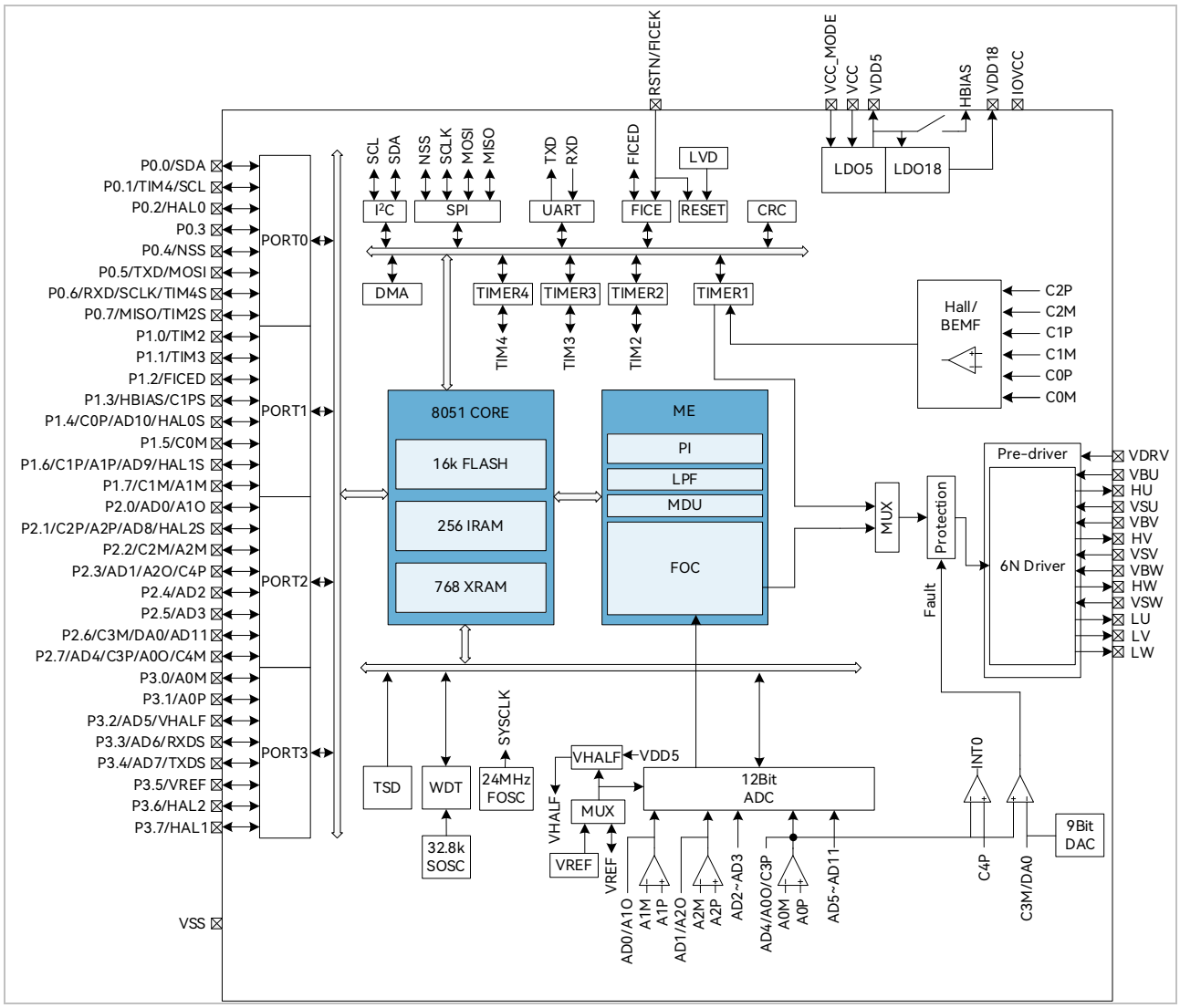
1.4.4 FU6812V

Figure 1-4 Functional Block Diagram of FU6812V



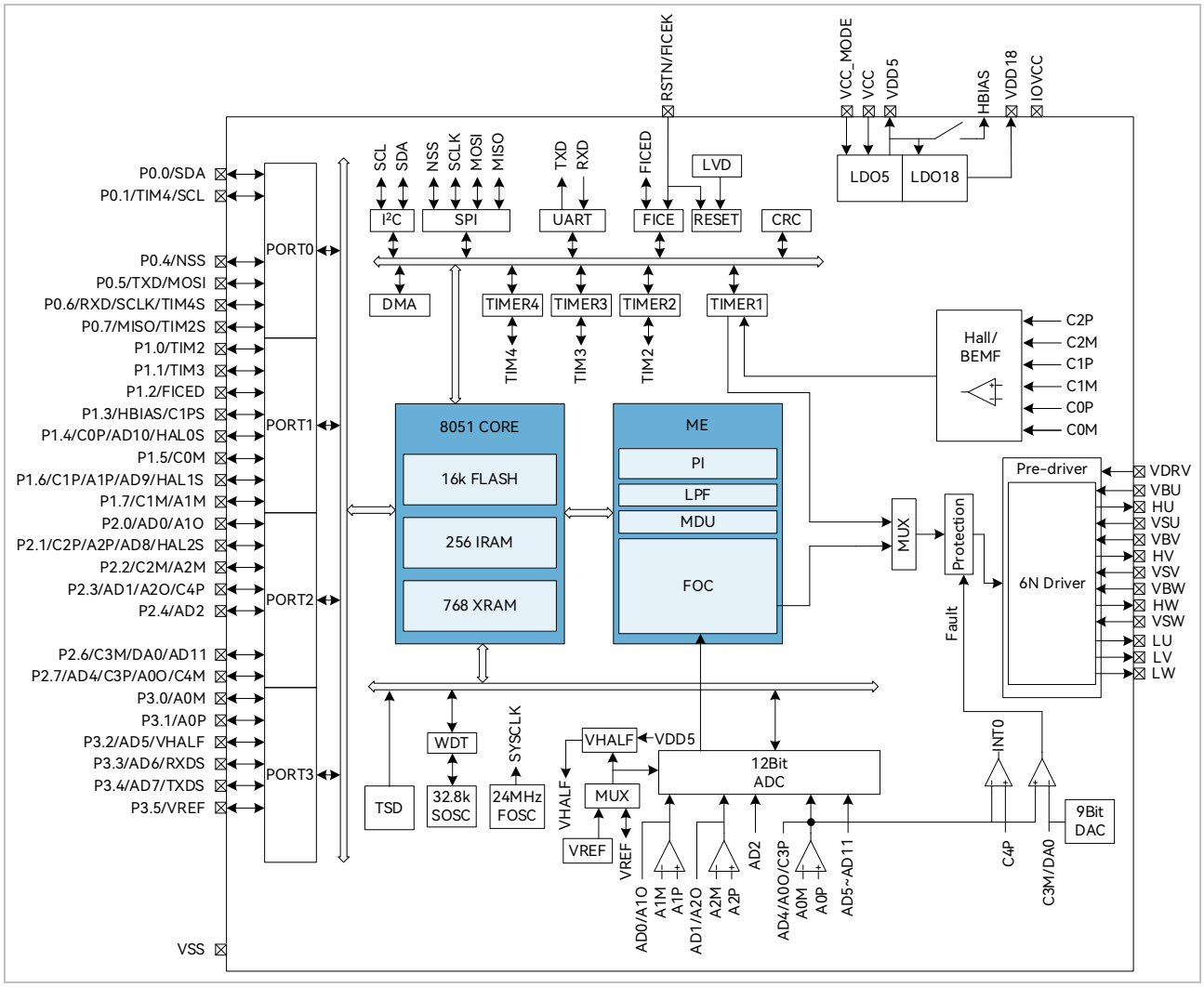
1.4.5 FU6861Q2

Figure 1-5 Functional Block Diagram of FU6861Q2



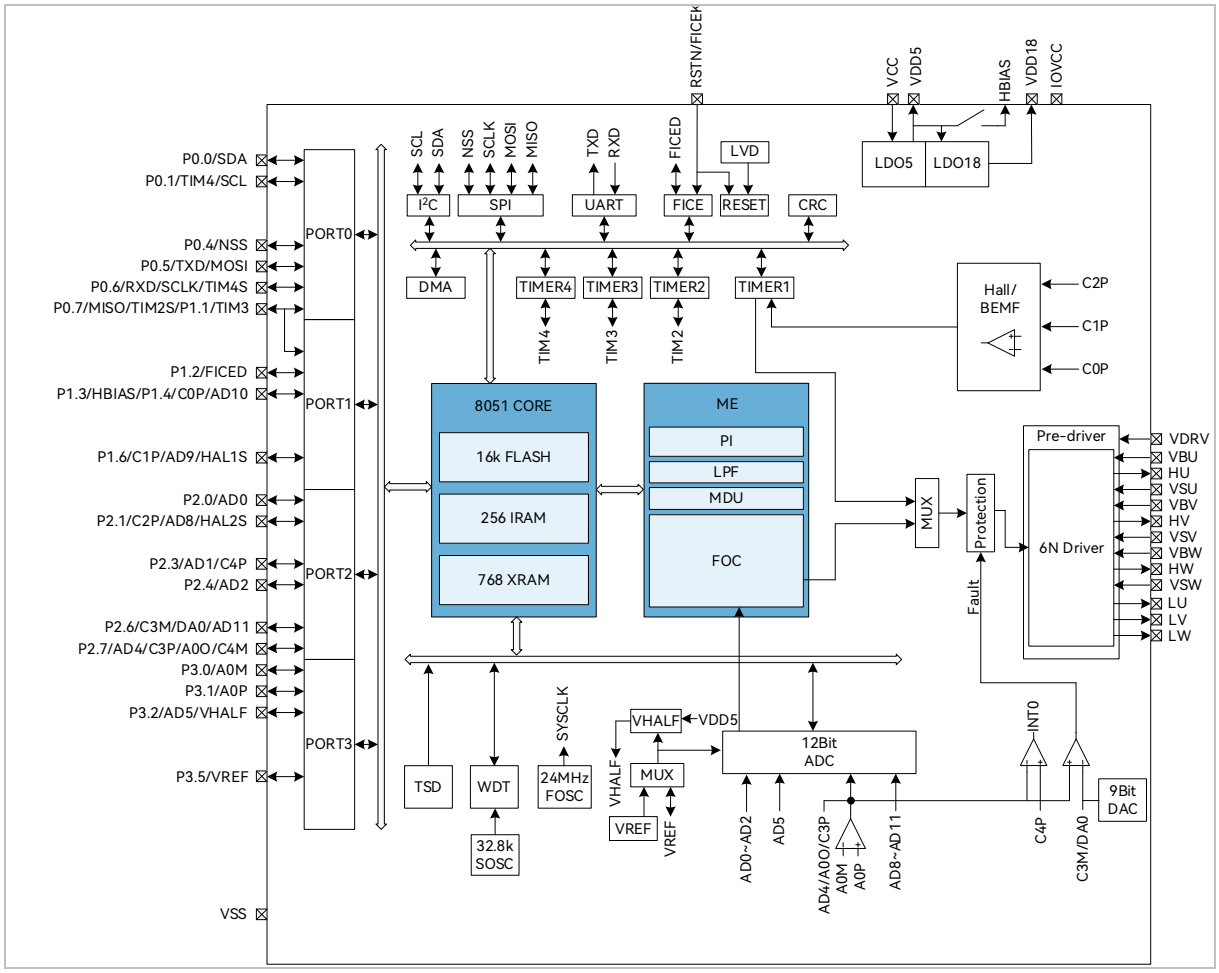
1.4.6 FU6861L2

Figure 1-6 Functional Block Diagram of FU6861L2



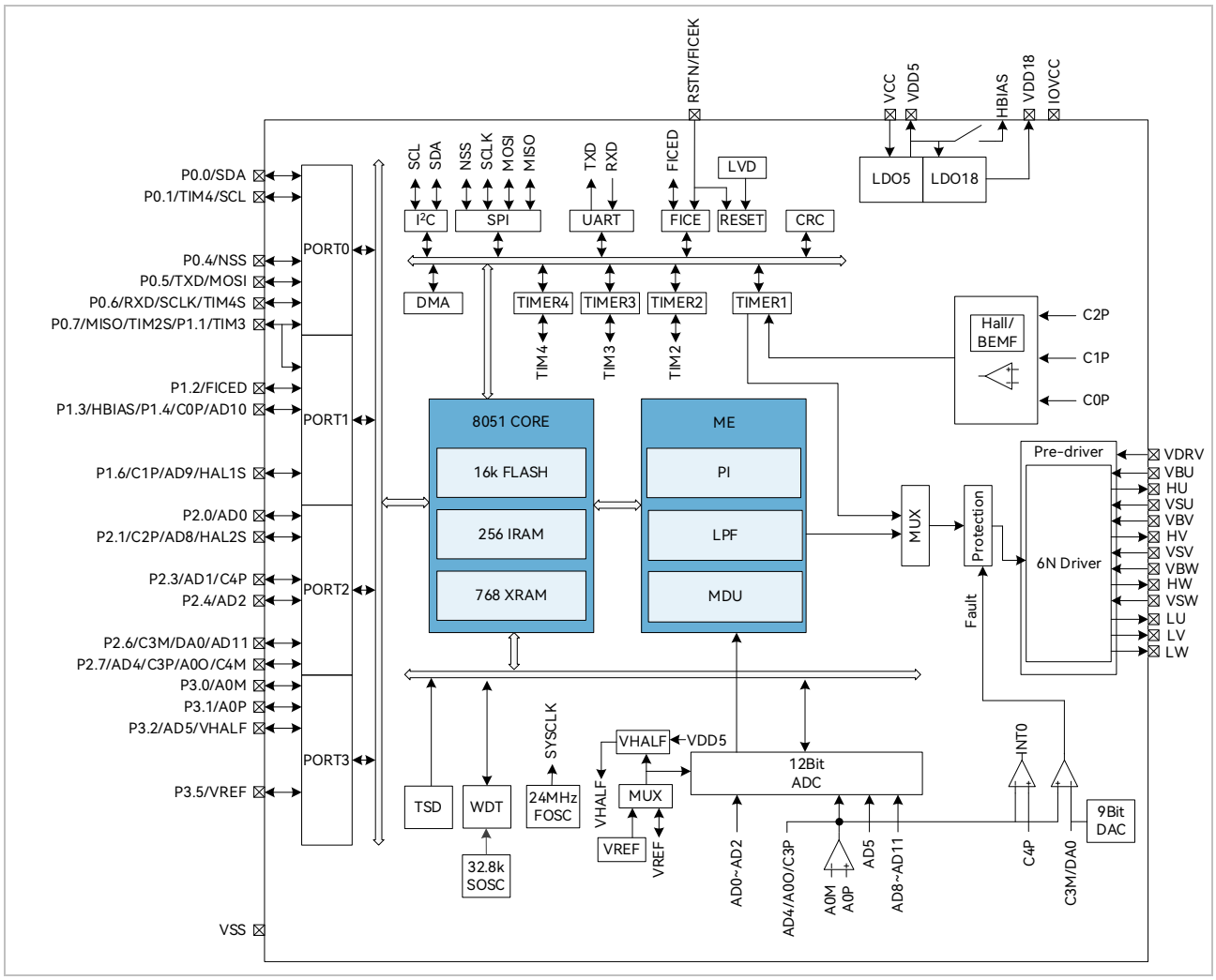
1.4.7 FU6861N2

Figure 1-7 Functional Block Diagram of FU6861N2



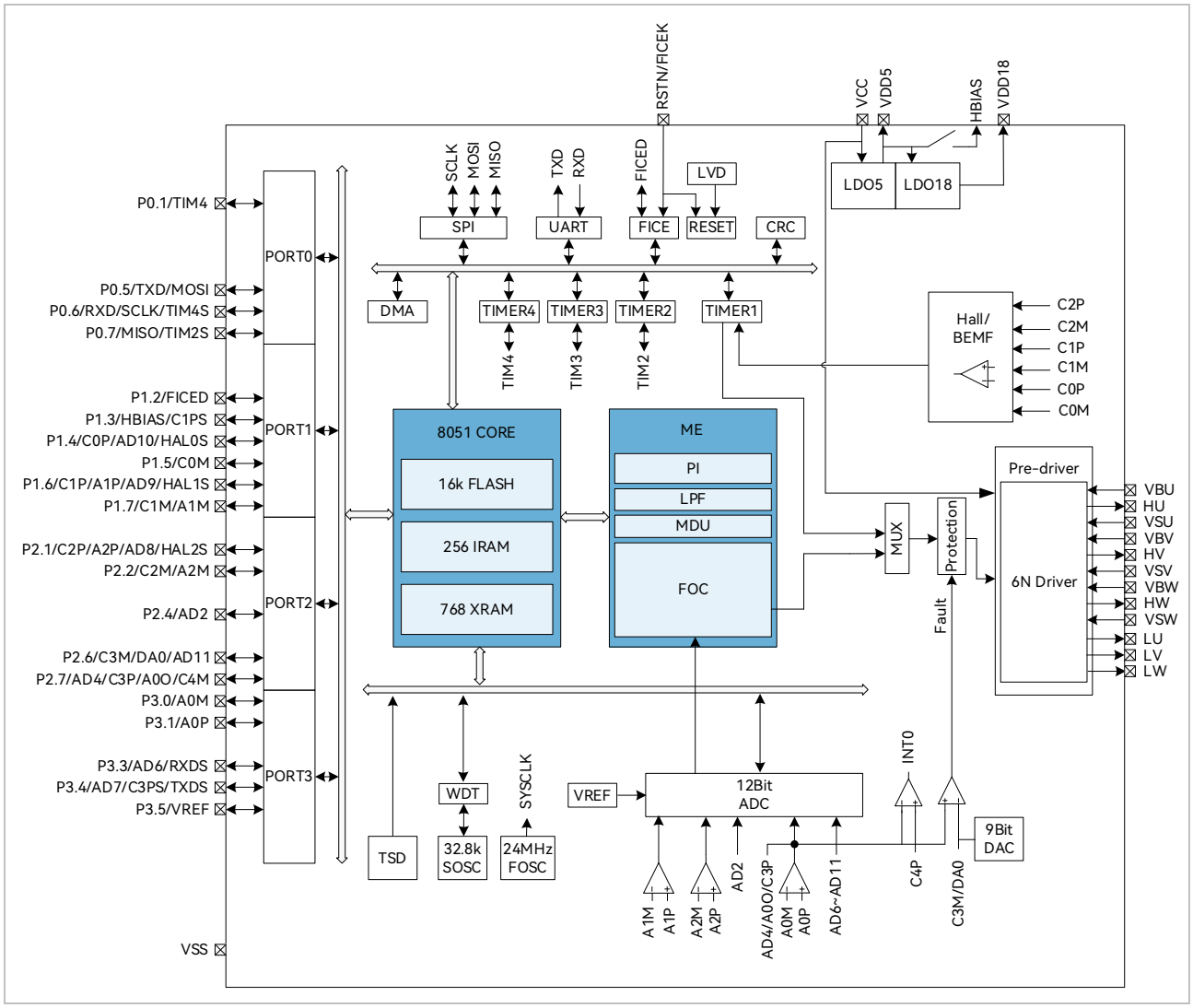
1.4.8 FU6861NF2

Figure 1-8 Functional Block Diagram of FU6861NF2



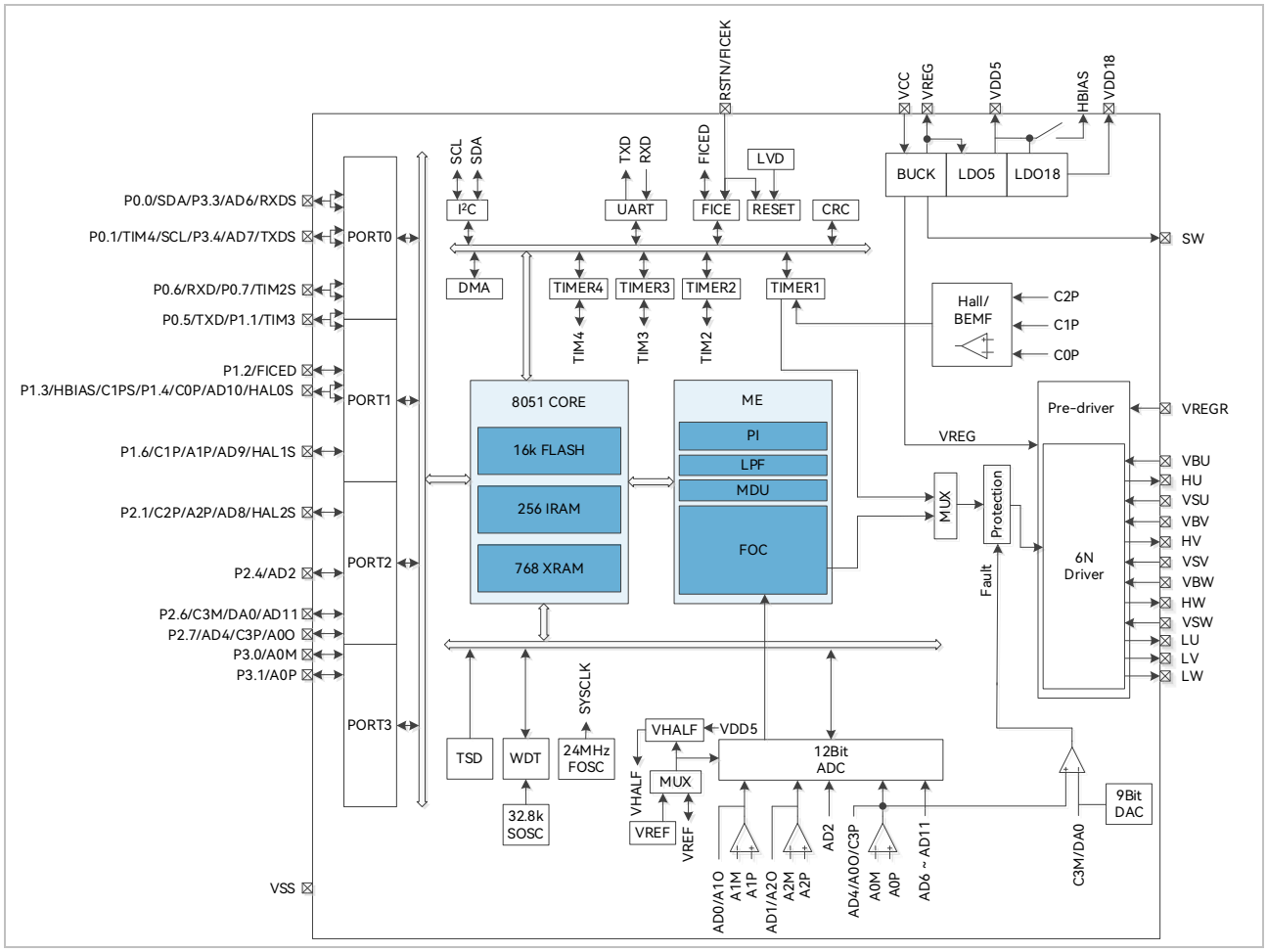
1.4.9 FU6862L/FU6862Q

Figure 1-9 Functional Block Diagram of FU6862L/FU6862Q



1.4.10 FU6872P

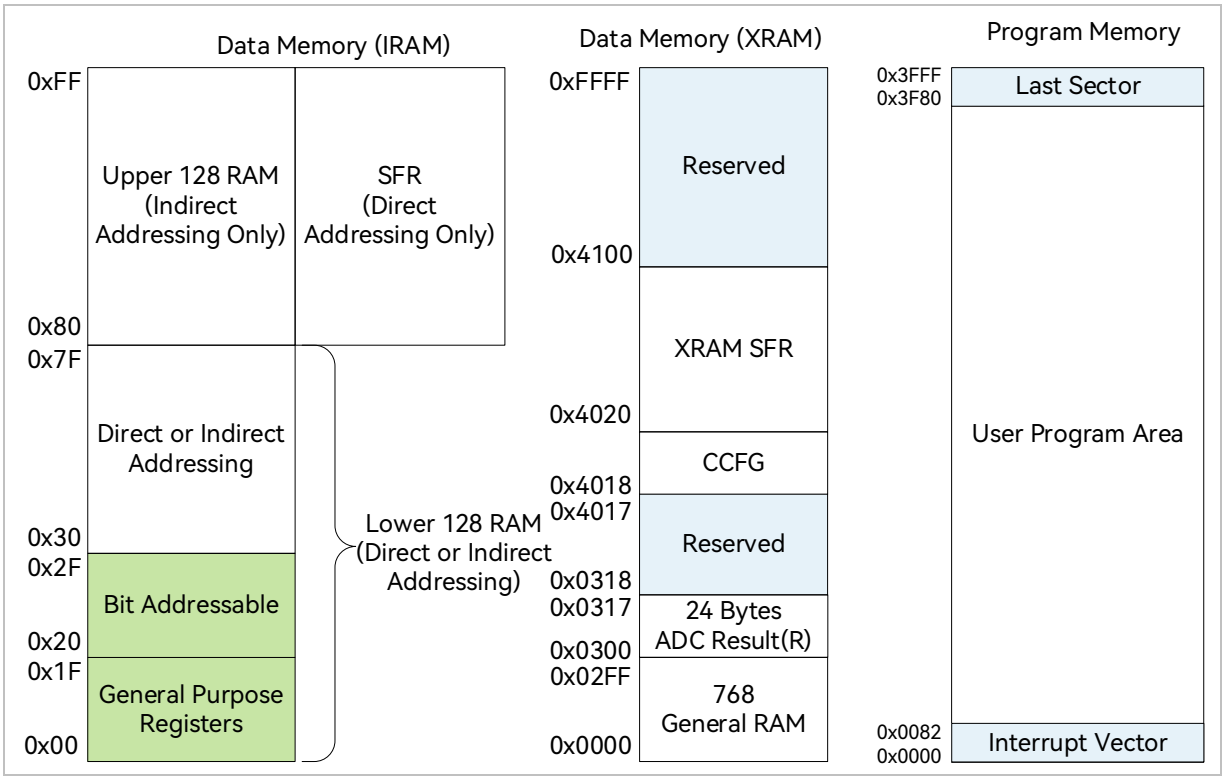
Figure 1-10 Functional Block Diagram of FU6872P



1.5 Memory Organization

The internal storage space is divided into Program Memory and Data Memory, which are independently addressed.

Figure 1-11 Memory Organization



1.5.1 Program Memory

The chip implements this program memory as Flash memory with a block from addresses 0x0000 to 0x3FFF to store control programs. CPU starts from 0x0000 after reset. The program memory storaage medium is Flash memory.

The sector (0x0000 ~ 0x0082) is the interrupt vector address area, which is used to store the start address of each interrupt subroutine. The last sector (0x3F80-0x3FFF) contains internal control bits of the chip.

1.5.2 Data Memory

The data memory is divided into External Data Memory and Internal Data Memory&SFRs.

The External Data Memory is addressed from 0x0000 to 0x02FF, which can be accessed with MOVX instructions only.

The Internal Data Memory is shown in Figure 1-11. Locations 0x00~0x1F are addressable as 4 banks of general-purpose registers, each bank consisting of 8 registers. Locations 0x20~0x2F are 16-bit addressable, and locations 0x30~0x7F support direct and indirect addressing. When locations 0x80~0xFF are accessed by indirect addressing, it points to RAM. When locations 0x80~0xFF are accessed by direct addressing, it points to SFRs. Stack space is located in the Internal Data Memory.

1.5.3 SFR

Table 1-1 SFR Address Mapping

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0xF8	DRV_OUT	PI_LPF_CR			P0_OE	P1_OE	P2_OE	P3_OE
0xF0	B		PI_KIL	PI_KIH	PI_UKMAXL	PI_UKMAXH	PI_UKMINL	PI_UKMINH
0xE8	P4	P4_OE	PI_EKL	PI_EKH	PI_UKL	PI_UKH	PI_KPL	PI_KPH
0xE0	ACC						LPF_YL	LPF_YH
0xD8	IP3	EVT_FILT	CMP_CR2	LVSR	CMP_CR3	LPF_K	LPF_XL	LPF_XH
0xD0	PSW	P1_IE	P1_IF	P2_IE	P2_IF	CMP_CR0	CMP_CR1	CMP_SR
0xC8	IP2	RST_SR	MDU_MBL	MDU_MBH	MDU_DB0	MDU_DB1		
0xC0	IP1	MDU_CR	MDU_MAL	MDU_MAH	MDU_DA0	MDU_DA1	MDU_DA2	MDU_DA3
0xB8	IP0							
0xB0	P3							
0xA8	IE	TIM2_CR1	TIM2__CNTRL	TIM2__CNTRH	TIM2__DRL	TIM2__DRH	TIM2__ARRL	TIM2__ARRH
0xA0	P2	TIM2_CR0	TIM3__CNTRL	TIM3__CNTRH	TIM3__DRL	TIM3__DRH	TIM3__ARRL	TIM3__ARRH
0x98	UT_CR	UT_DR	UT_BAUDL	UT_BAUDH	TIM3_CR0	TIM3_CR1	TIM4_CR0	TIM4_CR1
0x90	P1		TIM4__CNTRL	TIM4__CNTRH	TIM4__DRL	TIM4__DRH	TIM4__ARRL	TIM4__ARRH
0x88	TCON							
0x80	P0	SP	DPL	DPH	FLA_KEY	FLA_CR		PCON

Note

- Registers with 4 low-order bits as 0 or 8 support addressing access
- Registers containing the symbol "__" shall be read using variables. If it is read directly, the value will be incorrect

1.5.4 XSFR

Table 1-2 XSFR Address Mapping

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x40F0	EXT0	TIM234_CTRL	CMP_AMP	TSD_ADJ				
0x40E8	FOC_ID_LPFK	FOC_IQ_LPFK	FOC_KFGH	FOC_KFGL			FOC_CR3	
0x40E0	FOC__EMFH	FOC__EMFL	FOC_UDCPSH	FOC_UDCPSL	FOC_UQCPSH	FOC_UQCPSL	FOC__UQEXH	FOC__UQEXL
0x40D8	FOC__POWH	FOC__POWL	FOC__IAMAXH	FOC__IAMAXL	FOC__IBMAXH	FOC__IBMAXL	FOC__ICMAXH	FOC__ICMAXL
0x40D0	FOC__EALPH	FOC__EALPL	FOC__EBETH	FOC__EBETL	FOC__EOMEH	FOC__EOMEL	FOC__ESQUH	FOC__ESQUL
0x40C8	FOC__IBH	FOC__IBL	FOC__IAH	FOC__IAL	FOC_THETAH	FOC_THETAL	FOC__ETHETAH	FOC__ETHETAL
0x40C0	FOC__IBETH	FOC__IBETL	FOC_VBETH	FOC_VBETL	FOC_VALPH	FOC_VALPL	FOC__ICH	FOC__ICL
0x40B8	FOC__UDH	FOC__UDL	FOC__UQH	FOC__UQL	FOC__IDH	FOC__IDL	FOC__IQH	FOC__IQL
0x40B0	FOC_DMAXH	FOC_DMAXL	FOC_DMINH	FOC_DMINL	FOC_QMAXH	FOC_QMAXL	FOC_QMINH	FOC_QMINL
0x40A8	FOC__RTHESTEPH	FOC__RTHESTEPL	FOC_RTHEACCH	FOC_RTHEACCL	FOC_RTHECNT	FOC_THECOR/ CMP_SAMR	FOC_THECOMPH	FOC_THECOMPL
0x40A0	FOC_CR1	FOC_CR2	FOC_TSMIN	FOC_TGLI	FOC_TBLO	FOC_TRGDLY	FOC_CSOH	FOC_CSOL
0x4098	FOC__UDCFLTH	FOC__UDCFLTL						
	TIM1__ITRIPH	TIM1__ITRIPL						
0x4090	FOC_IDREFH	FOC_IDREFL	FOC_IQREFH	FOC_IQREFL	FOC_DQKPH	FOC_DQKPL	FOC_DQKIH	FOC_DQKIL
0x4088	FOC_EK3H	FOC_EK3L	FOC_EK4H	FOC_EK4L	FOC_EK1H	FOC_EK1L	FOC_EK2H	FOC_EK2L
	TIM1__RARRH	TIM1__RARRL	TIM1__RCNTRH	TIM1__RCNTRL				
0x4080	FOC_FBASEH	FOC_FBASEL	FOC_EFREQACCH	FOC_EFREQACCL	FOC_EFREQMINH	FOC_EFRQMINL	FOC_EFREQHOLDH	FOC_EFREQHOLDL
	TIM1_DBR7H	TIM1_DBR7L	TIM1__BCNTRH	TIM1__BCNTRL	TIM1__BCCRH	TIM1__BCCRL	TIM1__BARRH	TIM1__BARRL
0x4078	FOC_KSLIDEH	FOC_KSLIDEL	FOC_EKLPFMINH	FOC_EKLPFMINL	FOC_EBMFKH	FOC_EBMFKL	FOC_OMEKLPFH	FOC_OMEKLPFL
	TIM1_DBR3H	TIM1_DBR3L	TIM1_DBR4H	TIM1_DBR4L	TIM1_DBR5H	TIM1_DBR5L	TIM1_DBR6H	TIM1_DBR6L
0x4070	TIM1__BCORH	TIM1__BCORL			FOC_EKPH	FOC_EKPL	FOC_EKIH	FOC_EKIL
					TIM1_DBR1H	TIM1_DBR1L	TIM1_DBR2H	TIM1_DBR2L
0x4068	TIM1_CR0	TIM1_CR1	TIM1_CR2	TIM1_CR3	TIM1_CR4	TIM1_ IER	TIM1_SR	

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x4060	DRV_DTR	DRV_SR	DRV_CR		SYST_ARRH	SYST_ARRL		
0x4058	DRV_DRH	DRV_DRL	DRV_COMRH	DRV_COMRL	DRV_CMRH	DRV_CMRL	DRV_ARRH	DRV_ARRL
0x4050	P1_AN	P2_AN	P3_AN	P0_PU	P1_PU	P2_PU	P3_PU	P4_PU
0x4048				DAC_DR	PH_SEL		AMP_CR	VREF_VHALF_CR
0x4040	CAL_CRH	CAL_CRL						
0x4038	ADC_SCYC	ADC_CR	DMA0_CR0	DMA1_CR0	DMA0_CR1H	DMA0_CR1L	DMA1_CR1H	DMA1_CR1L
0x4030	SPI_CR0	SPI_CR1	SPI_CLK	SPI_DR		DAC_CR	ADC_MASK_SYSCH	ADC_MASK_SYSCL
0x4028	I2C_CR	I2C_ID	I2C_DR	I2C_SR	RTC_TMH	RTC_TML	RTC_STA	
0x4020		CRC_DIN	CRC_CR	CRC_DR	CRC_BEG	CRC_CNT	WDT_CR	WDT_REL
0x4018						CCFG2	CCFG1	
0x0310	ADC8_DRH	ADC8_DRL	ADC9_DRH	ADC9_DRL	ADC10_DRH	ADC10_DRL	ADC11_DRH	ADC11_DRL
0x0308	ADC4_DRH	ADC4_DRL	ADC5_DRH	ADC5_DRL	ADC6_DRH	ADC6_DRL	ADC7_DRH	ADC7_DRL
0x0300	ADC0_DRH	ADC0_DRL	ADC1_DRH	ADC1_DRL	ADC2_DRH	ADC2_DRL	ADC3_DRH	ADC3_DRL

0x03F8	LPF0_K	LPF0_X	LPF0_YH	LPF0_YL
0x03F0	LPF1_K	LPF1_X	LPF1_YH	LPF1_YL
0x03E8	PI0_UKH	PI0_UKL	PI0_UKMAX	PI0_UKMIN
0x03E0	PI0_KP	PI0_EK1	PI0_EK	PI0_KI
0x03D8	PI1_UKH	PI1_UKL	PI1_UKMAX	PI1_UKMIN
0x03D0	PI1_KP	PI1_EK1	PI1_EK	PI1_KI
0x03C8	MUL0_MA	MUL0_MB	MUL0_MCH	MUL0_MCL
0x03C0	MUL1_MA	MUL1_MB	MUL1_MCH	MUL1_MCL
0x03B8	DIV0_DB	DIV0_DQH	DIV0_DQL	DIV0_DR
0x03B0	DIV1_DQL	DIV1_DR	DIV0_DAH	DIV0_DAL
0x03A8	DIV1_DAH	DIV1_DAL	DIV1_DB	DIV1_DQH
0x03A0	LPF2_K	LPF2_X	LPF2_YH	LPF2_YL
0x0398	LPF3_K	LPF3_X	LPF3_YH	LPF3_YL

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x0390	PI2_UKH		PI2_UKL		PI2_UKMAX		PI2_UKMIN	
0x0388	PI2_KP		PI2_EK1		PI2_EK		PI2_KI	
0x0380	PI3_UKH		PI3_UKL		PI3_UKMAX		PI3_UKMIN	
0x0378	PI3_KP		PI3_EK1		PI3_EK		PI3_KI	
0x0370	MUL2_MA		MUL2_MB		MUL2_MCH		MUL2_MCL	
0x0368	MUL3_MA		MUL3_MB		MUL3_MCH		MUL3_MCL	
0x0360	DIV2_DB		DIV2_DQH		DIV2_DQL		DIV2_DR	
0x0358	DIV3_DQL		DIV3_DR		DIV2_DAH		DIV2_DAL	
0x0350	DIV3_DAH		DIV3_DAL		DIV3_DB		DIV3_DQH	
0x0348	SCAT0_SIN		SCAT0_THE		SCAT0_RES1		SCAT0_RES2	
0x0340	SCAT1_THE		SCAT1_RES1		SCAT1_RES2		SCAT0_COS	
0x0338	SCAT2_RES1		SCAT2_RES2		SCAT1_COS		SCAT1_SIN	
0x0330	SCAT3_RES2		SCAT2_COS		SCAT2_SIN		SCAT2_THE	
0x0328	SCAT3_COS		SCAT3_SIN		SCAT3_THE		SCAT3_RES1	

Note

- Registers containing the symbol "__" shall be read using variables. If it is read directly, the value will be incorrect
- The SFR is mapped partly to SFR sector of the Internal Data Memory, and partly to External Data Memory (also known as XSFR)

2 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- DB = Digital Bidirectional
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

2.1 FU6812L2 LQFP48 Pins

Table 2-1 Pin Descriptions of FU6812L2 LQFP48

Pin	FU6812L2 LQFP48	IO Type	Function Descriptions
P2.2/ C2M/ A2M	1	DB/ AI/ AI	GPIO, configurable as INT1 input CMP2 negative input AMP2 negative input
P2.3/ AD1/ A2O/ C4P	2	DB/ AI/ AO/ AI	GPIO, configurable as INT1 input Input of ADC channel 1 for collecting amplified signals from AMP2 AMP2 output CMP4 positive input
P2.4/ AD2	3	DB/ AI	GPIO, configurable as INT1 input Input of ADC channel 2 or bus voltage signal
P2.5/ AD3	4	DB/ AI	GPIO, configurable as INT1 input Input of ADC channel 3
P2.6/ C3M/ DA0/ ADC11	5	DB/ AI/ AO/ AI	GPIO, configurable as INT1 input CMP3 negative input DAC output, without Buffer output Input of ADC channel 11

Pin	FU6812L2 LQFP48	IO Type	Function Descriptions
P2.7/ AD4/ C3P/ A0O/ C4M	6	DB/ AI/ AI/ AO/ AI	GPIO, configurable as INT1 input Input of ADC channel 4 for collecting the amplified bus current signal CMP3 positive input for bus current sampling to detect overcurrent AMP0 output, the voltage output after the bus current is amplified CMP4 negative input
P3.0/ A0M/	7	DB/ AI	GPIO AMP0 negative input for amplifying the bus current signal
P3.1/ A0P	8	DB/ AI	GPIO AMP0 positive input for amplifying the bus current signal
P3.2/ AD5/ VHALF	9	DB/ AI/ AO	GPIO Input of ADC channel 5 or over-temperature signal input 1/2 VDD5 or 1/2 VREF output with an external 1μF capacitor
P3.3/ AD6/ RXDS	10	DB/ AI/ DB	GPIO Input of ADC channel 6 UART RXD input in two-wire mode or TXD output/RXD input in single-wire mode after function switching
P3.4/ AD7/ TXDS	11	DB AI/ DO	GPIO Input of ADC channel 7 or analog speed control input UART TXD output after function switching
P3.5/ VREF	12	DB/ AI	GPIO ADC external VREF input or internal VREF output, with a 1μF~4.7μF external capacitor
VSS	13	P	Ground
IOVCC	14	P	GPIO power supply, ranging from 3V to 5.5V, with a 1μF ~ 10μF capacitor connected to the ground. IOVCC ≤ VDD5. IOVCC supplies P3.7 ~ 6, P0.x, P1.1 ~~ 0, P4.x, H_DU, H_DV, H_DW, L_DU, L_DV and L_DW only, and VDD5 supplies other GPIOs.
P3.6/ HAL2	15	DB/ DI	GPIO Hall2 logic level input
P3.7/ HAL1	16	DB/ DI	GPIO Hall1 logic level input
P0.0/ SDA	17	DB/ DB	GPIO, configurable as INT0 input I^2C SDA, configured as open-drain output

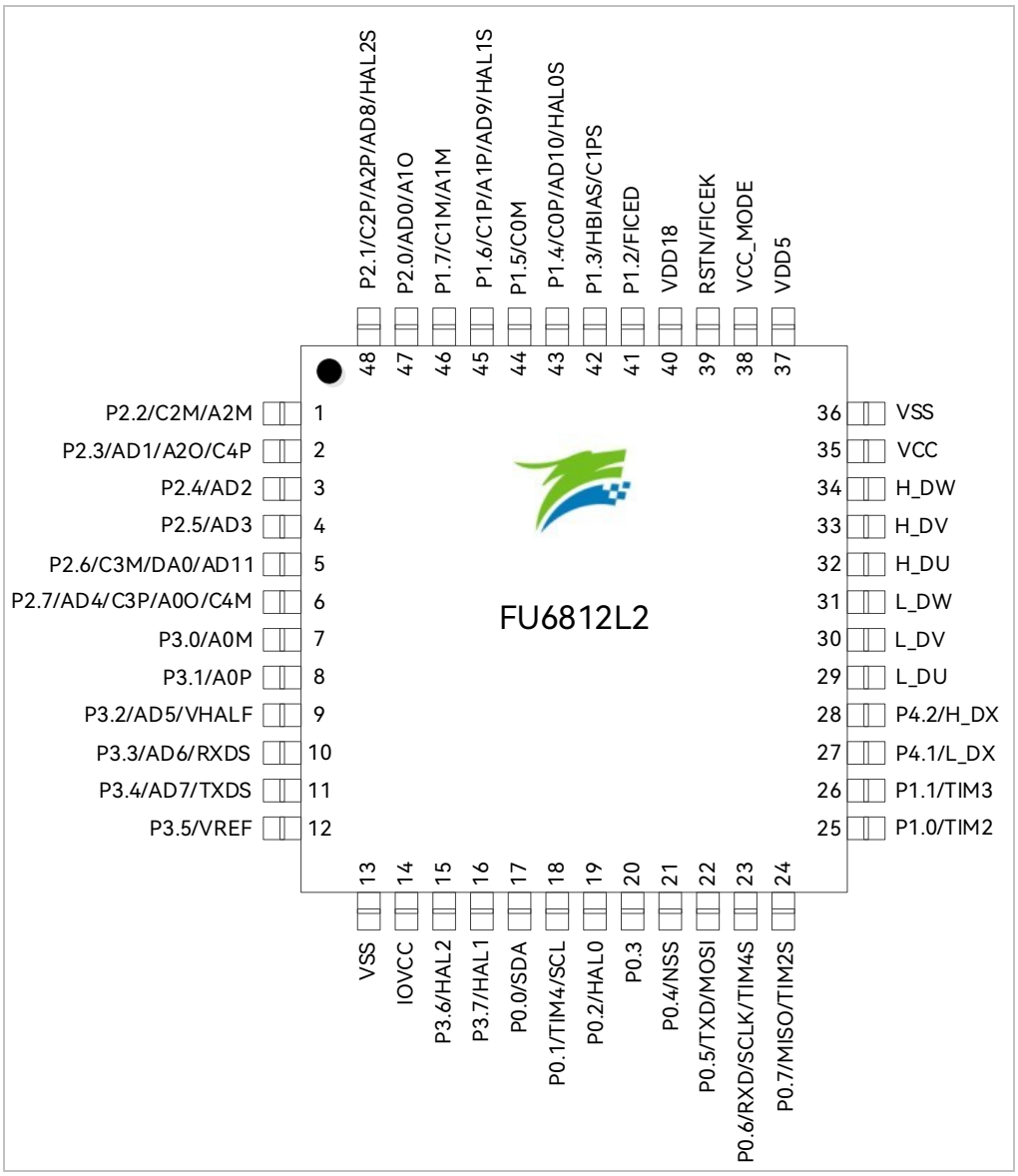
Pin	FU6812L2 LQFP48	IO Type	Function Descriptions
P0.1/ TIM4/ SCL	18	DB/ DB/ DB	GPIO, configurable as INT0 input Timer4 input capture mode I²C SCL, configured as open-drain output
P0.2/ HAL0	19	DB/ DI	GPIO, configurable as INT0 input Hall0 logic level input
P0.3	20	DB	GPIO, configurable as INT0 input
P0.4/ NSS	21	DB/ DB	GPIO, configurable as INT0 input SPI NSS
P0.5/ TXD/ MOSI	22	DB/ DO/ DI	GPIO, configurable as INT0 input UART1 TXD output SPI MOSI, master output or slave input
P0.6/ RXD/ SCLK/ TIM4S	23	DB/ DI/ DB/ DB	GPIO, configurable as INT0 input UART1 RXD SPI SCLK Timer4 input capture mode or PWM output after function switching
P0.7/ MISO/ TIM2S	24	DB/ DB/ DB	GPIO SPI MISO, master input or slave output Timer2 input capture mode or PWM output after function switching
P1.0/ TIM2	25	DB/ DB	GPIO, configurable as INT1 input Timer2 input capture mode or PWM output before function switching
P1.1/ TIM3	26	DB/ DB	GPIO, configurable as INT0/INT1 input Timer3 input capture mode
P4.1/ L_DX	27	DB/ DO	GPIO PWM output at low side of phase X
P4.2/ H_DX	28	DB/ DO	GPIO PWM output at high side of phase X
L_DU	29	DO	PWM output at low side of phase U
L_DV	30	DO	PWM output at low side of phase V
L_DW	31	DO	PWM output at low side of phase W
H_DU	32	DO	PWM output at high side of phase U
H_DV	33	DO	PWM output at high side of phase V
H_DW	34	DO	PWM output at high side of phase W

Pin	FU6812L2 LQFP48	IO Type	Function Descriptions
VCC	35	P	Power input. The voltage range is determined by VCC_MODE, with an external filter capacitor of 10μF or above. 1. High-voltage single-power supply mode: When VCC_MODE = 0, external power supply 5V~24V is connected to VCC pin, and internal LDO supplies VDD5 voltage. 2. Low-voltage single-power supply mode: When VCC_MODE = 1, external power supply 3V~5.5V is connected to VDD5 pin, and VDD5 pin is shorted to VCC pin. 3. Dual-power supply mode: When VCC_MODE = 1, external power supply 1 (5V~36V) is connected to VCC pin, and external power supply 2 (5V) is connected to VDD5 pin.
VSS	36	P	Ground
VDD5	37	P	Mid-voltage power input or 5V LDO power output is determined by VCC_MODE. See descriptions on VCC pin for power connection. It is connected with a 1μF~4.7μF external capacitor. When VCC_MODE = 0, internal LDO outputs 5V power supply. When VCC_MODE = 1, 3V~5.5V external power is supplied.
VCC_MODE	38	DI	Power supply mode control. See descriptions on VCC pin for details.
RSTN/ FICEK	39	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VDD18	40	P	Low-voltage power supply input or internal LDO outputs 1.85V power supply
P1.2/ FICED	41	DB/ DB	GPIO, configurable as INT1 input FICE data line
P1.3/ HBIAS/ C1PS	42	DB/ DO/ AI	GPIO, configurable as INT1 input Hall bias power supply, internally connected to VDD5 via a switch CMP1 positive input after function switching
P1.4/ C0P/ AD10/ HAL0S	43	DB/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP0 positive input Input of ADC channel 10 Hall-IC0 logic level input after function switching
P1.5/ C0M	44	DB/ AI	GPIO, configurable as INT1 input CMP0 negative input

Pin	FU6812L2 LQFP48	IO Type	Function Descriptions
P1.6/		AO/	GPIO, configurable as INT1 input
C1P/		AI/	CMP1 positive input
A1P/	45	AI/	AMP1 positive input
AD9/		AI/	Input of ADC channel 9
HAL1S		DI	Hall-IC1 logic level input after function switching
P1.7/		DB/	GPIO, configurable as INT1 input
C1M/	46	AI/	CMP1 negative input
A1M		AI	AMP1 negative input
P2.0/		DB/	GPIO, configurable as INT1 input
AD0/	47	AI/	Input of ADC channel 0 for collecting amplified signals from AMP1
A1O		AO	AMP1 output
P2.1/		DB/	GPIO, configurable as INT1 input
C2P/		AI/	CMP2 positive input
A2P/	48	AI/	AMP2 positive input
AD8/		AI/	Input of ADC channel 8
HAL2S		DI	Hall-IC2 logic level input after function switching

2.2 FU6812L2 LQFP48 Pinout Diagram

Figure 2-1 Pinout Diagram of FU6812L2 LQFP48



2.3 FU6812N2 QFN32 Pins

Table 2-2 Pin Descriptions of FU6812N2 QFN32

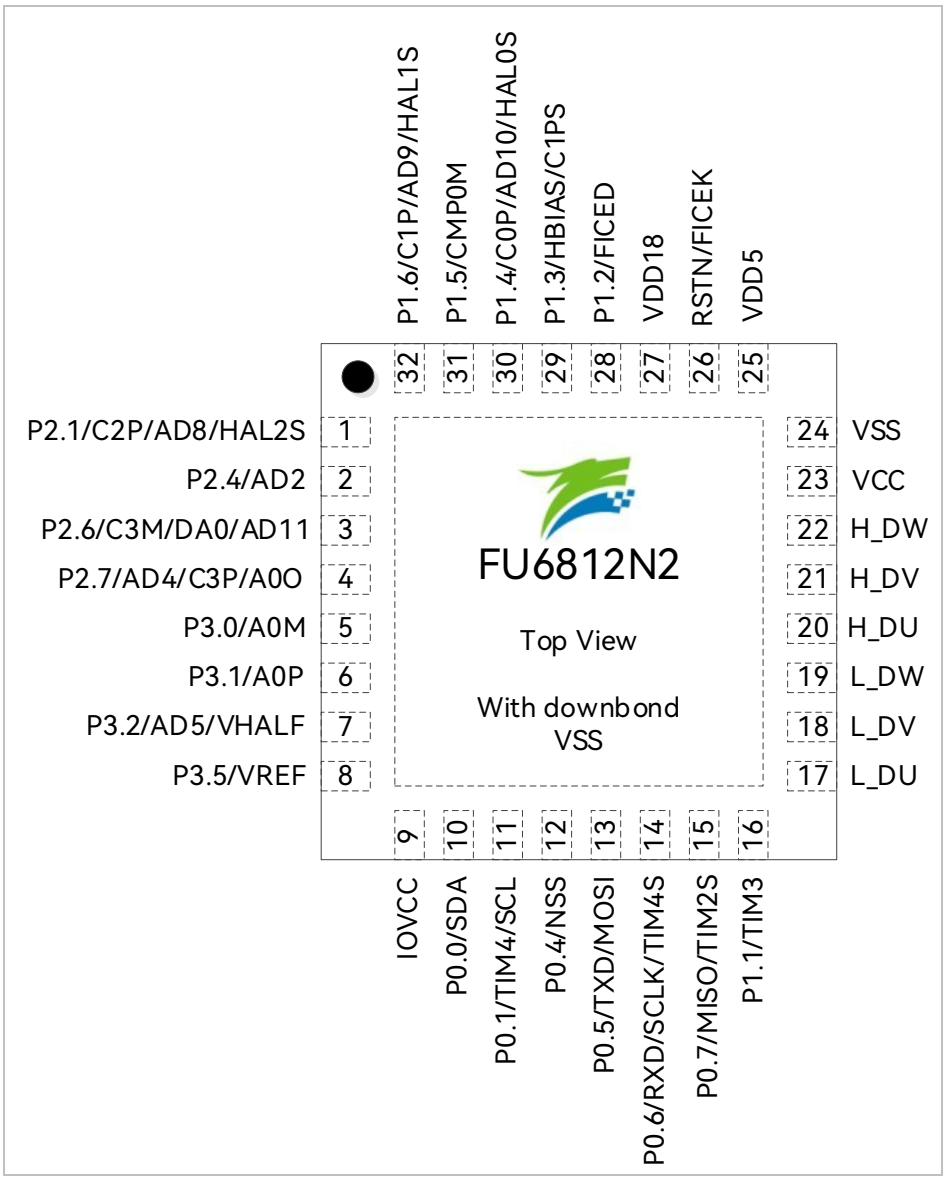
Pin	FU6812N2 QFN32	IO Type	Function Descriptions
P2.1/ C2P/ AD8/ HAL2S	1	DB/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP2 positive input Input of ADC channel 8 Hall2 logic level input after function switching
P2.4/ AD2	2	DB/ AI	GPIO, configurable as INT1 input Input of ADC channel 2 or bus voltage signal
P2.6/ C3M/ DA0/ AD11	3	DB/ AI/ AO/ AI	GPIO, configurable as INT1 input Over-current reference signal input; CMP3 negative input Internal DAC voltage, without Buffer output Input of ADC channel 11
P2.7/ AD4/ C3P/ A0O	4	DB/ AI/ AI/ AO	GPIO, configurable as INT1 input Input of ADC channel 4 for collecting the amplified bus current signal CMP3 positive input for bus current sampling to detect overcurrent AMP0 output, the voltage output after the bus current is amplified
P3.0/ A0M	5	DB/ AI	GPIO AMP0 negative input for amplifying the bus current signal
P3.1/ A0P	6	DB/ AI	GPIO AMP0 positive input for amplifying the bus current signal
P3.2/ AD5/ VHALF	7	DB/ AI/ AO	GPIO Input of ADC channel 5 or over-temperature signal input 1/2 VDD5 or 1/2 VREF output with an external 1μF capacitor
P3.5/ VREF	8	DB/ AI	GPIO ADC external VREF input or internal VREF output, with a 1μF~4.7 μF external capacitor
IOVCC	9	P	GPIO power supply, ranging from 3V to 5.5V, with a 1μF ~ 10μF capacitor connected to the ground. IOVCC ≤ VDD5. IOVCC supplies P0.x, P1.1, H_DU, H_DV, H_DW, L_DU, L_DV and L_DW only, and VDD5 supplies other GPIOs.
P0.0/ SDA	10	DB/ DB	GPIO, configurable as INT0 input I^2C SDA, configured as open-drain output

Pin	FU6812N2 QFN32	IO Type	Function Descriptions
P0.1/ TIM4/ SCL	11	DB/ DB/ DB	GPIO, configurable as INT0 input Timer4 input capture mode I²C SCL, configured as open-drain output
P0.4/ NSS	12	DB/ DB	GPIO, configurable as INT0 input SPI NSS
P0.5/ TXD/ MOSI	13	DB/ DO/ DB	GPIO, configurable as INT0 input UART1 TXD before function switching SPI MOSI, master output or slave input
P0.6/ RXD/ SCLK/ TIM4S	14	DB/ DI/ DB/ DB	GPIO, configurable as INT0 input UART1 RXD SPI SCLK Timer4 input capture mode or PWM output after function switching
P0.7/ MISO/ TIM2S	15	DB/ DB/ DB	GPIO SPI_MISO, master input or slave output Timer2 input capture mode or PWM output after function switching
P1.1/ TIM3	16	DB/ DB	GPIO, configurable as INT0/INT1 input Timer3 input capture mode
L_DU	17	DO	PWM output at low side of phase U
L_DV	18	DO	PWM output at low side of phase V
L_DW	19	DO	PWM output at low side of phase W
H_DU	20	DO	PWM output at high side of phase U
H_DV	21	DO	PWM output at high side of phase V
H_DW	22	DO	PWM output at high side of phase W
VCC	23	P	Power input, with an external filter capacitor of 10μF or above. 1. High-voltage single-power supply mode: External power supply 5V~24V is connected to VCC pin, and internal LDO supplies VDD5 voltage. 2. Low-voltage single-power supply mode: External power supply 3V~5.5V is connected to VDD5 pin, and VDD5 pin is shorted to VCC pin.
VSS	24	P	Ground

Pin	FU6812N2 QFN32	IO Type	Function Descriptions
VDD5	25	P	Mid-voltage power input or 5V LDO power output. See descriptions on VCC pin for power connection. It is connected with a 1μF~4.7μF external capacitor. When VCC > 5.5V, VDD5 outputs 5V. When VCC ranges in 3V ~ 5.5V, VCC pin is shorted to VDD5 pin.
RSTN/ FICEK	26	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VDD18	27	P	1.85V LDO output with an external 1μF ~ 4.7μF capacitor
P1.2/ FICED	28	DB/ DB	GPIO, configurable as INT1 input FICE data line
P1.3/ HBIAS/ C1PS	29	DB/ DO/ AI	GPIO, configurable as INT1 input Hall bias power supply, internally connected to VDD5 via a switch CMP1 positive input after function switching
P1.4/ C0P/ AD10/ HAL0S	30	DB/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP0 positive input Input of ADC channel 10 Hall0 logic level input after function switching
P1.5/ C0M	31	DB/ AI	GPIO, configurable as INT1 input CMP0 negative input
P1.6/ C1P/ AD9/ HAL1S	32	DB/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP1 positive input Input of ADC channel 9 Hall1 logic level input after function switching

2.4 FU6812N2 QFN32 Pinout Diagram

Figure 2-2 Pinout Diagram of FU6812N2 QFN32



2.5 FU6812S2 SSOP24 Pins

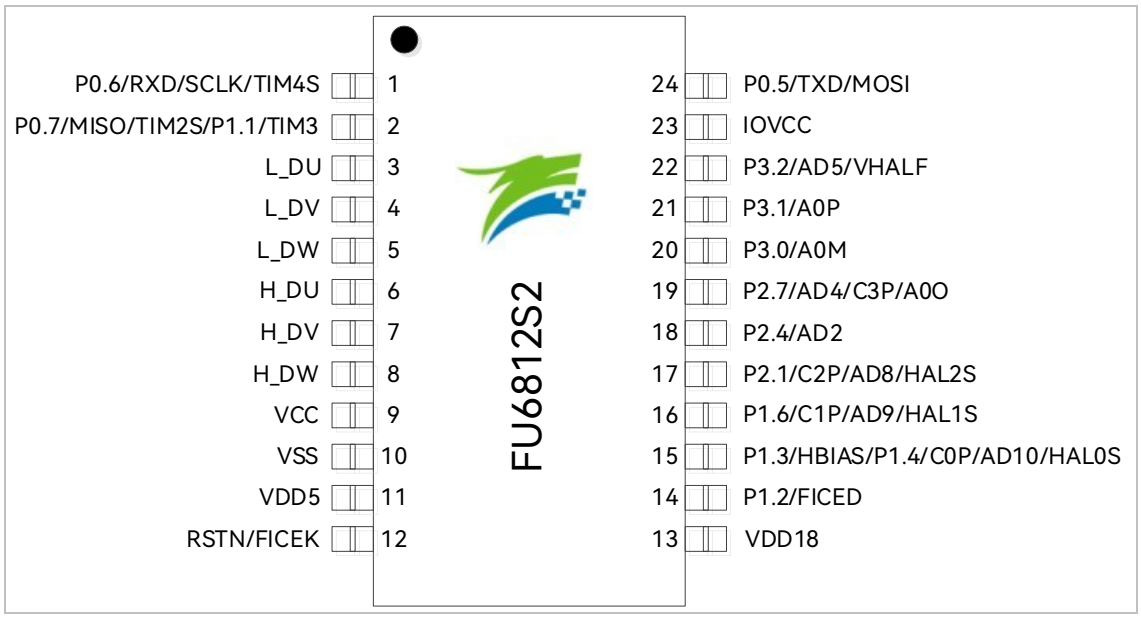
Table 2-3 Pin Descriptions of FU6812S2 SSOP24

Pin	FU6812S2 SSOP24	IO Type	Function Descriptions
P0.6/ RXD/ SCLK/ TIM4S	1	DB/ DI/ DB/ DB	GPIO, configurable as INT0 input UART1 RXD SPI SCLK Timer4 input capture mode or PWM output after function switching
P0.7/ MISO/ TIM2S/ P1.1/ TIM3	2	DB/ DB/ DB/ DB/ DB	GPIO SPI_MISO, master input or slave output Timer2 input capture mode or PWM output after function switching GPIO, configurable as INT0/INT1 input Timer3 input capture mode
L_DU	3	DO	PWM output at low side of phase U
L_DV	4	DO	PWM output at low side of phase V
L_DW	5	DO	PWM output at low side of phase W
H_DU	6	DO	PWM output at high side of phase U
H_DV	7	DO	PWM output at high side of phase V
H_DW	8	DO	PWM output at high side of phase W
VCC	9	P	Power input, with an external filter capacitor of 10μF or above. High-voltage single-power supply mode: External power supply 5V ~ 24V is connected to VCC pin, and internal LDO supplies VDD5 voltage.
VSS	10	P	Ground
VDD5	11	P	Mid-voltage power input or 5V LDO power output. See descriptions on VCC pin for power connection. It is connected with a 1μF~4.7μF external capacitor.
RSTN/ FICEK	12	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VDD18	13	P	1.85V LDO output with an external 1μF ~ 4.7μF capacitor
P1.2/ FICED	14	DB/ DB	GPIO, configurable as INT1 input FICE data line

Pin	FU6812S2 SSOP24	IO Type	Function Descriptions
P1.3/ HBIAS/ P1.4/ C0P/ AD10/ HAL0S	15	DB/ DO/ DB/ AI/ AI/ DI	GPIO P1.3, configurable as INT1 input Hall bias power supply, internally connected to VDD5 via a switch GPIO P1.4, configurable as INT1 input CMP0 positive input Input of ADC channel 10 Hall0 logic level input after function switching
P1.6/ C1P/ AD9/ HAL1S	16	DB/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP1 positive input Input of ADC channel 9 Hall1 logic level input after function switching
P2.1/ C2P/ AD8/ HAL2S	17	DB/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP2 positive input Input of ADC channel 8 Hall2 logic level input after function switching
P2.4/ AD2	18	DB/ AI	GPIO, configurable as INT1 input Input of ADC channel 2 or bus voltage signal
P2.7/ AD4/ C3P/ A0O	19	DB/ AI/ AI/ AO	GPIO, configurable as INT1 input Input of ADC channel 4 for collecting the amplified bus current signal CMP3 positive input for bus current sampling to detect overcurrent AMP0 output, the voltage output after the bus current is amplified
P3.0/ A0M	20	DB/ AI	GPIO AMP0 negative input for amplifying the bus current signal
P3.1/ A0P	21	DB/ AI	GPIO AMP0 positive input for amplifying the bus current signal
P3.2/ AD5/ VHALF	22	DB/ AI/ AO	GPIO Input of ADC channel 5 or over-temperature signal input 1/2 VDD5 or 1/2 VREF output with an external 1μF capacitor
IOVCC	23	P	GPIO power supply, ranging from 3V to 5.5V, with a 1μF ~ 10μF capacitor connected to the ground. IOVCC ≤ VDD5.
P0.5/ TXD/ MOSI	24	DB/ DO/ DB	GPIO, configurable as INT0 input UART1 TXD before function switching SPI MOSI, master output or slave input

2.6 FU6812S2 SSOP24 Pinout Diagram

Figure 2-3 Pinout Diagram of FU6812S2 SSOP24



2.7 FU6812V SSOP24 Pins

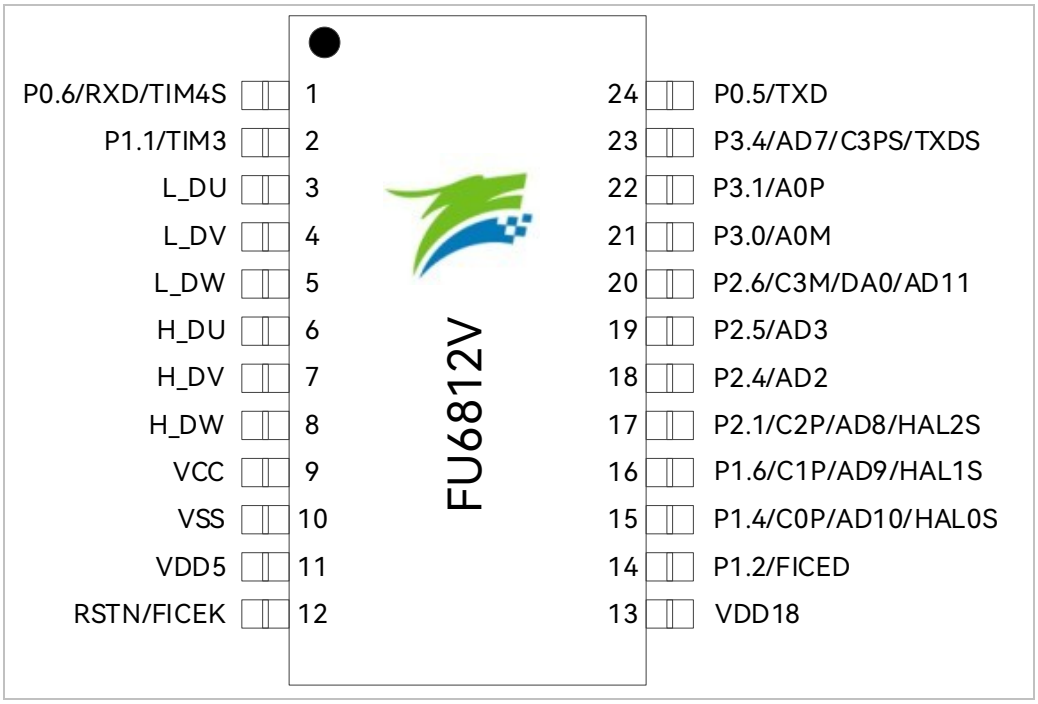
Table 2-4 Pin Descriptions of FU6812V SSOP24

Pin	FU6812V SSOP24	IO Type	Function Descriptions
P0.6/ RXD/ TIM4S	1	DB/ DI/ DB	GPIO, configurable as INT0 input UART1 RXD Timer4 input capture mode or PWM output after function switching
P1.1/ TIM3	2	DB/ DB	GPIO, configurable as INT0/INT1 input Timer3 input capture mode
L_DU	3	DO	PWM output at low side of phase U
L_DV	4	DO	PWM output at low side of phase V
L_DW	5	DO	PWM output at low side of phase W
H_DU	6	DO	PWM output at high side of phase U
H_DV	7	DO	PWM output at high side of phase V
H_DW	8	DO	PWM output at high side of phase W
VCC	9	P	Power input, with an external filter capacitor of 4.7μF or above. 1. High-voltage single-power supply mode: External power supply 5V ~ 24V is connected to VCC pin, and internal LDO supplies VDD5 voltage. 2. Low-voltage single-power supply mode: External power supply 3V~5.5V is connected to VDD5 pin, and VDD5 pin is shorted to VCC pin.
VSS	10	P	Ground
VDD5	11	P	Mid-voltage power input or 5V LDO power output. See descriptions on VCC pin for power connection. It is connected with a 1μF~4.7μF external capacitor.
RSTN/ FICEK	12	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VDD18	13	P	1.85V LDO output with an external 1μF ~ 4.7μF capacitor
P1.2/ FICED	14	DB/ DB	GPIO, configurable as INT1 input FICE data line
P1.4/ C0P/ AD10/ HAL0S	15	DB/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP0 positive input Input of ADC channel 10 Hall0 logic level input after function switching

Pin	FU6812V SSOP24	IO Type	Function Descriptions
P1.6/	16	DB/	GPIO, configurable as INT1 input
C1P/		AI/	CMP1 positive input
A1P/		AI/	AMP1 positive input
AD9/		AI/	Input of ADC channel 9
HAL1S		DI	Hall1 logic level input after function switching
P2.1/	17	DB/	GPIO, configurable as INT1 input
C2P/		AI/	CMP2 positive input
A2P/		AI/	AMP2 positive input
AD8/		AI/	Input of ADC channel 8
HAL2S		DI	Hall2 logic level input after function switching
P2.4/	18	DB/	GPIO, configurable as INT1 input
AD2		AI	Input of ADC channel 2 or bus voltage signal
P2.5/	19	DB/	GPIO, configurable as INT1 input
AD3		AI	Input of ADC channel 3
P2.6/	20	DB/	GPIO, configurable as INT1 input
C3M/		AI/	Over-current reference signal input; CMP3 negative input
DA0/		AO/	Internal DAC voltage, without Buffer output
AD11		AI	Input of ADC channel 11
P3.0/	21	DB/	GPIO
A0M		AI	AMP0 negative input for amplifying the bus current signal
P3.1/	22	DB/	GPIO
A0P		AI	AMP0 positive input for amplifying the bus current signal
P3.4/	23	DB	GPIO
AD7/		AI/	Input of ADC channel 7 or analog speed control input
C3PS/		AI/	CMP3 positive input after function switching
TXDS		DO	UART TXD output after function switching
P0.5/	24	DB/	GPIO, configurable as INT0 input
TXD		DO	UART1 TXD

2.8 FU6812V SSOP24 Pinout Diagram

Figure 2-4 Pinout Diagram of FU6812V SSOP24 Pinout Diagram



2.9 FU6861Q2 QFN56 Pins

Table 2-5 Pin Descriptions of FU6861Q2 QFN56

Pin	FU6812Q2 QFN56	IO Type	Function Descriptions
VSU	1	P	6N pre-driver U-phase input, as GND reference for U-phase high-side bootstrap
HU	2	DO	6N pre-driver high-side U-phase PWM output
VBU	3	P	6N pre-driver high-side U-phase bootstrap power supply
VSV	4	P	6N pre-driver V-phase input, as GND reference for V-phase high-side bootstrap
HV	5	DO	6N pre-driver high-side V-phase PWM output
VBV	6	P	6N pre-driver high-side V-phase bootstrap power supply
VSW	7	P	6N pre-driver W-phase input, as GND reference for W-phase high-side bootstrap
HW	8	DO	6N pre-driver high-side W-phase PWM output
VBW	9	P	6N pre-driver high-side W-phase bootstrap power supply
VCC	10	P	Power input. The voltage range is determined by VCC_MODE, with an external filter capacitor of 10μF or above. 1. High-voltage single-power supply mode: When VCC_MODE = 0, external power supply 5V~24V is connected to VCC pin, and internal LDO supplies VDD5 voltage. 2. Low-voltage single-power supply mode: When VCC_MODE = 1, external power supply 3V~5.5V is connected to VDD5 pin, and VDD5 pin is shorted to VCC pin. 3. Dual-power supply mode: When VCC_MODE = 1, external power supply 1 (5V~36V) is connected to VCC pin, and external power supply 2 (5V) is connected to VDD5 pin.
VSS	11	P	Ground
VDD5	12	P	Mid-voltage power input or 5V LDO power output is determined by VCC_MODE. See descriptions on VCC pin for power connection. It is connected with a 1μF~4.7μF external capacitor. When VCC_MODE = 0, internal LDO outputs 5V power supply. When VCC_MODE = 1, 3V~5.5V external power is supplied.
VCC_MODE	13	DI	Power supply mode control. See descriptions on VCC pin for details.

Pin	FU6812Q2 QFN56	IO Type	Function Descriptions
RSTN/	14	DI/	Input of external reset, with built-in pull-up resistor
FICEK		DI	FICE clock line
VDD18	15	P	1.85V LDO output with an external 1μF ~ 4.7μF capacitor
VSS	16	P	Ground
P1.2/	17	DB/	GPIO, configurable as INT1 input
FICED		DB	FICE data line
P1.3/	18	DB/	GPIO, configurable as INT1 input
HBIAS/		DO/	Hall bias power supply, internally connected to VDD5 via a switch
C1PS		AI	CMP1 positive input after function switching
P1.4/	19	DB/	GPIO, configurable as INT1 input
C0P/		AI/	CMP0 positive input
AD10/		AI/	Input of ADC channel 10
HAL0S		DI	Hall0 logic level input after function switching
P1.5/	20	DB/	GPIO, configurable as INT1 input
C0M		AI	CMP0 negative input
P1.6/	21	DB/	GPIO, configurable as INT1 input
C1P/		AI/	CMP1 positive input
A1P/		AI/	AMP1 positive input
AD9/		AI/	Input of ADC channel 9
HAL1S		DI	Hall1 logic level input after function switching
P1.7/	22	DB/	GPIO, configurable as INT1 input
C1M/		AI/	CMP1 negative input
A1M		AI	AMP1 negative input
P2.0/	23	DB/	GPIO, configurable as INT1 input
AD0/		AI/	Input of ADC channel 0 for collecting amplified signals from AMP1
A1O		AO	AMP1 output
P2.1/	24	DB/	GPIO, configurable as INT1 input
C2P/		AI/	CMP2 positive input
A2P/		AI/	AMP2 positive input for voltage signals generated by AMP2
AD8/		AI/	Input of ADC channel 8
HAL2S		DI	Hall2 logic level input after function switching
P2.2/	25	DB/	GPIO, configurable as INT1 input
C2M/		AI/	CMP2 negative input
A2M		AI	AMP2 negative input

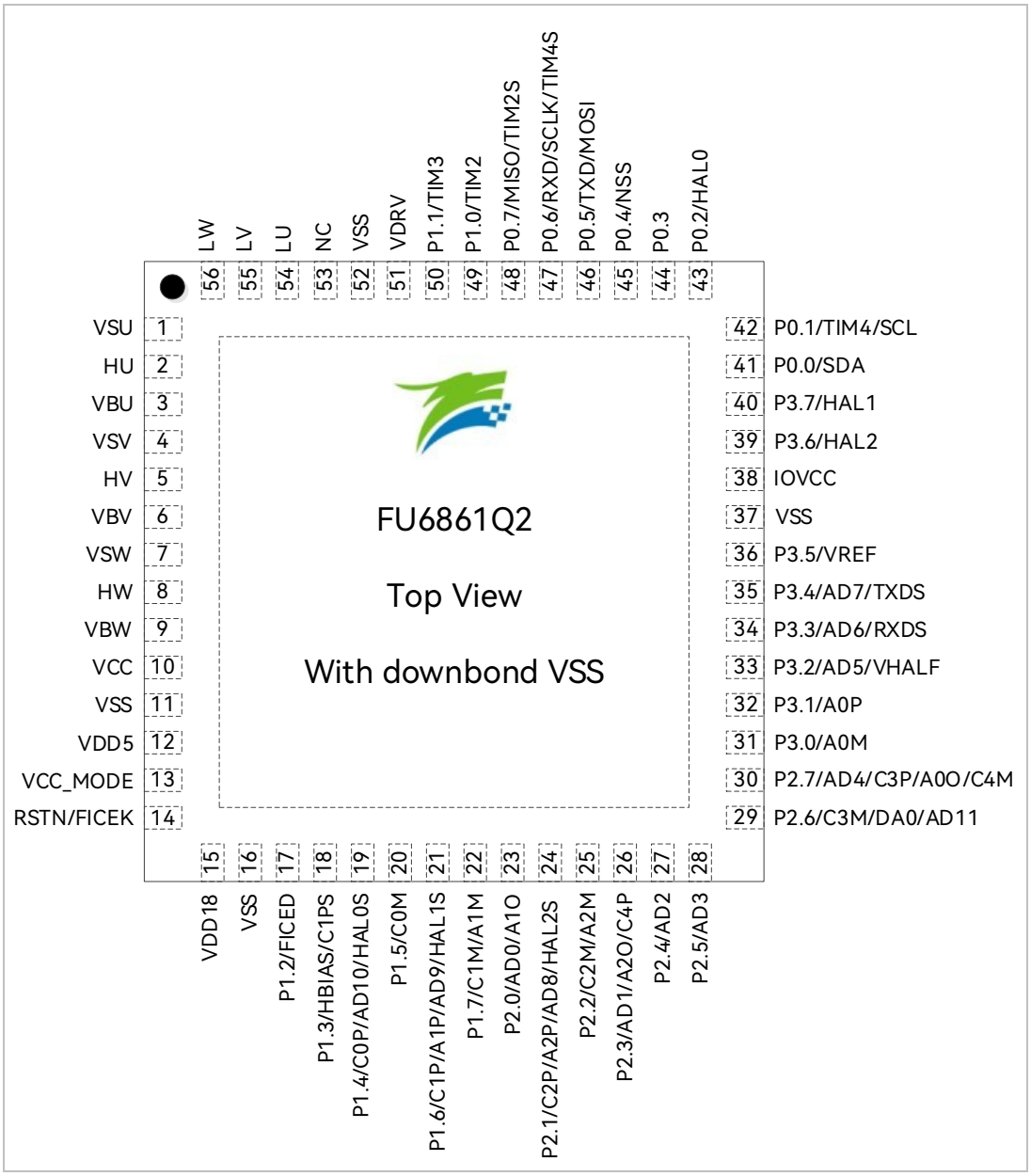
Pin	FU6812Q2 QFN56	IO Type	Function Descriptions
P2.3/ AD1/ A2O/ C4P	26	DB/ AI/ AO/ AI	GPIO, configurable as INT1 input Input of ADC channel 1 for collecting amplified signals from AMP2 AMP2 output CMP4 positive input
P2.4/ AD2	27	DB/ AI	GPIO, configurable as INT1 input Input of ADC channel 2 or bus voltage signal
P2.5/ AD3	28	DB/ AI	GPIO, configurable as INT1 input Input of ADC channel 3
P2.6/ C3M/ DA0/ AD11	29	DB/ AI/ AO/ AI	GPIO, configurable as INT1 input Over-current reference signal input; CMP3 negative input Internal DAC voltage, without Buffer output Input of ADC channel 11
P2.7/ AD4/ C3P/ A0O/ C4M	30	DB/ AI/ AI/ AO/ AI	GPIO, configurable as INT1 input Input of ADC channel 4 for collecting the amplified bus current signal CMP3 positive input for bus current sampling to detect overcurrent AMP0 output, the voltage output after the bus current is amplified CMP4 negative input
P3.0/ A0M	31	DB/ AI	GPIO AMP0 negative input for amplifying the bus current signal
P3.1/ A0P	32	DB/ AI	GPIO AMP0 positive input for amplifying the bus current signal
P3.2/ AD5/ VHALF	33	DB/ AI/ AO	GPIO Input of ADC channel 5 or over-temperature signal input 1/2 VDD5 or 1/2 VREF output with an external 1μF capacitor
P3.3/ AD6/ RXDS	34	DB/ AI/ DB	GPIO Input of ADC channel 6 UART RXD input in two-wire mode or TXD output/RXD input in single-wire mode after function switching
P3.4/ AD7/ TXDS	35	DB AI/ DO	GPIO Input of ADC channel 7 or analog speed control input UART TXD output after function switching
P3.5/ VREF	36	DB/ AI	GPIO ADC external VREF input or internal VREF output, with a 1μF~4.7μF external capacitor
VSS	37	P	Ground

Pin	FU6812Q2 QFN56	IO Type	Function Descriptions
IOVCC	38	P	GPIO power supply, ranging from 3V to 5.5V, with a 1μF ~ 10μF capacitor connected to the ground. IOVCC ≤ VDD5. IOVCC supplies P3.7 ~ 6, P0.x and P1.1 ~ 0 only, and VDD5 supplies other GPIOs.
P3.6/ HAL2	39	DB/ DI	GPIO Hall2 logic level input
P3.7/ HAL1	40	DB/ DI	GPIO Hall1 logic level input
P0.0/ SDA	41	DB/ DB	GPIO, configurable as INT0 input I²C SDA, configured as open-drain output
P0.1/ TIM4/ SCL	42	DB/ DB/ DB	GPIO, configurable as INT0 input Timer4 input capture mode I²C SCL, configured as open-drain output
P0.2/ HAL0	43	DB/ DI	GPIO, configurable as INT0 input Hall0 logic level input
P0.3	44	DB	GPIO, configurable as INT0 input
P0.4/ NSS	45	DB/ DB	GPIO, configurable as INT0 input SPI NSS
P0.5/ TXD/ MOSI	46	DB/ DO/ DB	GPIO, configurable as INT0 input UART1 TXD before function switching SPI MOSI, master output or slave input
P0.6/ RXD/ SCLK/ TIM4S	47	DB/ DI/ DB/ DB	GPIO, configurable as INT0 input UART1 RXD SPI SCLK Timer4 input capture mode or PWM output after function switching
P0.7/ MISO/ TIM2S	48	DB/ DB/ DB	GPIO SPI_MISO, master input or slave output Timer2 input capture mode or PWM output after function switching
P1.0/ TIM2	49	DB/ DB	GPIO, configurable as INT1 input Timer2 input capture mode or PWM output before function switching
P1.1/ TIM3	50	DB/ DB	GPIO, configurable as INT0/INT1 input Timer3 input capture mode
VDRV	51	P	6N pre-driver power supply, 7V~18V, with an external 1μF ~ 10μF capacitor
VSS	52	P	Ground

Pin	FU6812Q2 QFN56	IO Type	Function Descriptions
Not connected	53		Not connected
LU	54	DO	6N pre-driver low-side U-phase PWM output
LV	55	DO	6N pre-driver low-side V-phase PWM output
LW	56	DO	6N pre-driver low-side W-phase PWM output

2.10 FU6861Q2 QFN56 Pinout Diagram

Figure 2-5 Pinout Diagram of FU6861Q2 QFN56



2.11 FU6861L2 LQFP48 Pins

Table 2-6 Pin Descriptions of FU6861L2

Pin	FU6861L2 LQFP48	IO Type	Function Descriptions
P2.3/ AD1/ A2O/ C4P	1	DB/ AI/ AO/ AI	GPIO, configurable as INT1 input Input of ADC channel 1 for collecting amplified signals from AMP2 AMP2 output CMP4 positive input
P2.4/ AD2	2	DB/ AI	GPIO, configurable as INT1 input Input of ADC channel 2 or bus voltage signal
P2.6/ C3M/ DA0/ AD11	3	DB/ AI/ AO/ AI	GPIO, configurable as INT1 input Over-current reference signal input; CMP3 negative input Internal DAC voltage, without Buffer output Input of ADC channel 11
P2.7/ AD4/ C3P/ A0O/ C4M	4	DB/ AI/ AI/ AO/ AI	GPIO, configurable as INT1 input Input of ADC channel 4 for collecting the amplified bus current signal CMP3 positive input for bus current sampling to detect overcurrent AMP0 output, the voltage output after the bus current is amplified CMP4 negative input
P3.0/ A0M	5	DB/ AI	GPIO AMP0 negative input for amplifying the bus current signal
P3.1/ A0P	6	DB/ AI	GPIO AMP0 positive input for amplifying the bus current signal
P3.2/ AD5/ VHALF	7	DB/ AI/ AO	GPIO Input of ADC channel 5 or over-temperature signal input 1/2 VDD5 or 1/2 VREF output with an external 1μF capacitor
P3.3/ AD6/ RXDS	8	DB/ AI/ DB	GPIO Input of ADC channel 6 UART RXD input in two-wire mode or TXD output/RXD input in single-wire mode after function switching
P3.4/ AD7/ TXDS	9	DB AI/ DO	GPIO Input of ADC channel 7 or analog speed control input UART TXD output after function switching
P3.5/ VREF	10	DB/ AI	GPIO ADC external VREF input or internal VREF output, with a 1μF~4.7μF external capacitor

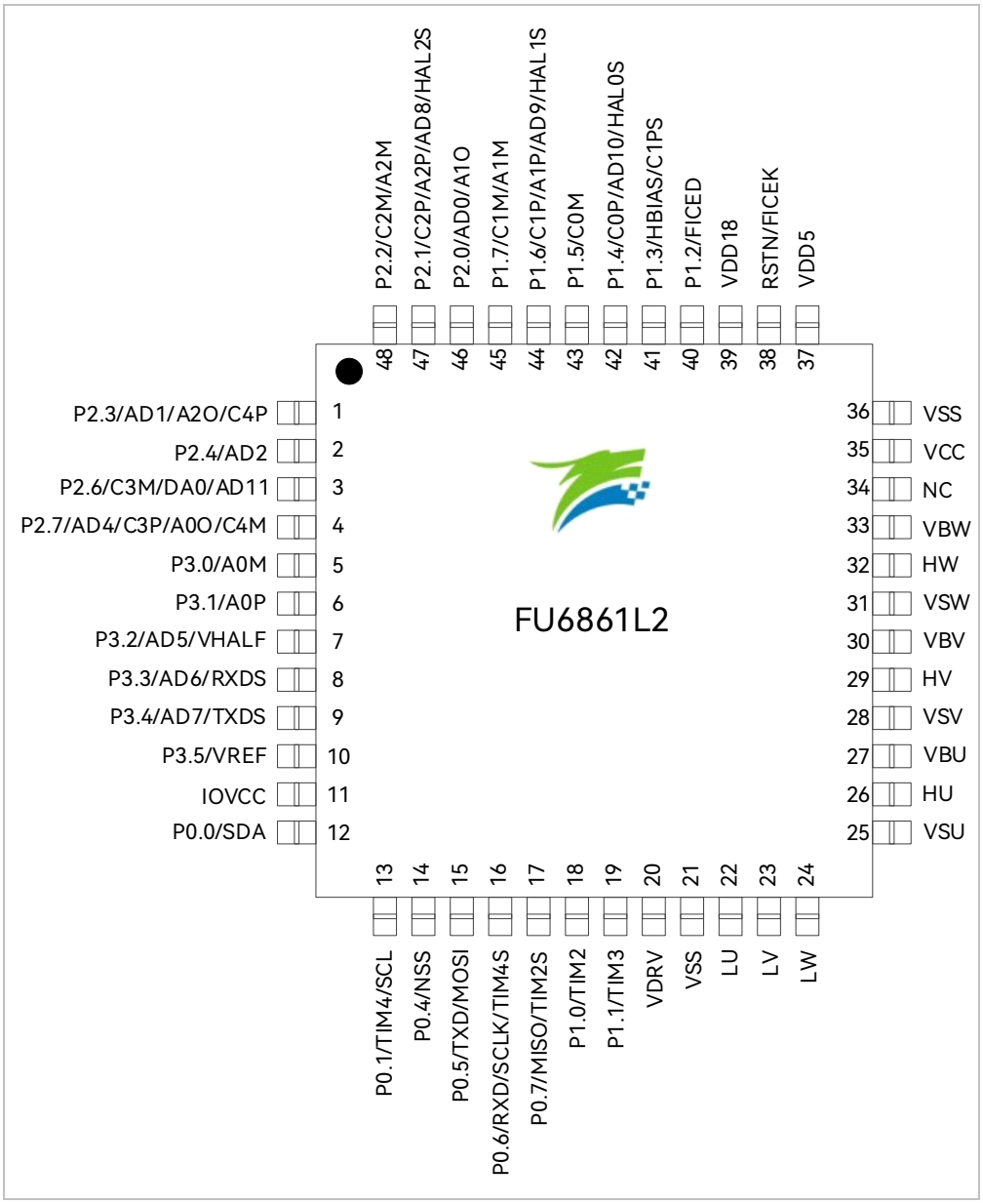
Pin	FU6861L2 LQFP48	IO Type	Function Descriptions
IOVCC	11	P	GPIO power supply, ranging from 3V to 5.5V, with a 1μF ~ 10μF capacitor connected to the ground. IOVCC ≤ VDD5.
P0.0/ SDA	12	DB/ DB	GPIO, configurable as INT0 input I²C SDA, configured as open-drain output
P0.1/ TIM4/ SCL	13	DB/ DB/ DB	GPIO, configurable as INT0 input Timer4 input capture mode I²C SCL, configured as open-drain output
P0.4/ NSS	14	DB/ DB	GPIO, configurable as INT0 input SPI NSS
P0.5/ TXD/ MOSI	15	DB/ DO/ DB	GPIO, configurable as INT0 input UART1 TXD before function switching SPI MOSI, master output or slave input
P0.6/ RXD/ SCLK/ TIM4S	16	DB/ DI/ DB/ DB	GPIO, configurable as INT0 input UART1 RXD SPI SCLK Timer4 input capture mode or PWM output after function switching
P0.7/ MISO/ TIM2S	17	DB/ DB/ DB	GPIO SPI_MISO, master input or slave output Timer2 input capture mode or PWM output after function switching
P1.0/ TIM2	18	DB/ DB	GPIO, configurable as INT1 input Timer2 input capture mode or PWM output before function switching
P1.1/ TIM3	19	DB/ DB	GPIO, configurable as INT0/INT1 input Timer3 input capture mode
VDRV	20	P	6N pre-driver power supply, 7V~18V, with an external 1μF ~ 10μF capacitor
VSS	21	P	Ground
LU	22	DO	6N pre-driver low-side U-phase PWM output
LV	23	DO	6N pre-driver low-side V-phase PWM output
LW	24	DO	6N pre-driver low-side W-phase PWM output
VSU	25	P	6N pre-driver U-phase input, as GND reference for U-phase high-side bootstrap
HU	26	DO	6N pre-driver high-side U-phase PWM output
VBU	27	P	6N pre-driver high-side U-phase bootstrap power supply
VSV	28	P	6N pre-driver V-phase input, as GND reference for V-phase high-side bootstrap

Pin	FU6861L2 LQFP48	IO Type	Function Descriptions
HV	29	DO	6N pre-driver high-side V-phase PWM output
VBV	30	P	6N pre-driver high-side V-phase bootstrap power supply
VSW	31	P	6N pre-driver W-phase input, as GND reference for W-phase high-side bootstrap
HW	32	DO	6N pre-driver high-side W-phase PWM output
VBW	33	P	6N pre-driver high-side W-phase bootstrap power supply
Not connected	34	-	Not connected
VCC	35	P	Power input. The voltage range is determined by VCC_MODE, with an external filter capacitor of 10μF or above.
VSS	36	P	Ground
VDD5	37	P	Mid-voltage power input or 5V LDO power output is determined by VCC_MODE. See descriptions on VCC pin for power connection. It is connected with a 1μF~4.7μF external capacitor.
RSTN/ FICEK	38	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VDD18	39	P	1.85V LDO output with an external 1μF ~ 4.7μF capacitor
P1.2/ FICED	40	DB/ DB	GPIO, configurable as INT1 input FICE data line
P1.3/ HBIAS/ C1PS	41	DB/ DO/ AI	GPIO, configurable as INT1 input Hall bias power supply, internally connected to VDD5 via a switch CMP1 positive input after function switching
P1.4/ C0P/ AD10/ HAL0S	42	DB/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP0 positive input Input of ADC channel 10 Hall0 logic level input after function switching
P1.5/ C0M	43	DB/ AI	GPIO, configurable as INT1 input CMP0 negative input
P1.6/ C1P/ A1P/ AD9/ HAL1S	44	DB/ AI/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP1 positive input AMP1 positive input Input of ADC channel 9 Hall1 logic level input after function switching
P1.7/ C1M/ A1M	45	DB/ AI/ AI	GPIO, configurable as INT1 input CMP1 negative input AMP1 negative input

Pin	FU6861L2 LQFP48	IO Type	Function Descriptions
P2.0/	46	DB/	GPIO, configurable as INT1 input
AD0/		AI/	Input of ADC channel 0 for collecting amplified signals from AMP1
A1O		AO	AMP1 output
P2.1/	47	DB/	GPIO, configurable as INT1 input
C2P/		AI/	CMP2 positive input
A2P/		AI/	AMP2 positive input for voltage signals generated by AMP2
AD8/		AI/	Input of ADC channel 8
HAL2S		DI	Hall2 logic level input after function switching
P2.2/	48	DB/	GPIO, configurable as INT1 input
C2M/		AI/	CMP2 negative input
A2M		AI	AMP2 negative input

2.12 FU6861L2 LQFP48 Pinout Diagram

Figure 2-6 Pinout Diagram of FU6861L2 LQFP48



2.13 FU6861N2/FU6861NF2 QFN40 Pins

Table 2-7 Pin Descriptionsb of FU6861N2/ FU6861NF2 QFN40

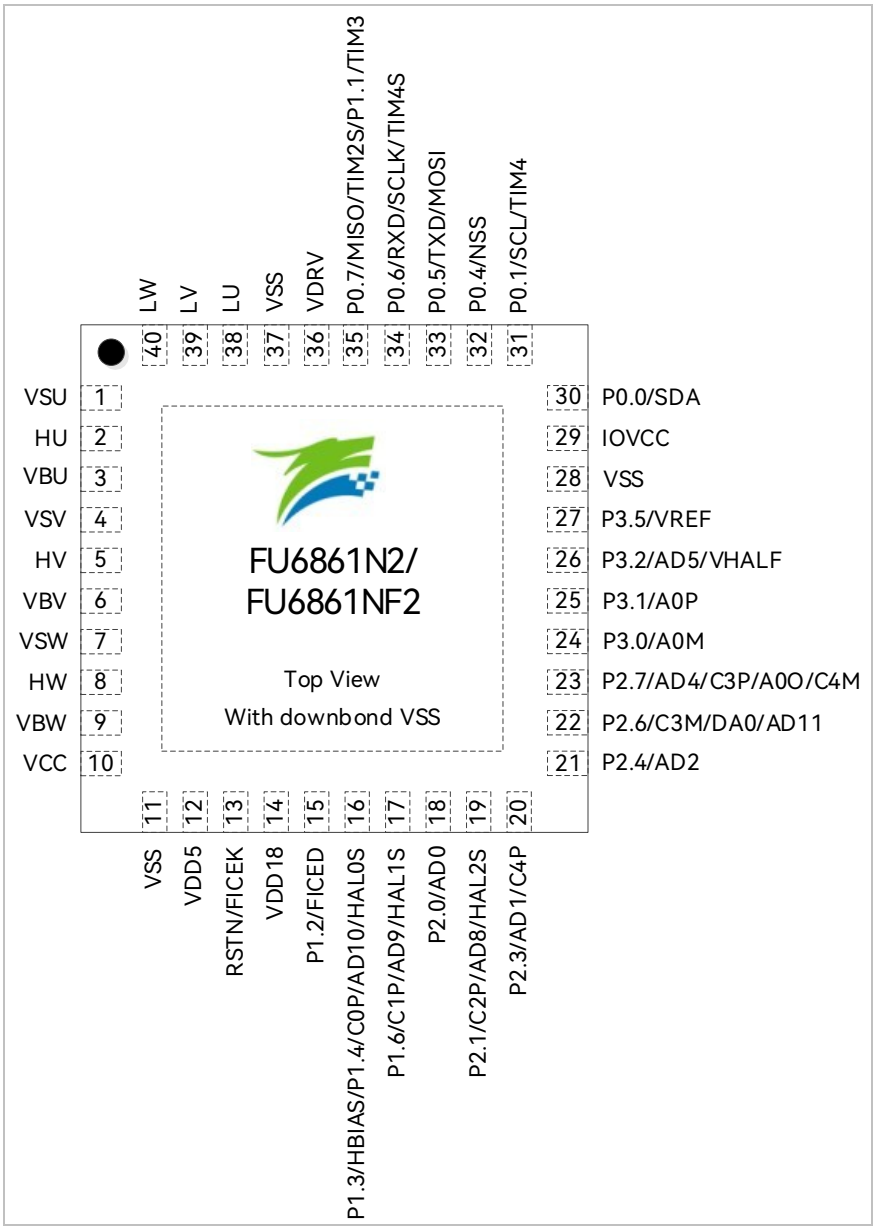
Pin	FU6861N2/ FU6861NF2 QFN40	IO Type	Function Descriptions
VSU	1	P	6N pre-driver U-phase input, as GND reference for U-phase high-side bootstrap
HU	2	DO	6N pre-driver high-side U-phase PWM output
VBU	3	P	6N pre-driver high-side U-phase bootstrap power supply
VSV	4	P	6N pre-driver V-phase input, as GND reference for V-phase high-side bootstrap
HV	5	DO	6N pre-driver high-side V-phase PWM output
VBV	6	P	6N pre-driver high-side V-phase bootstrap power supply
VSW	7	P	6N pre-driver W-phase input, as GND reference for W-phase high-side bootstrap
HW	8	DO	6N pre-driver high-side W-phase PWM output
VBW	9	P	6N pre-driver high-side W-phase bootstrap power supply
VCC	10	P	Power input. The voltage range is determined by VCC_MODE, with an external filter capacitor of 10μF or above.
VSS	11	P	Ground
VDD5	12	P	Mid-voltage power input or 5V LDO power output is determined by VCC_MODE. See descriptions on VCC pin for power connection. It is connected with a 1μF~4.7μF external capacitor.
RSTN/ FICEK	13	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VDD18	14	P	1.85V LDO output with an external 1μF ~ 4.7μF capacitor
P1.2/ FICED	15	DB/ DB	GPIO, configurable as INT1 input FICE data line
P1.3/ HBIAS/ P1.4/ C0P/ AD10/ HAL0S	16	DB/ DO/ DB/ AI/ AI/ DI	GPIO Hall bias power supply, internally connected to VDD5 via a switch GPIO, configurable as INT1 input CMP0 positive input Input of ADC channel 10 Hall0 logic level input after function switching

Pin	FU6861N2/ FU6861NF2 QFN40	IO Type	Function Descriptions
P1.6/ C1P/ AD9/ HAL1S	17	DB/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP1 positive input Input of ADC channel 9 Hall1 logic level input after function switching
P2.0/ AD0	18	DB/ AI	GPIO, configurable as INT1 input Input of ADC channel 0 for collecting amplified signals from AMP1
P2.1/ C2P/ AD8/ HAL2S	19	DB/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP2 positive input Input of ADC channel 8 Hall2 logic level input after function switching
P2.3/ AD1/ C4P	20	DB/ AI/ AI	GPIO, configurable as INT1 input Input of ADC channel 1 for collecting amplified signals from AMP2 CMP4 positive input
P2.4/ AD2	21	DB/ AI	GPIO, configurable as INT1 input Input of ADC channel 2 or bus voltage signal
P2.6/ C3M/ DA0/ AD11	22	DB/ AI/ AO/ AI	GPIO, configurable as INT1 input Over-current reference signal input; CMP3 negative input Internal DAC voltage, without Buffer output Input of ADC channel 11
P2.7/ AD4/ C3P/ A0O/ C4M	23	DB/ AI/ AI/ AO/ AI	GPIO, configurable as INT1 input Input of ADC channel 4 for collecting the amplified bus current signal CMP3 positive input for bus current sampling to detect overcurrent AMP0 output, the voltage output after the bus current is amplified CMP4 negative input
P3.0/ A0M	24	DB/ AI	GPIO AMP0 negative input for amplifying the bus current signal
P3.1/ A0P	25	DB/ AI	GPIO AMP0 positive input for amplifying the bus current signal
P3.2/ AD5/ VHALF	26	DB/ AI/ AO	GPIO Input of ADC channel 5 or over-temperature signal input 1/2 VDD5 or 1/2 VREF output with an external 1μF capacitor
P3.5/ VREF	27	DB/ AI	GPIO ADC external VREF input or internal VREF output, with a 1μF~4.7μF external capacitor

Pin	FU6861N2/ FU6861NF2 QFN40	IO Type	Function Descriptions
VSS	28	P	Ground
IOVCC	29	P	GPIO power supply, ranging from 3V to 5.5V, with a 1μF ~ 10μF capacitor connected to the ground. IOVCC ≤ VDD5.
P0.0/ SDA	30	DB/ DB	GPIO, configurable as INT0 input I²C SDA, configured as open-drain output
P0.1/ TIM4/ SCL	31	DB/ DB/ DB	GPIO, configurable as INT0 input Timer4 input capture mode or PWM output I²C SCL, configured as open-drain output
P0.4/ NSS	32	DB/ DB	GPIO, configurable as INT0 input SPI NSS
P0.5/ TXD/ MOSI	33	DB/ DO/ DB	GPIO, configurable as INT0 input UART1 TXD before function switching SPI MOSI, master output or slave input
P0.6/ RXD/ SCLK/ TIM4S	34	DB/ DI/ DB/ DB	GPIO, configurable as INT0 input UART1 RXD SPI SCLK Timer4 input capture mode or PWM output after function switching
P0.7/ MISO/ TIM2S/ P1.1/ TIM3	35	DB/ DB/ DB/ DB/ DB	GPIO P0.7 SPI_MISO, master input or slave output Timer2 input capture mode or PWM output after function switching GPIO P1.1, configurable as INT0/INT1 input Timer3 input capture mode
VDRV	36	P	6N pre-driver power supply, 7V~18V, with an external 1μF ~ 10μF capacitor
VSS	37	P	Ground
LU	38	DO	6N pre-driver low-side U-phase PWM output
LV	39	DO	6N pre-driver low-side V-phase PWM output
LW	40	DO	6N pre-driver low-side W-phase PWM output

2.14 FU6861N2/FU6861NF2 QFN40 Pinout Diagram

Figure 2-7 Pinout Diagram of FU6861N2/FU6861NF2 QFN40



2.15 FU6862L LQFP48 Pins

Table 2-8 Pin Descriptions of FU6862L LQFP48

Pin	FU6862L LQFP48	IO Type	Function Descriptions
P2.1/ C2P/ A2P/ AD8/ HAL2S	1	DB/ AI/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP2 positive input AMP2 positive input for voltage signals generated by AMP2 Input of ADC channel 8 Hall2 logic level input after function switching
P2.2/ C2M/ A2M	2	DB/ AI/ AI	GPIO, configurable as INT1 input CMP2 negative input AMP2 negative input
P2.4/ AD2	3	DB/ AI	GPIO, configurable as INT1 input Input of ADC channel 2 or bus voltage signal
P2.6/ C3M/ DA0/ AD11	4	DB/ AI/ AO/ AI	GPIO, configurable as INT1 input Over-current reference signal input; CMP3 negative input Internal DAC voltage, without Buffer output Input of ADC channel 11
P2.7/ AD4/ C3P/ A0O/ C4M	5	DB/ AI/ AI/ AO/ AI	GPIO, configurable as INT1 input Input of ADC channel 4 for collecting the amplified bus current signal CMP3 positive input for bus current sampling to detect overcurrent AMP0 output, the voltage output after the bus current is amplified CMP4 negative input
P3.0/ A0M	6	DB/ AI	GPIO AMP0 negative input for amplifying the bus current signal
P3.1/ A0P	7	DB/ AI	GPIO AMP0 positive input for amplifying the bus current signal
P3.3/ AD6/ RXDS	8	DB/ AI/ DB	GPIO Input of ADC channel 6 UART RXD input in two-wire mode or TXD output/RXD input in single-wire mode after function switching
P3.4/ AD7/ C3PS TXDS	9	DB AI/ AI DO	GPIO Input of ADC channel 7 or analog speed control input CMP3 positive input after function switching UART TXD output after function switching

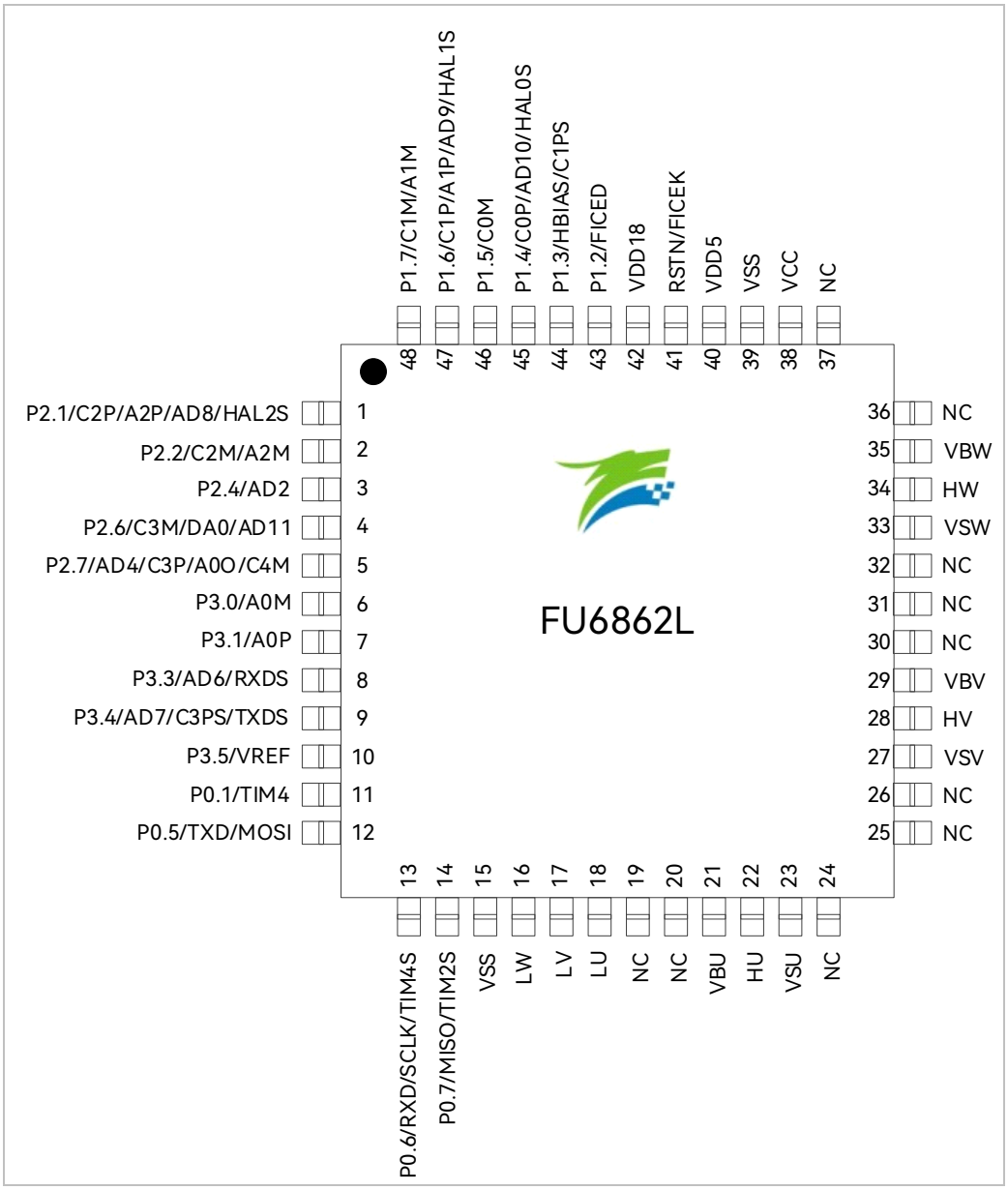
Pin	FU6862L LQFP48	IO Type	Function Descriptions
P3.5/ VREF	10	DB/ AI	GPIO ADC external VREF input or internal VREF output, with a 1μF~4.7μF external capacitor
P0.1/ TIM4	11	DB/ DB	GPIO, configurable as INT0 input Timer4 input capture mode
P0.5/ TXD/ MOSI	12	DB/ DO/ DB	GPIO, configurable as INT0 input UART1 TXD before function switching SPI MOSI, master output or slave input
P0.6/ RXD/ SCLK/ TIM4S	13	DB/ DI/ DB/ DB	GPIO, configurable as INT0 input UART1 RXD SPI SCLK Timer4 input capture mode or PWM output after function switching
P0.7/ MISO/ TIM2S	14	DB/ DB/ DB	GPIO SPI_MISO, master input or slave output Timer2 input capture mode or PWM output after function switching
VSS	15	P	Ground
LW	16	DO	6N pre-driver low-side W-phase PWM output
LV	17	DO	6N pre-driver low-side V-phase PWM output
LU	18	DO	6N pre-driver low-side U-phase PWM output
Not connected	19	-	Not connected
Not connected	20	-	Not connected
VBU	21	P	6N pre-driver high-side U-phase bootstrap power supply
HU	22	DO	6N pre-driver high-side U-phase PWM output
VSU	23	P	6N pre-driver U-phase input, as GND reference for U-phase high-side bootstrap
Not connected	24	-	Not connected
Not connected	25	-	Not connected
Not connected	26	-	Not connected
VSV	27	P	6N pre-driver V-phase input, as GND reference for V-phase high-side bootstrap
HV	28	DO	6N pre-driver high-side V-phase PWM output

Pin	FU6862L LQFP48	IO Type	Function Descriptions
VBV	29	P	6N pre-driver high-side V-phase bootstrap power supply
Not connected	30	-	Not connected
Not connected	31	-	Not connected
Not connected	32	-	Not connected
VSW	33	P	6N pre-driver W-phase input, as GND reference for W-phase high-side bootstrap
HW	34	DO	6N pre-driver high-side W-phase PWM output
VBW	35	P	6N pre-driver high-side W-phase bootstrap power supply
Not connected	36	-	Not connected
Not connected	37	-	Not connected
VCC	38	P	Power input, with an external filter capacitor of 10μF or above. High-voltage single-power supply mode: External power supply 12V~20V is connected to VCC pin, and internal LDO supplies VDD5 voltage.
VSS	39	P	Ground
VDD5	40	P	Medium-voltage power input or 5V LDO power output, with a 1μF ~4.7μF external capacitor. When VCC > 5.5V, VDD5 outputs 5V power supply.
RSTN/ FICEK	41	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VDD18	42	P	1.85V LDO output with an external 1μF ~ 4.7μF capacitor
P1.2/ FICED	43	DB/ DB	GPIO, configurable as INT1 input FICE data line
P1.3/ HBIAS/ C1PS	44	DB/ DO/ AI	GPIO, configurable as INT1 input Hall bias power supply, internally connected to VDD5 via a switch CMP1 positive input after function switching
P1.4/ C0P/ AD10/ HAL0S	45	DB/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP0 positive input Input of ADC channel 10 Hall0 logic level input after function switching

Pin	FU6862L LQFP48	IO Type	Function Descriptions
P1.5/	46	DB/	GPIO, configurable as INT1 input
C0M		AI	CMP0 negative input
P1.6/	47	DB/	GPIO, configurable as INT1 input
C1P/		AI/	CMP1 positive input
A1P/		AI/	AMP1 positive input
AD9/		AI/	Input of ADC channel 9
HAL1S		DI	Hall1 logic level input after function switching
P1.7/	48	DB/	GPIO, configurable as INT1 input
C1M/		AI/	CMP1 negative input
A1M		AI	AMP1 negative input

2.16 FU6862L LQFP48 Pinout Diagram

Figure 2-8 Pinout Diagram of FU6862L LQFP48



2.17 FU6862Q QFN48-38 Pins

Table 2-9 Pin Descriptions of FU6862Q QFN48-38

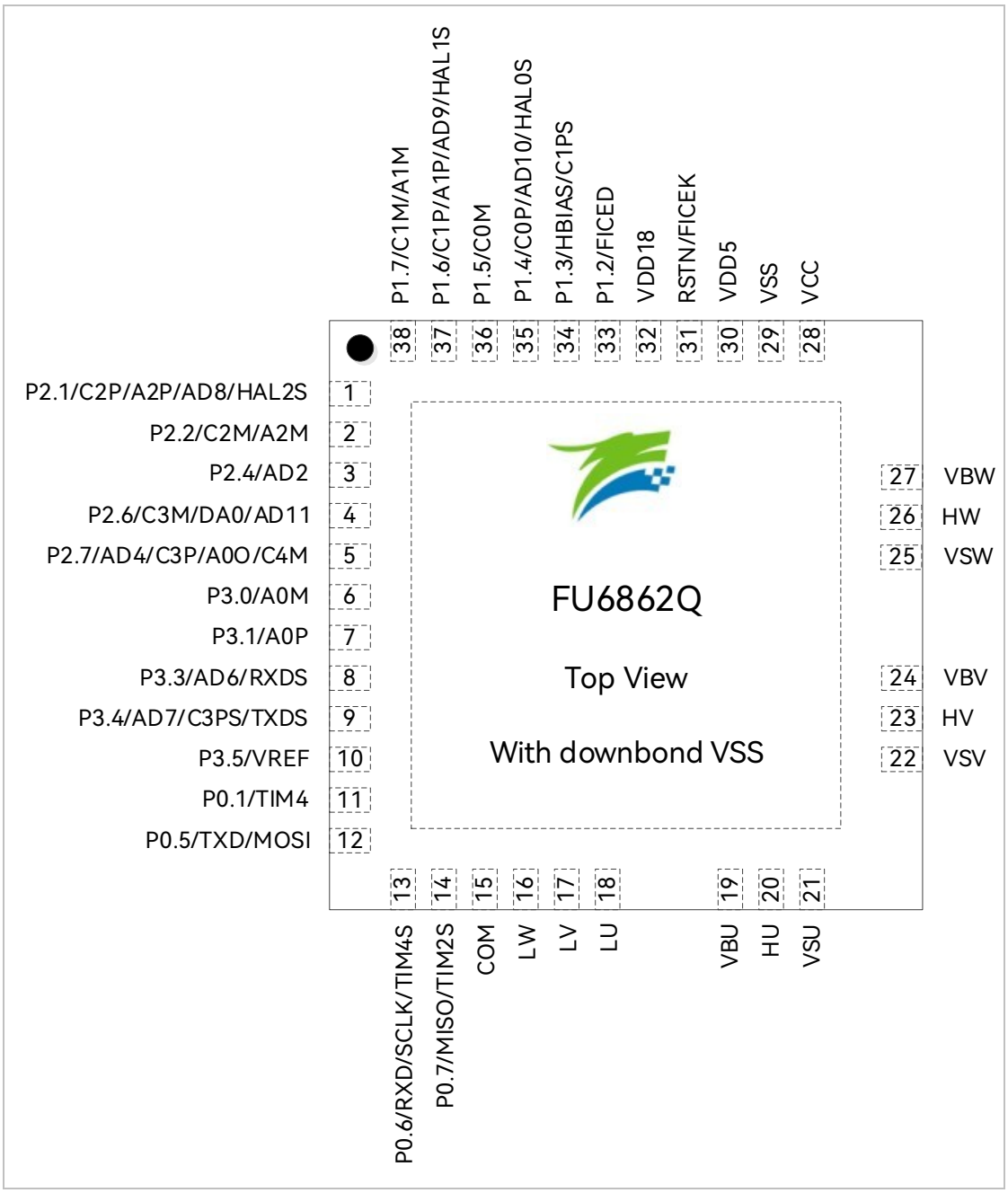
Pin	FU6862Q QFN48-38	IO Type	Function Descriptions
P2.1/ C2P/ A2P/ AD8/ HAL2S	1	DB/ AI/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP2 positive input AMP2 positive input for voltage signals generated by AMP2 Input of ADC channel 8 Hall2 logic level input after function switching
P2.2/ C2M/ A2M	2	DB/ AI/ AI	GPIO, configurable as INT1 input CMP2 negative input AMP2 negative input
P2.4/ AD2	3	DB/ AI	GPIO, configurable as INT1 input Input of ADC channel 2 or bus voltage signal
P2.6/ C3M/ DA0/ AD11	4	DB/ AI/ AO/ AI	GPIO, configurable as INT1 input Over-current reference signal input; CMP3 negative input Internal DAC voltage, without Buffer output Input of ADC channel 11
P2.7/ AD4/ C3P/ A0O/ C4M	5	DB/ AI/ AI/ AO/ AI	GPIO, configurable as INT1 input Input of ADC channel 4 for collecting the amplified bus current signal CMP3 positive input for bus current sampling to detect overcurrent AMP0 output, the voltage output after the bus current is amplified CMP4 negative input
P3.0/ A0M	6	DB/ AI	GPIO AMP0 negative input for amplifying the bus current signal
P3.1/ A0P	7	DB/ AI	GPIO AMP0 positive input for amplifying the bus current signal
P3.3/ AD6/ RXDS	8	DB/ AI/ DB	GPIO Input of ADC channel 6 UART RXD input in two-wire mode or TXD output/RXD input in single-wire mode after function switching
P3.4/ AD7/ C3PS/ TXDS	9	DB AI/ AI/ DO	GPIO Input of ADC channel 7 or analog speed control input CMP3 positive input after function switching UART TXD output after function switching

Pin	FU6862Q QFN48-38	IO Type	Function Descriptions
P3.5/ VREF	10	DB/ AI	GPIO ADC external VREF input or internal VREF output, with a 1μF~4.7μF external capacitor
P0.1/ TIM4	11	DB/ DB	GPIO, configurable as INT0 input Timer4 input capture mode
P0.5/ TXD/ MOSI	12	DB/ DO/ DB	GPIO, configurable as INT0 input UART1 TXD before function switching SPI MOSI, master output or slave input
P0.6/ RXD/ SCLK/ TIM4S	13	DB/ DI/ DB/ DB	GPIO, configurable as INT0 input UART1 RXD SPI SCLK Timer4 input capture mode or PWM output after function switching
P0.7/ MISO/ TIM2S	14	DB/ DB/ DB	GPIO SPI_MISO, master input or slave output Timer2 input capture mode or PWM output after function switching
VSS	15	P	Ground
LW	16	DO	6N pre-driver low-side W-phase PWM output
LV	17	DO	6N pre-driver low-side V-phase PWM output
LU	18	DO	6N pre-driver low-side U-phase PWM output
VBU	19	P	6N pre-driver high-side U-phase bootstrap power supply
HU	20	DO	6N pre-driver high-side U-phase PWM output
VSU	21	P	6N pre-driver U-phase input, as GND reference for U-phase high-side bootstrap
VSV	22	P	6N pre-driver V-phase input, as GND reference for V-phase high-side bootstrap
HV	23	DO	6N pre-driver high-side V-phase PWM output
VBV	24	P	6N pre-driver high-side V-phase bootstrap power supply
VSW	25	P	6N pre-driver W-phase input, as GND reference for W-phase high-side bootstrap
HW	26	DO	6N pre-driver high-side W-phase PWM output
VBW	27	P	6N pre-driver high-side W-phase bootstrap power supply
VCC	28	P	Power input, with an external filter capacitor of 10μF or above. High-voltage single-power supply mode: External power supply 12V~20V is connected to VCC pin, and internal LDO supplies VDD5 voltage.
VSS	29	P	Ground

Pin	FU6862Q QFN48-38	IO Type	Function Descriptions
VDD5	30	P	Medium-voltage power input or 5V LDO power output, with a 1μF ~4.7μF external capacitor. When VCC > 5.5V, VDD5 outputs 5V power supply.
RSTN/ FICEK	31	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VDD18	32	P	1.85V LDO output with an external 1μF ~ 4.7μF capacitor
P1.2/ FICED	33	DB/ DB	GPIO, configurable as INT1 input FICE data line
P1.3/ HBIAS/ C1PS	34	DB/ DO/ AI	GPIO, configurable as INT1 input Hall bias power supply, internally connected to VDD5 via a switch CMP1 positive input after function switching
P1.4/ C0P/ AD10/ HAL0S	35	DB/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP0 positive input Input of ADC channel 10 Hall0 logic level input after function switching
P1.5/ C0M	36	DB/ AI	GPIO, configurable as INT1 input CMP0 negative input
P1.6/ C1P/ A1P/ AD9/ HAL1S	37	DB/ AI/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP1 positive input AMP1 positive input Input of ADC channel 9 Hall1 logic level input after function switching
P1.7/ C1M/ A1M	38	DB/ AI/ AI	GPIO, configurable as INT1 input CMP1 negative input AMP1 negative input

2.18 FU6862Q QFN48-38 Pinout Diagram

Figure 2-9 Pinout Diagram of FU6862Q QFN48-38



2.19 FU6872P PLQFN32 Pins

Table 2-10 Pin Descriptions of FU6872P PLQFN32

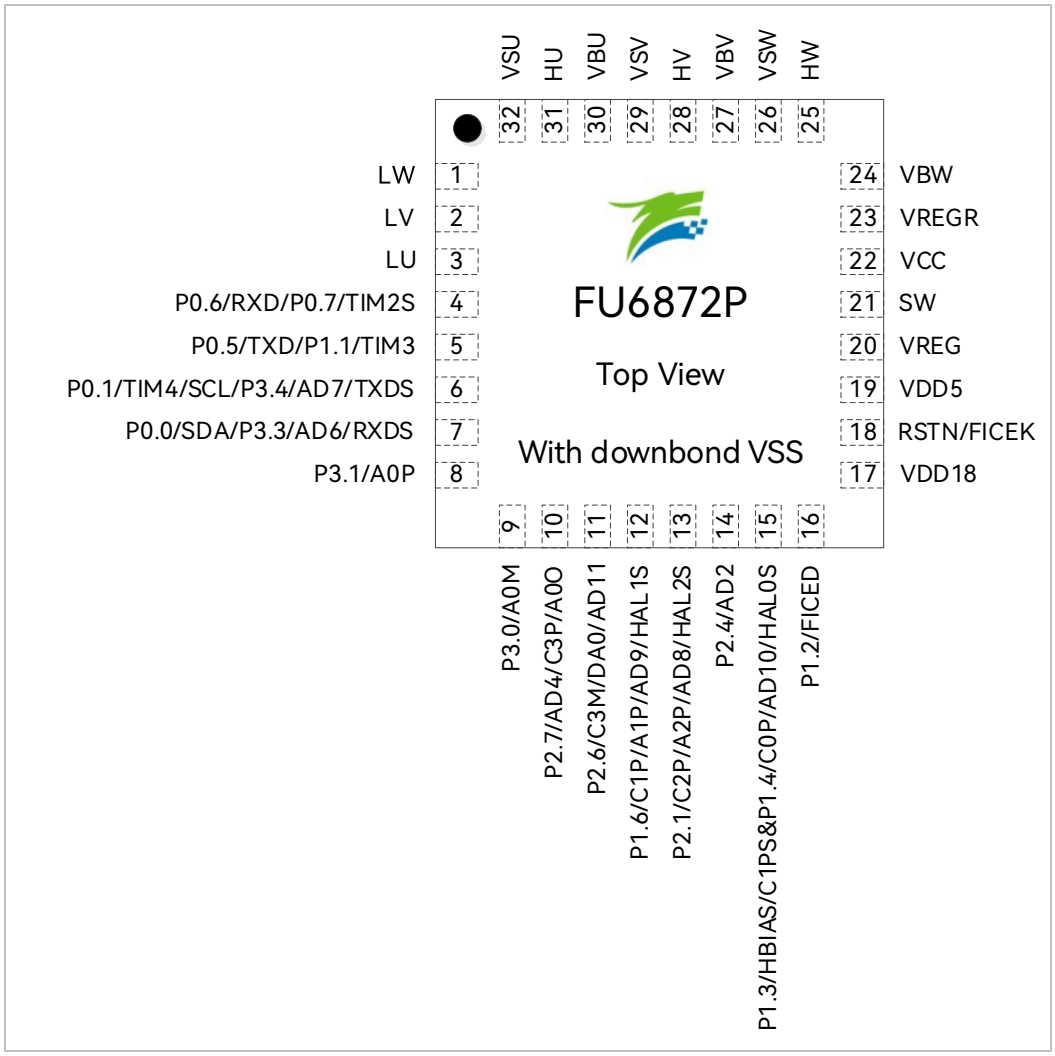
Pin	FU6872P PLQFN32	IO Type	Function Descriptions
LW	1	DO	6N pre-driver low-side W-phase PWM output
LV	2	DO	6N pre-driver low-side V-phase PWM output
LU	3	DO	6N pre-driver low-side U-phase PWM output
P0.6/ RXD/ P0.7/ TIM2S	4	DB/ DI/ DB/ DB	GPIO P0.6, configurable as INT0 input UART1 RXD GPIO P0.7 Timer2 input capture mode or PWM output after function switching
P0.5/ TXD/ P1.1/ TIM3	5	DB/ DO/ DB/ DB	GPIO, configurable as INT0 input UART1 TXD output GPIO, configurable as INT0/INT1 input Timer3 input capture mode
P0.1/ TIM4/ SCL/ P3.4/ AD7/ TXDS	6	DB/ DB/ DB/ DB/ AI/ DO	GPIO P0.1, configurable as INT0 input Timer4 input capture mode I²C SCL, configured as open-drain output GPIO P3.4 Input of ADC channel 7 or analog speed control input UART TXD output after function switching
P0.0/ SDA/ P3.3/ AD6/ RXDS	7	DB/ DB/ DB/ AI/ DB	GPIO P0.0, configurable as INT0 input I²C SDA, configured as open-drain output GPIO P3.3 Input of ADC channel 6 UART RXD input in two-wire mode or TXD output/RXD input in single-wire mode after function switching
P3.1/ A0P	8	DB/ AI	GPIO AMP0 positive input for amplifying the bus current signal
P3.0/ A0M	9	DB/ AI	GPIO AMP0 negative input for amplifying the bus current signal

Pin	FU6872P PLQFN32	IO Type	Function Descriptions
P2.7/ AD4/ C3P/ A0O	10	DB/ AI/ AI/ AO	GPIO, configurable as INT1 input Input of ADC channel 4 for collecting the amplified bus current signal CMP3 positive input for bus current sampling to detect overcurrent AMP0 output, the voltage output after the bus current is amplified
P2.6/ C3M/ DA0/ ADC11	11	DB/ AI/ AO/ AI	GPIO, configurable as INT1 input CMP3 negative input DAC0 output, without Buffer output Input of ADC channel 11
P1.6/ C1P/ A1P/ AD9/ HAL1S	12	AO/ AI/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP1 positive input AMP1 positive input Input of ADC channel 9 Hall-IC1 logic level input after function switching
P2.1/ C2P/ A2P/ AD8/ HAL2S	13	DB/ AI/ AI/ AI/ DI	GPIO, configurable as INT1 input CMP2 positive input AMP2 positive input Input of ADC channel 8 Hall-IC2 logic level input after function switching
P2.4/ AD2	14	DB/ AI	GPIO, configurable as INT1 input Input of ADC channel 2 or bus voltage signal
P1.3/ HBIAS/ C1PS/ P1.4/ C0P/ AD10/ HAL0S	15	DB/ DO/ AI/ DB/ AI/ AI/ DI	GPIO P1.3, configurable as INT1 input Hall bias power supply, internally connected to VDD5 via a switch CMP1 positive input after function switching GPIO P1.4, configurable as INT1 input CMP0 positive input Input of ADC channel 10 Hall-IC0 logic level input after function switching
P1.2/ FICED	16	DB/ DB	GPIO, configurable as INT1 input FICE data line
VDD18	17	P	Low-voltage power supply input or internal LDO outputs 1.85V power supply
RSTN/ FICEK	18	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VDD5	19	P	5V LDO output with a 1μF ~ 4.7μF external capacitor

Pin	FU6872P PLQFN32	IO Type	Function Descriptions
VREG	20	P	BUCK Output
SW	21	P	BUCK Switch Output
VCC	22	P	Power input, with an external filter capacitor of 10μF or above.
VREGR	23	P	VREG current limit voltage input signal with external 47Ω resistor connected to the VREG pin≥
VBW	24	P	6N pre-driver high-side W-phase bootstrap power supply
HW	25	DO	6N pre-driver high-side W-phase PWM output
VSW	26	P	6N pre-driver W-phase input, as GND reference for W-phase high-side bootstrap
VBV	27	P	6N pre-driver high-side V-phase bootstrap power supply
HV	28	DO	6N pre-driver high-side V-phase PWM output
VSV	29	P	6N pre-driver V-phase input, as GND reference for V-phase high-side bootstrap
VBU	30	P	6N pre-driver high-side U-phase bootstrap power supply
HU	31	DO	6N pre-driver high-side U-phase PWM output
VSU	32	P	6N pre-driver U-phase input, as GND reference for U-phase high-side bootstrap

2.20 FU6872P PLQFN32 Pinout Diagram

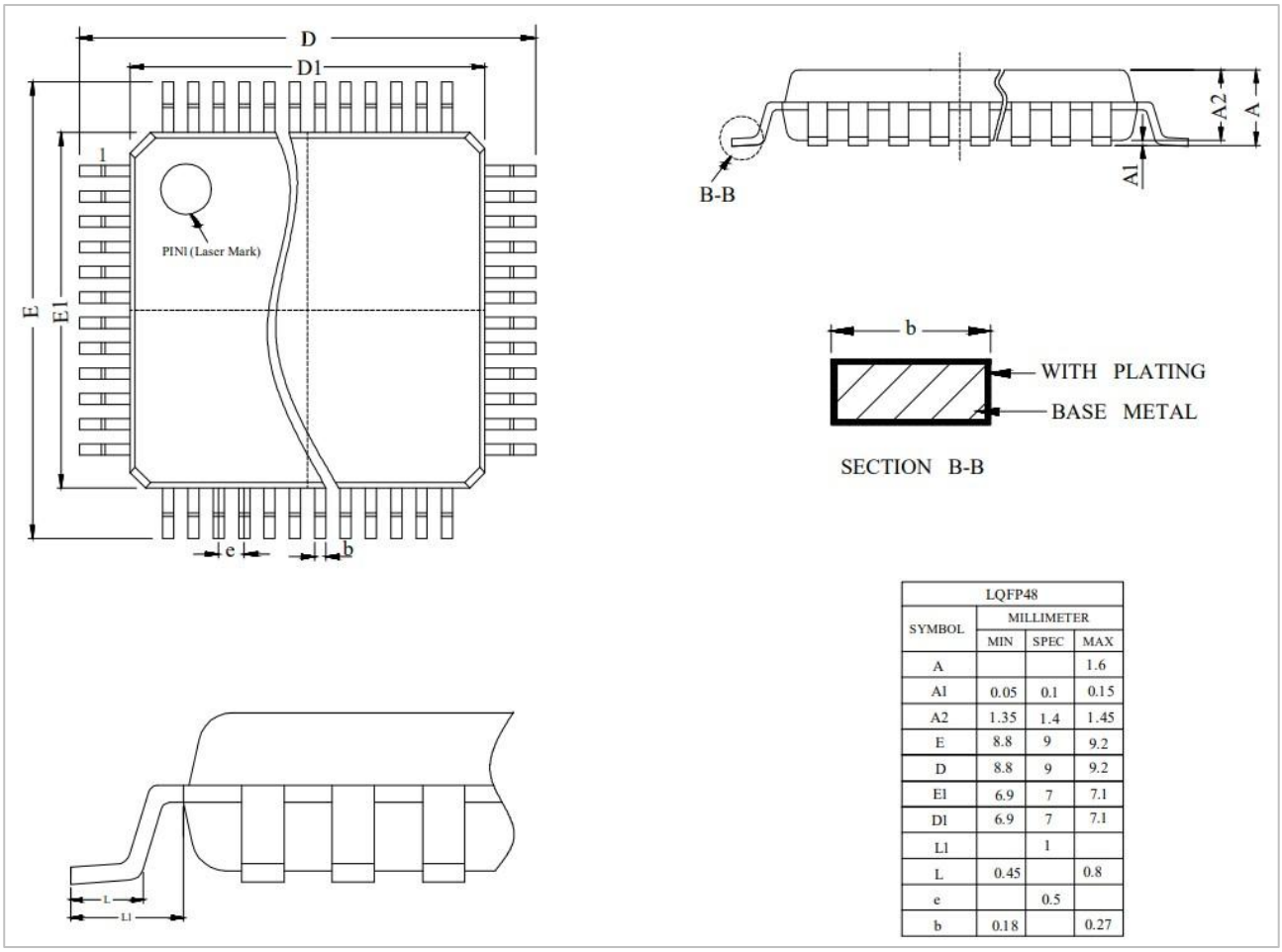
Figure 2-10 Pinout Diagram of FU6872P PLQFN32



3 Package Information

3.1 LQFP48_7X7(for FU6812L2, FU6861L2, FU6862L)

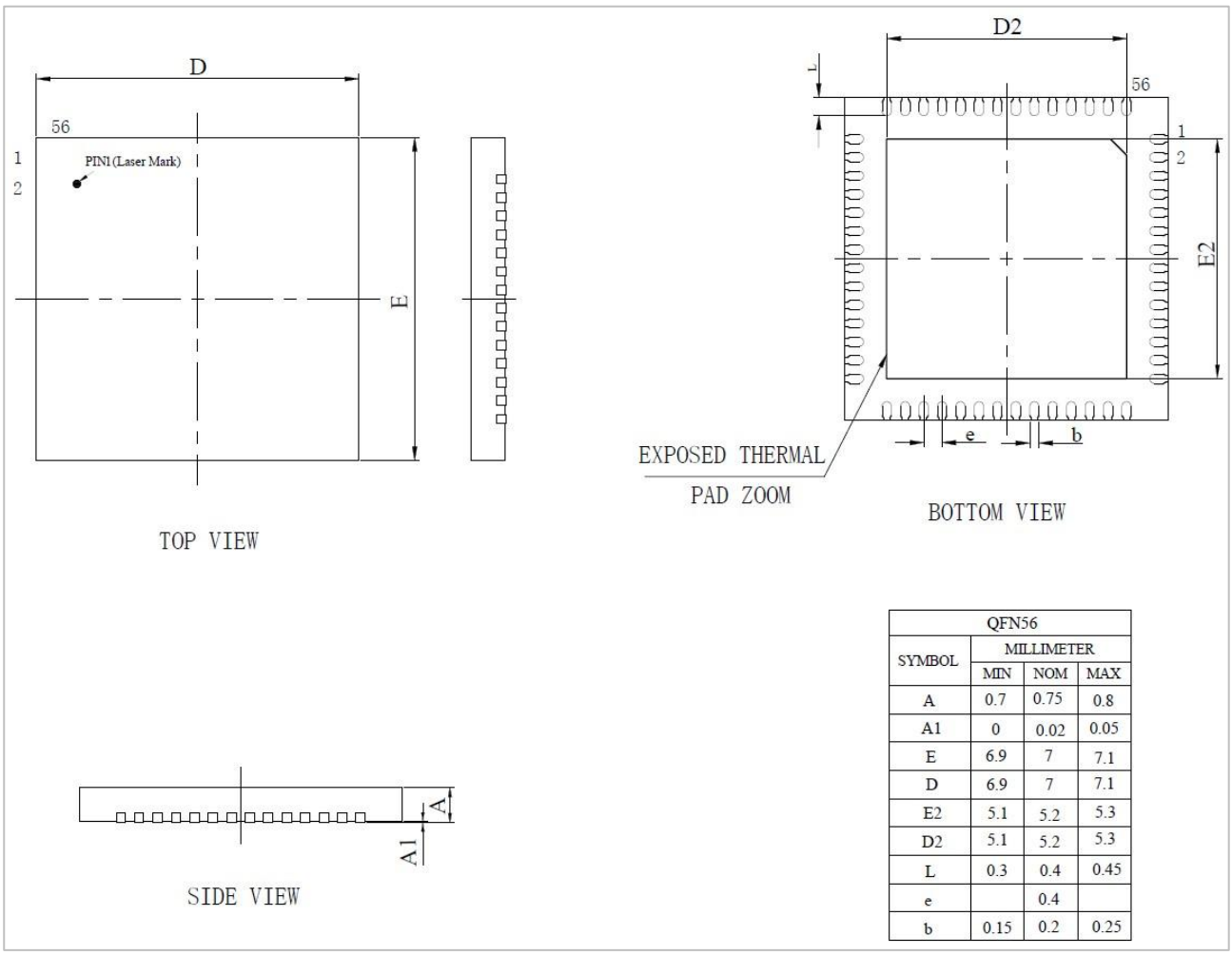
Figure 3-1 Package Drawings and Dimensions of LQFP48_7X7



LQFP48			
SYMBOL	MILLIMETER		
	MIN	SPEC	MAX
A			1.6
A1	0.05	0.1	0.15
A2	1.35	1.4	1.45
E	8.8	9	9.2
D	8.8	9	9.2
E1	6.9	7	7.1
D1	6.9	7	7.1
L1		1	
L	0.45		0.8
e		0.5	
b	0.18		0.27

3.2 QFN56_7X7(for FU6861Q2)

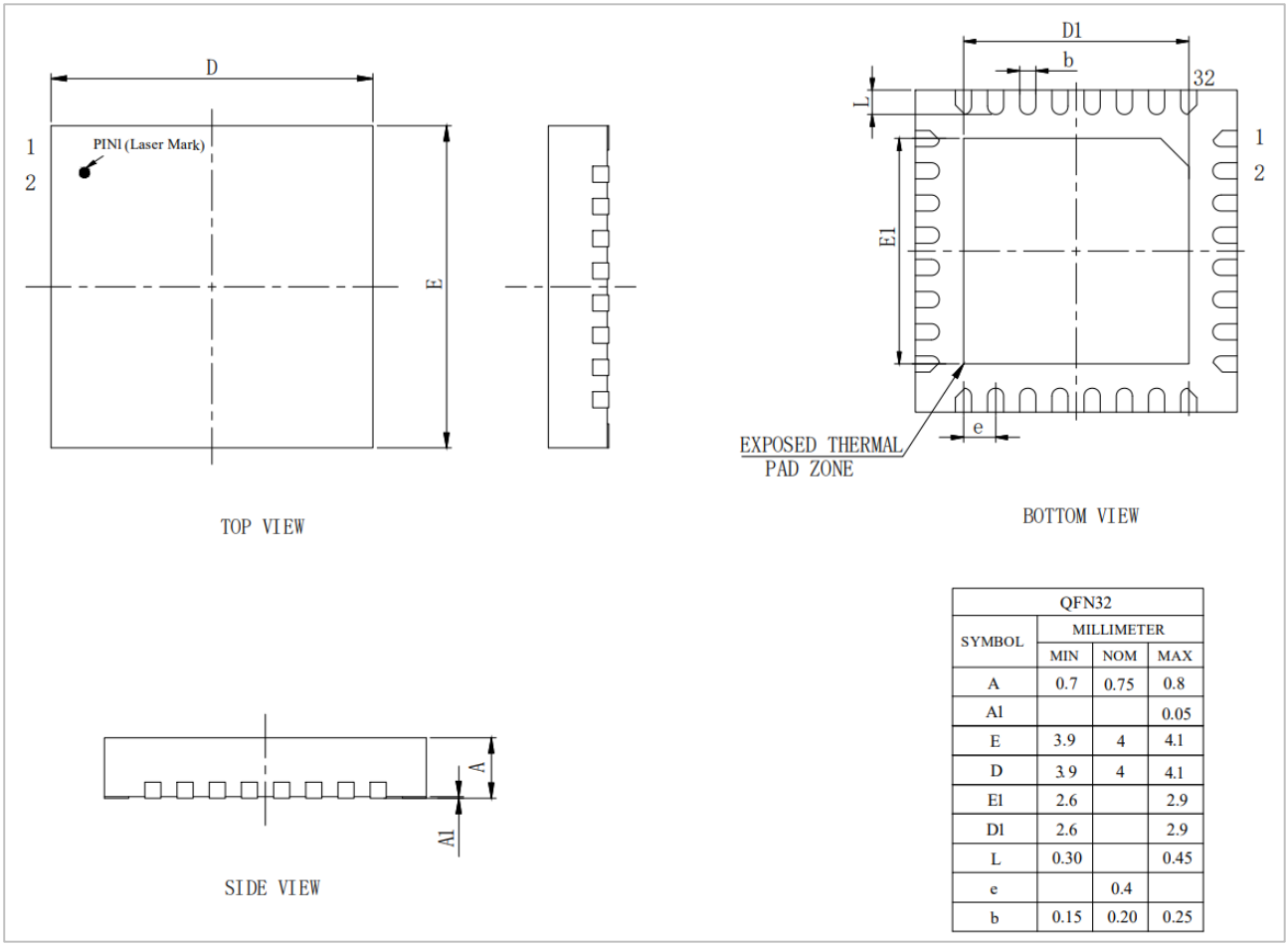
Figure 3-2 Package Drawings and Dimensions of QFN56_7X7



QFN56			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
E	6.9	7	7.1
D	6.9	7	7.1
E2	5.1	5.2	5.3
D2	5.1	5.2	5.3
L	0.3	0.4	0.45
e		0.4	
b	0.15	0.2	0.25

3.3 QFN32_4X4(for FU6812N2)

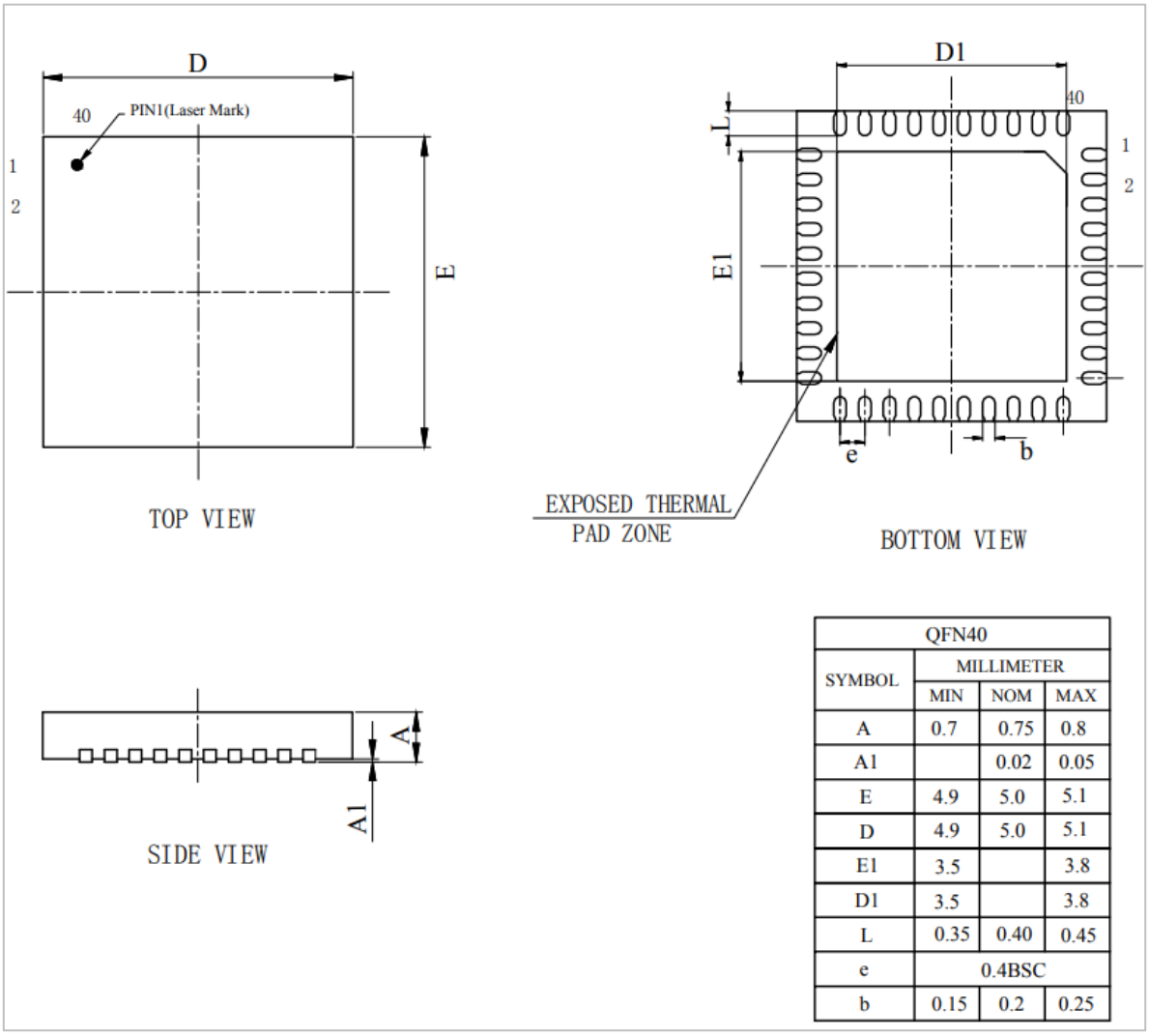
Figure 3-3 Package Drawings and Dimensions of QFN32_4X4



SYMBOL	QFN32 MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1			0.05
E	3.9	4	4.1
D	3.9	4	4.1
E1	2.6		2.9
D1	2.6		2.9
L	0.30		0.45
e		0.4	
b	0.15	0.20	0.25

3.4 QFN40_5X5(for FU6861N2/ FU6861NF2)

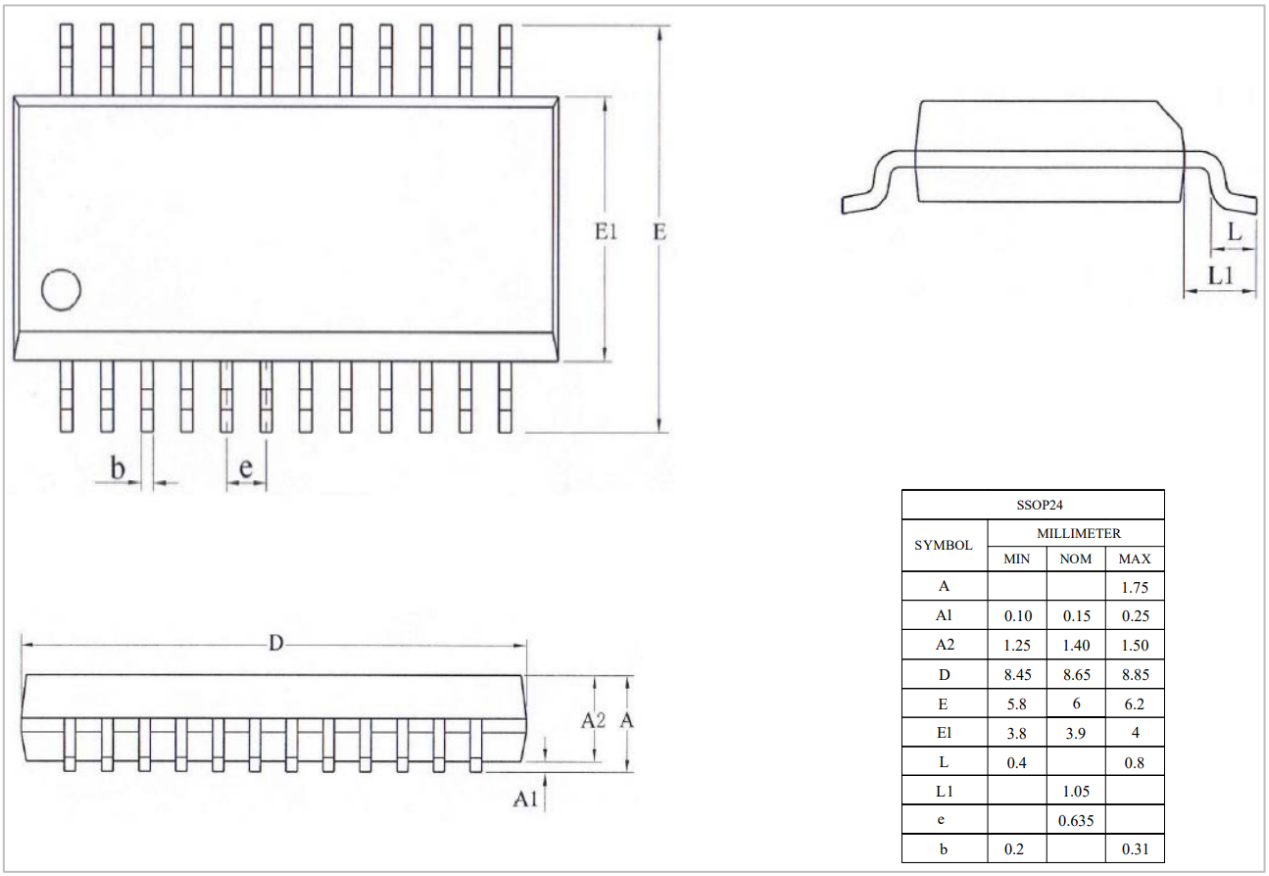
Figure 3-4 Package Drawings and Dimensions of QFN40_5X5



QFN40			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1		0.02	0.05
E	4.9	5.0	5.1
D	4.9	5.0	5.1
E1	3.5		3.8
D1	3.5		3.8
L	0.35	0.40	0.45
e	0.4BSC		
b	0.15	0.2	0.25

3.5 SSOP24_8.65X3.9(for FU6812S2 / FU6812V)

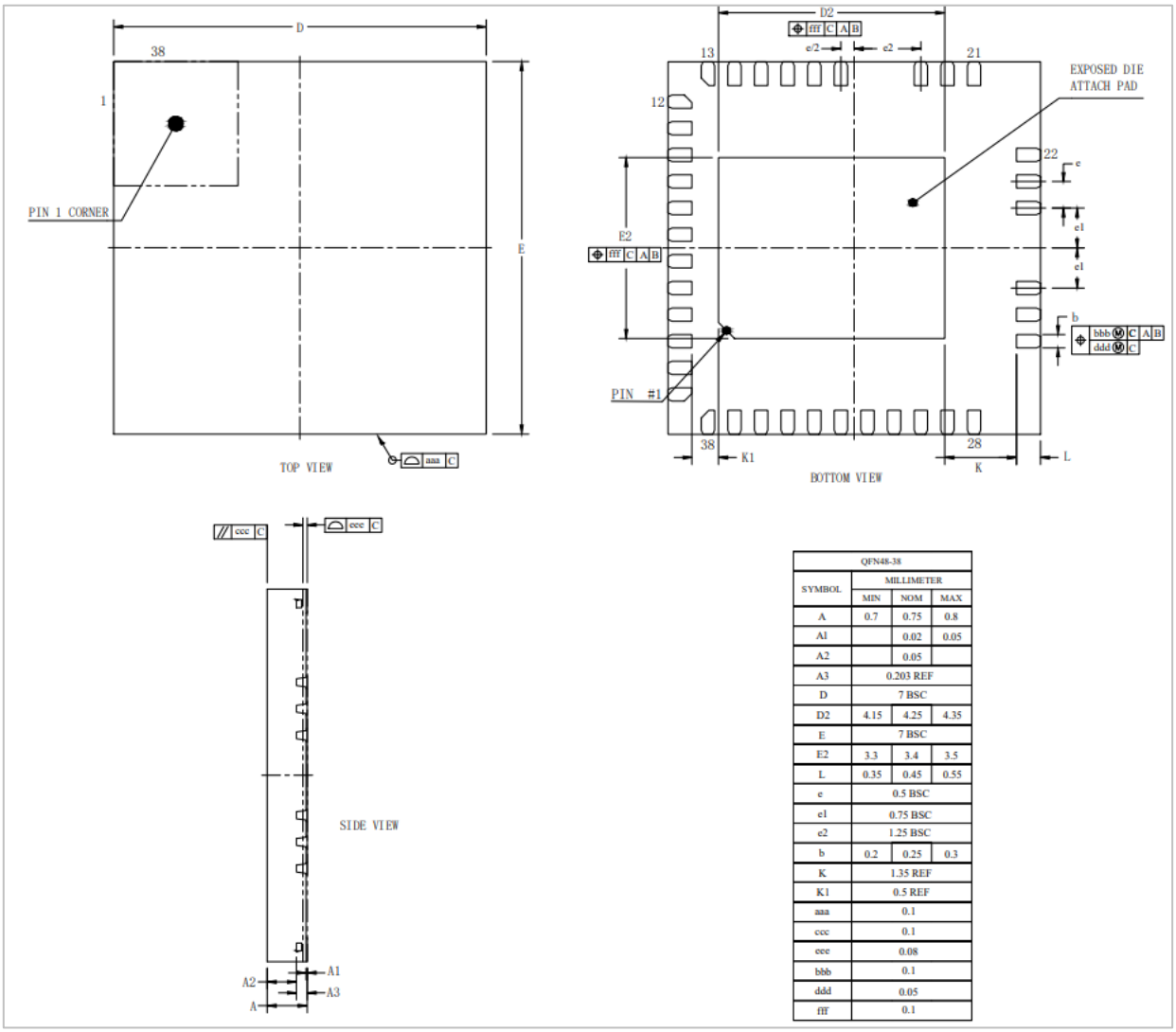
Figure 3-5 Package Drawings and Dimensions of SSOP24_8.65X3.9



SSOP24			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A			1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.50
D	8.45	8.65	8.85
E	5.8	6	6.2
E1	3.8	3.9	4
L	0.4		0.8
L1		1.05	
e		0.635	
b	0.2		0.31

3.6 QFN48-38_7X7(for FU6862Q)

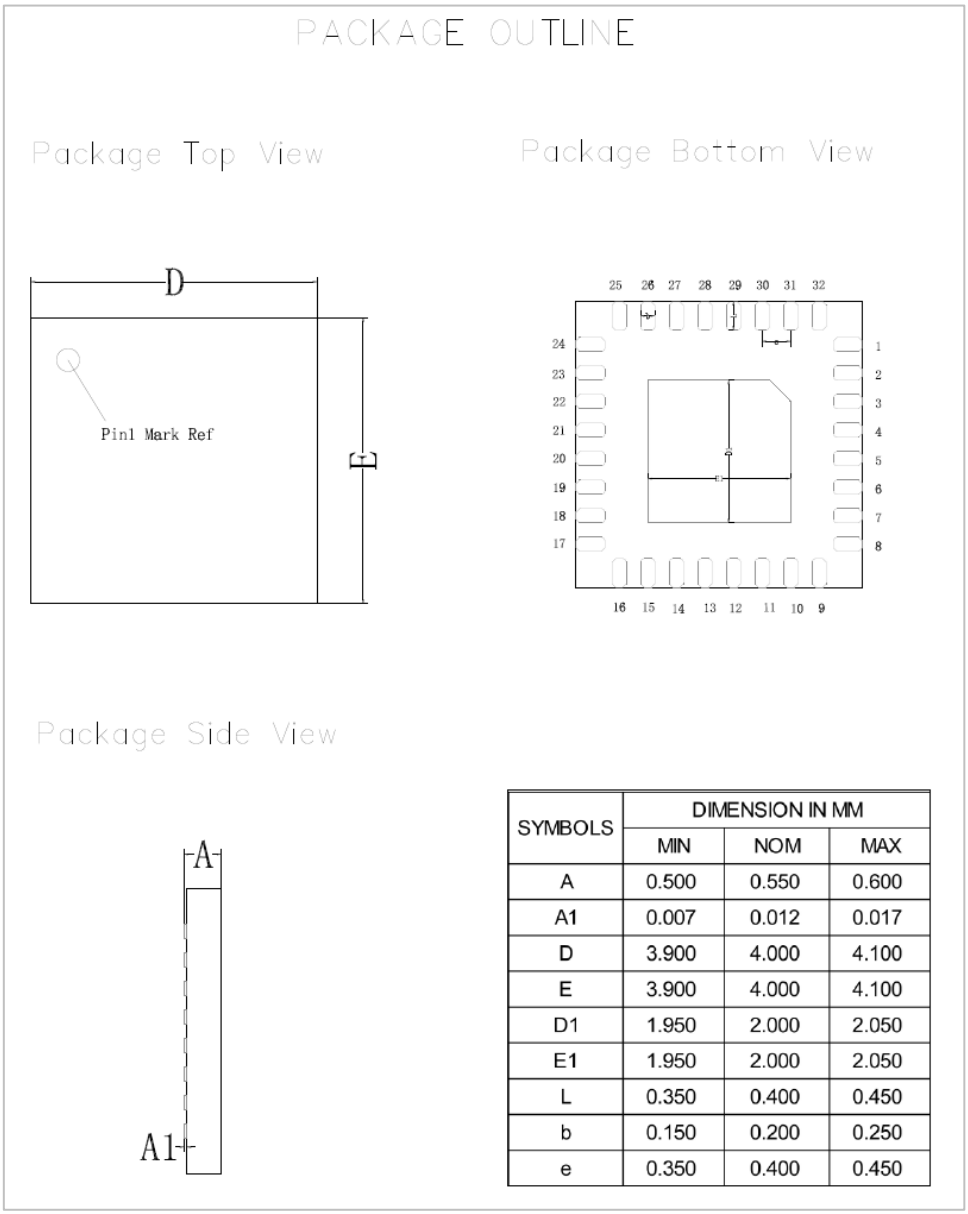
Figure 3-6 Package Drawings of QFN48-38_7X7



QFN48-38			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1		0.02	0.05
A2		0.05	
A3	0.203 REF		
D	7 BSC		
D2	4.15	4.25	4.35
E	7 BSC		
E2	3.3	3.4	3.5
L	0.35	0.45	0.55
e	0.5 BSC		
e1	0.75 BSC		
e2	1.25 BSC		
b	0.2	0.25	0.3
K	1.35 REF		
K1	0.5 REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
ddd	0.05		
fff	0.1		

3.7 PLQFN32_4X4(for FU6872P)

Figure 3-7 Package Drawings and Dimensions of QFN32_4X4



SYMBOLS	DIMENSION IN MM		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.007	0.012	0.017
D	3.900	4.000	4.100
E	3.900	4.000	4.100
D1	1.950	2.000	2.050
E1	1.950	2.000	2.050
L	0.350	0.400	0.450
b	0.150	0.200	0.250
e	0.350	0.400	0.450

4 Ordering Information

Table 4-1 Model Selections

Model	Clock Rate (MHz)	Flash (kByte)	XRAM (kByte)	Clock Circuit		Driver Interface		Drive Type			I²C	UART	SPI	DMA	GPIO	Timer	Analog Peripherals								Lead-free	Package
																	ADC			DAC						
				Internal Fast Clock	Internal Slow Clock	6N Pre-driver	PWM	Square-wave	SVPWM	FOC							Number	Channel	Bits	Number	Bits	VREF	Operational Amplifier	Comparator		
FU6812L2	24	16	0.75	√	√	-	√	√	√	√	√	√	√	√	34	6	1	12	12	1	9	√	3	3	√	LQFP48 (7x7mm)
FU6812N2	24	16	0.75	√	√	-	√	√	√	√	√	√	√	√	20	6	1	7	12	1	9	√	1	2	√	QFN32 (4x4mm)
FU6812S2	24	16	0.75	√	√	-	√	√	√	√	-	√	√	√	12	6	1	6	12	1	9	√	1	2	√	SSOP24 (8.65x 3.9mm)
FU6812V	24	16	0.75	√	√	-	√	√	√	√	-	√	-	√	13	6	1	7	12	1	9	√	3	2	√	SSOP24 (8.65x 3.9mm)

Model	Clock Rate (MHz)	Flash (kByte)	XRAM (kByte)	Clock Circuit		Driver Interface		Drive Type			I²C	UART	SPI	DMA	GPIO	Timer	Analog Peripherals								Lead-free	Package
																	ADC			DAC						
				Internal Fast Clock	Internal Slow Clock	6N Pre-driver	PWM	Square-wave	SVPWM	FOC							Number	Channel	Bits	Number	Bits	VREF	Operational Amplifier	Comparator		
FU6861Q2	24	16	0.75	√	√	√	-	√	√	√	√	√	√	√	32	6	1	12	12	1	9	√	3	3	√	QFN56 (7x7mm)
FU6861L2	24	16	0.75	√	√	√	-	√	√	√	√	√	√	√	27	6	1	11	12	1	9	√	3	3	√	LQFP48 (7x7mm)
FU6861N2	24	16	0.75	√	√	√	-	√	√	√	√	√	√	√	19	6	1	9	12	1	9	√	1	3	√	QFN40 (5x5mm)
FU6861NF2	24	16	0.75	√	√	√	-	√	-	-	√	√	√	√	19	6	1	9	12	1	9	√	1	3	√	QFN40 (5x5mm)
FU6862L	24	16	0.75	√	√	√	-	√	√	√	-	√	√	√	20	6	1	10	12	1	9	√	3	3	√	LQFP48 (7x7mm)
FU6862Q	24	16	0.75	√	√	√	-	√	√	√	-	√	√	√	20	6	1	10	12	1	9	√	3	3	√	QFN48 (7x7mm)
FU6872P	24	16	0.75	√	√	√	-	√	√	√	√	√	-	√	18	6	1	10	12	1	9	√	3	2	√	PLQFN32 (4x4mm)

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Attention:

Stress values greater than "Absolute Maximum Ratings" listed in Table 5-1 ~ Table 5-4 may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

5.1.1 FU6812L2

Table 5-1 Absolute Maximum Ratings of FU6812L2

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature STG		-55	-	150	℃
Operating Ambient Temperature T_A	VCC ≤ 12V, Ivcc ≤ 30mA	-40	-	105	℃
Operating Ambient Temperature T_A		-40	-	85	℃
VCC to VSS Voltage		-0.3	-	36	V
VDD5/IOVCC to VSS Voltage		-0.3	5	6.5	V
VDD18		-0.3	1.85	2	V
RSTN/VCC_MODE/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V

5.1.2 FU6812N2

Table 5-2 Absolute Maximum Ratings of FU6812N2

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature TSTG		-55	-	150	℃
Operating Ambient Temperature T_A	VCC ≤ 12V, Ivcc ≤ 30mA	-40	-	105	℃
Operating Ambient Temperature T_A		-40	-	85	℃
VCC to VSS Voltage		-0.3	-	36	V
VDD5/IOVCC to VSS Voltage		-0.3	5	6.5	V
VDD18		-0.3	1.85	2	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RSTN/VCC_MODE/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V

5.1.3 FU6812S2

Table 5-3 Absolute Maximum Ratings of FU6812S2

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature TJ		-40	-	150	℃
Storage Temperature TSTG		-55	-	150	℃
Operating Ambient Temperature TA	VCC ≤ 12V, Ivcc ≤ 30mA	-40	-	105	℃
Operating Ambient Temperature TA		-40	-	85	℃
VCC to VSS Voltage		-0.3	-	36	V
VDD5/IOVCC to VSS Voltage		-0.3	5	6.5	V
VDD18		-0.3	1.85	2	V
RSTN/VCC_MODE/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V

5.1.4 FU6812V

Table 5-4 Absolute Maximum Ratings of FU6812V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature TSTG		-55	-	150	℃
Operating Ambient Temperature T_A	VCC ≤ 12V, Ivcc ≤ 30mA	-40	-	105	℃
Operating Ambient Temperature T_A		-40	-	85	℃
VCC to VSS Voltage		-0.3	-	36	V
VDD5/IOVCC to VSS Voltage		-0.3	5	6.5	V
VDD18		-0.3	1.85	2	V
RSTN/VCC_MODE/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V

5.1.5 FU6861Q2

Table 5-5 Absolute Maximum Ratings of FU6861Q2

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature TSTG		-55	-	150	℃
Operating Ambient Temperature T_A	VCC ≤ 12V, Ivcc ≤ 30mA	-40	-	105	℃

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Ambient Temperature T_A		-40	-	85	℃
VCC to VSS Voltage		-0.3	-	36	V
VDD5/IOVCC to VSS Voltage		-0.3	5	6.5	V
VDRV to VSS Voltage		-0.3	-	22	V
High-side Floating Voltage $V_{BU,BV,BW}$		-0.3	-	180	V
High-side Floating Offset Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 22	-	$V_{BU,BV,BW}$ + 0.3	V
High-side Output Voltage $V_{HU,HV,HW}$		$V_{SU,SV,SW}$ - 0.3	-	$V_{BU,BV,BW}$ + 0.3	V
Low-side Output Voltage $V_{LU,LV,LW}$		-0.3	-	VDRV + 0.3	V
VDD18		-0.3	1.85	2	V
RSTN/VCC_MODE/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V

5.1.6 FU6861N2

Table 5-6 Absolute Maximum Ratings of FU6861N2

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature STG		-55	-	150	℃
Operating Ambient Temperature T_A	VCC ≤ 12V, Ivcc ≤ 30mA	-40	-	105	℃
Operating Ambient Temperature T_A		-40	-	85	℃
VCC to VSS Voltage		-0.3	-	36	V
VDD5/IOVCC to VSS Voltage		-0.3	-	6.5	V
VDRV to VSS Voltage		-0.3	-	22	V
High-side Floating Voltage $V_{BU,BV,BW}$		-0.3	-	180	V
High-side Floating Offset Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 22	-	$V_{BU,BV,BW}$ + 0.3	V
High-side Output Voltage $V_{HU,HV,HW}$		$V_{SU,SV,SW}$ - 0.3	-	$V_{BU,BV,BW}$ + 0.3	V
Low-side Output Voltage $V_{LU,LV,LW}$		-0.3	-	VDRV + 0.3	V
VDD18		-0.3	1.85	2	V
RSTN/VCC_MODE/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V

5.1.7 FU6861L2

Table 5-7 Absolute Maximum Ratings of FU6861L2

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature TSTG		-55	-	150	℃
Operating Ambient Temperature T_A	VCC ≤ 12V, Ivcc ≤ 30mA	-40	-	105	℃
Operating Ambient Temperature T_A		-40	-	85	℃
VCC to VSS Voltage		-0.3	-	36	V
VDD5/IOVCC to VSS Voltage		-0.3	5	6.5	V
VDRV to VSS Voltage		-0.3	-	22	V
High-side Floating Voltage $V_{BU,BV,BW}$		-0.3	-	180	V
High-side Floating Offset Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 22	-	$V_{BU,BV,BW}$ + 0.3	V
High-side Output Voltage $V_{HU,HV,HW}$		$V_{SU,SV,SW}$ - 0.3	-	$V_{BU,BV,BW}$ + 0.3	V
Low-side Output Voltage $V_{LU,LV,LW}$		-0.3	-	VDRV + 0.3	V
VDD18		-0.3	1.85	2	V
RSTN/VCC_MODE/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V

5.1.8 FU6861NF2

Table 5-8 Absolute Maximum Ratings of FU6861NF2

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature TSTG		-55	-	150	℃
Operating Ambient Temperature T_A	VCC ≤ 12V, Ivcc ≤ 30mA	-40	-	105	℃
Operating Ambient Temperature T_A		-40	-	85	℃
VCC to VSS Voltage		-0.3	-	36	V
VDD5/IOVCC to VSS Voltage		-0.3	5	6.5	V
VDRV to VSS Voltage		-0.3	-	22	V
High-side Floating Voltage $V_{BU,BV,BW}$		-0.3	-	165	V
High-side Floating Offset Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 22	-	$V_{BU,BV,BW}$ + 0.3	V
High-side Output Voltage $V_{HU,HV,HW}$		$V_{SU,SV,SW}$ - 0.3	-	$V_{BU,BV,BW}$ + 0.3	V
Low-side Output Voltage $V_{LU,LV,LW}$		-0.3	-	VDRV + 0.3	V
VDD18		-0.3	1.85	2	V

RSTN/VCC_MODE/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V

5.1.9 FU6862L

Table 5-9 Absolute Maximum Ratings of FU6862L

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature TSTG		-55	-	150	℃
Operating Ambient Temperature T_A		-40	-	85	℃
VCC to VSS Voltage		-0.3	-	22	V
VDD5 to VSS Voltage		-0.3	-	6.5	V
High-side Floating Voltage $V_{BU,BV,BW}$		-0.3	-	625	V
High-side Floating Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 22	-	$V_{BU,BV,BW}$ - 0.3	V
High-side Output Voltage $V_{HU,HV,HW}$		$V_{SU,SV,SW}$ - 0.3	-	$V_{BU,BV,BW}$ - 0.3	V
Low-side supply voltage		-0.3	-	VCC	V
Low-side Output Voltage $V_{LU,LV,LW}$		-0.3	-	VCC + 0.3	V
RSTN/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V

5.1.10 FU6862Q

Table 5-10 Absolute Maximum Ratings of FU6862Q

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature TSTG		-55	-	150	℃
Operating Ambient Temperature T_A		-40	-	85	℃
VCC to VSS Voltage		-0.3	-	22	V
VDD5 to VSS Voltage		-0.3	-	6.5	V
High-side Floating Voltage $V_{BU,BV,BW}$		-0.3	-	625	V
High-side Floating Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 22	-	$V_{BU,BV,BW}$ - 0.3	V
High-side Output Voltage $V_{HU,HV,HW}$		$V_{SU,SV,SW}$ - 0.3	-	$V_{BU,BV,BW}$ - 0.3	V
Low-side supply voltage		-0.3	-	VCC	V
Low-side Output Voltage $V_{LU,LV,LW}$		-0.3	-	VCC + 0.3	V
RSTN/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V

5.1.11 FU6872P

Table 5-11 Absolute Maximum Ratings of FU6872P

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	℃

Storage Temperature TSTG		-55	-	150	℃
Operating Ambient Temperature T_A		-40	-	85	℃
VCC to VSS Spike Voltage	t < 500ms	-0.3	-	90	V
VCC to VSS Voltage		-0.3	-	80	V
VREG to VSS Voltage		-0.3	-	20	V
VDD5 to VSS Voltage		-0.3	-	6	V
VDD18 to VSS Voltage		-0.3	1.85	2	V
$V_{BU,BV,BW}$ to VSS Voltage		-0.3	-	VCC + VREG + 0.3	V
$V_{SU,SV,SW}$ to VSS Voltage		-2	-	VCC + 0.3	V
$V_{HU,HV,HW}$ to VSS Voltage		-2	-	VCC + VREG + 0.3	V
$V_{LU,LV,LW}$ to VSS Voltage		-0.3	-	VREG + 0.3	V
RSTN/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V

5.2 Global Electrical Characteristics

5.2.1 FU6812L2

Table 5-12 Global Electrical Characteristics of FU6812L2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1]	High-voltage single-power supply mode: VCC_MODE = 0	5	-	24	V
	High-voltage dual-power supply mode: VCC_MODE = 1, VCC ≥ VDD5.	5	-	36	V
	Low-voltage single-power supply mode: VCC_MODE = 1 and VCC pin is connected to VDD5 pin.	3	-	5.5	V
VDD5 Operating Voltage[1]	VCC_MODE = 1, VCC pin is connected to VDD5 pin.	3	5	5.5	V
IOVCC Operating Voltage		3	VDD5	VDD5 + 0.3	V
I_{VCC} Operating Current[2]		-	24	-	mA
I_{VCC} Standby Current[2]		-	6	-	mA
I_{VCC} Sleep-mode Current[3]	VCC_MODE = 0	-	100	250	μA

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Ambient Temperature T_A	VCC_MODE = 1, VCC = VDD5 = 5V	-	45	100	μA
Operating Ambient Temperature T_A	VCC ≤ 15V & Ivcc ≤ 30mA	-40	-	105[4]	℃

5.2.2 FU6812N2

Table 5-13 Global Electrical Characteristics of FU6812N2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1]	High-voltage single-power supply mode: VCC_MODE = 0	5	-	24	V
	High-voltage dual-power supply mode: VCC_MODE = 1, VCC ≥ VDD5.	5	-	36	V
	Low-voltage single-power supply mode: VCC_MODE = 1 and VCC pin is connected to VDD5 pin.	3	-	5.5	V
VDD5 Operating Voltage[1]	VCC_MODE = 1, VCC pin is connected to VDD5 pin.	3	5	5.5	V
IOVCC Operating Voltage		3	VDD5	VDD5 + 0.3	V
I_{VCC} Operating Current[2]		-	24	-	mA
I_{VCC} Standby Current[2]		-	6	-	mA
I_{VCC} Sleep-mode Current[3]	VCC_MODE = 0	-	100	250	μA
Operating Ambient Temperature T_A	VCC_MODE = 1, VCC = VDD5 = 5V	-	45	100	μA
Operating Ambient Temperature T_A	VCC ≤ 15V & Ivcc ≤ 30mA	-40	-	105[4]	℃

5.2.3 FU6812S2

Table 5-14 Global Electrical Characteristics of FU6812S2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1]	High-voltage single-power supply mode: VCC_MODE = 0	5	-	24	V
	High-voltage dual-power supply mode: VCC_MODE = 1,	5	-	36	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	VCC ≥ VDD5.				
	Low-voltage single-power supply mode: VCC_MODE = 1 and VCC pin is connected to VDD5 pin.	3	-	5.5	V
VDD5 Operating Voltage[1]	VCC_MODE = 1, VCC pin is connected to VDD5 pin.	3	5	5.5	V
IOVCC Operating Voltage		3	VDD5	VDD5 + 0.3	V
I_{VCC} Operating Current[2]		-	24	-	mA
I_{VCC} Standby Current[2]		-	6	-	mA
I_{VCC} Sleep-mode Current[3]	VCC_MODE = 0	-	100	250	μA
Operating Ambient Temperature T_A	VCC_MODE = 1, VCC = VDD5 = 5V	-	45	100	μA
Operating Ambient Temperature T_A	VCC ≤ 15V & Ivcc ≤ 30mA	-40	-	105[4]	℃

5.2.4 FU6812V

Table 5-15 Global Electrical Characteristics of FU6812V

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1]	High-voltage single-power supply mode: VCC_MODE = 0	5	-	24	V
	High-voltage dual-power supply mode: VCC_MODE = 1, VCC ≥ VDD5.	5	-	36	V
	Low-voltage single-power supply mode: VCC_MODE = 1 and VCC pin is connected to VDD5 pin.	3	-	5.5	V
VDD5 Operating Voltage[1]	VCC_MODE = 1, VCC pin is connected to VDD5 pin.	3	5	5.5	V
IOVCC Operating Voltage		3	VDD5	VDD5 + 0.3	V
I_{VCC} Operating Current[2]		-	24	-	mA
I_{VCC} Standby Current[2]		-	6	-	mA
I_{VCC} Sleep-mode Current[3]	VCC_MODE = 0	-	100	250	μA
Operating Ambient Temperature T_A	VCC_MODE = 1, VCC = VDD5 = 5V	-	45	100	μA

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Ambient Temperature T_A	VCC ≤ 15V & Ivcc ≤ 30mA	-40	-	105[4]	℃

Note

[1] VDD5 must be in the range of 5V~5.5V during Flash write or erase

[2] Characteristics may vary with different configurations

Unless otherwise specified, VCC_MODE = 0 means VCC_MODE = GND, and VCC_MODE = 1 means VCC_MODE = VDD5

[4] The chip can work at the maximum T_A only if T_J does not exceed the maximum T_J at any time

5.2.5 FU6861Q2

Table 5-16 Global Electrical Characteristics of FU6861Q2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1]	High-voltage single-power supply mode: VCC_MODE = 0	5	-	24	V
	Dual-power supply mode: VCC_MODE = 1, VCC ≥ VDD5	5	-	36	V
VDD5 Operating Voltage[1]	VCC_MODE = 1, VCC pin is connected to VDD5 pin.	3	5	5.5	V
IOVCC Operating Voltage		3	VDD5	VDD5 + 0.3	V
VDRV Operating Voltage		7	-	18	V
V_{BU}, V_{BV}, V_{BW} Floating Voltage		-	-	180	V
V_{BU} to V_{SU} Voltage V_{BV} to V_{SV} Voltage V_{BW} to V_{SW} Voltage		-	-	18	V
I_{VCC} Operating Current[2]		-	24	-	mA
I_{VCC} Standby Current[2]		-	6	-	mA
I_{VCC} Sleep-mode Current	VCC_MODE = 0	-	350	650	μA
	VCC_MODE = 1, VCC = VDD5 = 5V	-	300	500	μA
Operating Ambient Temperature T_A	VCC ≤ 15V & Ivcc ≤ 30mA	-40	-	105[3]	℃

5.2.6 FU6861N2

Table 5-17 Global Electrical Characteristics of FU6861N2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1]	High-voltage single-power supply mode: VCC_MODE = 0	5	-	24	V
	Dual-power supply mode: VCC_MODE = 1, VCC ≥ VDD5	5	-	36	V
VDD5 Operating Voltage[1]	VCC_MODE = 1, VCC pin is connected to VDD5 pin.	3	5	5.5	V
IOVCC Operating Voltage		3	VDD5	VDD5 + 0.3	V
VDRV Operating Voltage		7	-	18	V
V_{BU}, V_{BV}, V_{BW} Floating Voltage		-	-	180	V
V_{BU} to V_{SU} Voltage V_{BV} to V_{SV} Voltage V_{BW} to V_{SW} Voltage		-	-	18	V
I_{VCC} Operating Current[2]		-	24	-	mA
I_{VCC} Standby Current[2]		-	6	-	mA
I_{VCC} Sleep-mode Current	VCC_MODE = 0	-	350	650	μA
	VCC_MODE = 1, VCC = VDD5 = 5V	-	300	500	μA
Operating Ambient Temperature T_A	VCC ≤ 15V & Ivcc ≤ 30mA	-40	-	105[3]	℃

5.2.7 FU6861L2

Table 5-18 Global Electrical Characteristics of FU6861L2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1]	High-voltage single-power supply mode: VCC_MODE = 0	5	-	24	V
	Dual-power supply mode: VCC_MODE = 1, VCC ≥ VDD5	5	-	36	V
VDD5 Operating Voltage[1]	VCC_MODE = 1, VCC pin connects with VDD5 pin	3	5	5.5	V
IOVCC Operating Voltage		3	VDD5	VDD5 + 0.3	V
VDRV Operating Voltage		7	-	18	V
V_{BU}, V_{BV}, V_{BW} Floating Voltage		-	-	180	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{BU} to V_{SU} Voltage V_{BV} to V_{SV} Voltage V_{BW} to V_{SW} Voltage		-	-	18	V
I_{VCC} Operating Current[2]		-	24	-	mA
I_{VCC} Standby Current[2]		-	6	-	mA
I_{VCC} Sleep-mode Current	VCC_MODE = 0	-	350	650	μA
	VCC_MODE = 1, VCC = VDD5 = 5V	-	300	500	μA
Operating Ambient Temperature T_A	VCC ≤ 15V & Ivcc ≤ 30mA	-40	-	105[3]	℃

5.2.8 FU6861NF2

Table 5-19 Global Electrical Characteristics of FU6861NF2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1]	High-voltage single-power supply mode: VCC_MODE = 0	5	-	24	V
	Dual-power supply mode: VCC_MODE = 1, VCC ≥ VDD5	5	-	36	V
VDD5 Operating Voltage[1]	VCC_MODE = 1, VCC pin is connected to VDD5 pin.	3	5	5.5	V
IOVCC Operating Voltage		3	VDD5	VDD5 + 0.3	V
VDRV Operating Voltage		7	-	18	V
V_{BU}, V_{BV}, V_{BW} Floating Voltage		-	-	180	V
V_{BU} to V_{SU} Voltage V_{BV} to V_{SV} Voltage V_{BW} to V_{SW} Voltage		-	-	18	V
I_{VCC} Operating Current[2]		-	24	-	mA
I_{VCC} Standby Current[2]		-	6	-	mA
I_{VCC} Sleep-mode Current	VCC_MODE = 0	-	350	650	μA
	VCC_MODE = 1, VCC = VDD5 = 5V	-	300	500	μA
Operating Ambient Temperature T_A	VCC ≤ 15V & Ivcc ≤ 30mA	-40	-	105[3]	℃

Note

[1] VDD5 must be in the range of 5V~5.5V during Flash write or erase

[2] Characteristics may vary with different configurations

The chip can work at the maximum T_A only if T_J does not exceed the maximum T_J at any time

5.2.9 FU6862L

Table 5-20 Global Electrical Characteristics of FU6862L

(T_A = 25℃ and VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1][2]		12	-	20	V
I_{VCC} Operating Current[3]		-	24	-	mA
I_{VCC} Standby Current[3]		-	6	-	mA
I_{VCC} Sleep-mode Current	VCC = 12V	-	210	-	μA
Operating Ambient Temperature T_A	VCC ≤ 15V & Ivcc ≤ 30mA	-40	-	105[4]	℃

5.2.10 FU6862Q

Table 5-21 Global Electrical Characteristics of FU6862Q

(T_A = 25℃ and VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1][2]		12	-	20	V
I_{VCC} Operating Current[3]		-	24	-	mA
I_{VCC} Standby Current[3]		-	6	-	mA
I_{VCC} Sleep-mode Current	VCC = 12V	-	210	-	μA
Operating Ambient Temperature T_A	VCC ≤ 15V & Ivcc ≤ 30mA	-40	-	105[4]	℃

Note

[1] VDD5 must be in the range of 5V~5.5V during Flash write or erase

[2] VCC voltage rise rate ranges from 0.5V/μs to 0.1V/s depending on samples batches

[3] Characteristics may vary with different configurations.

[4] The chip can work at the maximum T_A only if T_J does not exceed the maximum T_J at any time

5.2.11 FU6872P

Table 5-22 Global Electrical Characteristics of FU6872P

(T_A = 25℃ and VCC = 15V ~ 75V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage[1][2]		15	-	75	V
VREG Operating Voltage		10	-	13	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Operating Voltage[2]		3	5	5.5	V
I_{VCC} Operating Current[3]		-	24	-	mA
I_{VCC} Standby Current[3]		-	6	-	mA
I_{VCC} Sleep-mode Current		-	150	300	μA
Operating Ambient Temperature T_A	VCC = 48V, I_{VCC} ≤ 30mA	-40	-	105[4]	℃

Note

[1] VDD5 must be in the range of 5V~5.5V during Flash write or erase

[2] VCC voltage rise rate ranges from 0.5V/μs to 0.1V/s depending on samples batches

[3] Characteristics may vary with different configurations

[4] The chip can work at the maximum T_A only if T_J does not exceed the maximum T_J at any time

5.3 GPIO Electrical Characteristics

5.3.1 FU6812L2

Table 5-23 GPIO Electrical Characteristics of FU6812L2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, TA = 25℃	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, TA = 25℃	-	13	-	ns
V_{OH} High-level Output Voltage	I_{OH} = 4mA, I_{OVCC} = VDD5 = 5	VDD5 - 0.7	-	-	V
V_{OL} Low-level Output Voltage	I_{OL} = 4mA, I_{OVCC} = VDD5 = 5	-	-	0.7	V
V_{IH} High-level Input Voltage[1]		0.7*VDD5	-	-	V
V_{IL} Low-level Input Voltage	I_{OVCC} = VDD5 = 5V	-	-	0.2*VDD5	V
Pull-up Resistor[2]	V_{IN} = 0V	-	33	-	kΩ
Pull-up Resistor[3]	V_{IN} = 0V	-	5	-	kΩ

Note

[1] When VDD5 = 5V, minimum value of VIH is 0.6*VDD5

[2] GPIOs except P0[2:0], P1[6:3], P2[1] and P3[7:6]

[3] P0[2:0], P1[6:3], P2[1] and P3[7:6]

5.3.2 FU6812N2

Table 5-24 GPIO Electrical Characteristics of FU6812N2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, TA = 25℃	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, TA = 25℃	-	13	-	ns
V_{OH} High-level Output Voltage	I_{OH} = 4mA, I_{OVCC} = VDD5 = 5	VDD5 - 0.7	-	-	V
V_{OL} Low-level Output Voltage	I_{OL} = 4mA, I_{OVCC} = VDD5 = 5	-	-	0.7	V
V_{IH} High-level Input Voltage[1]		0.7*VDD5	-	-	V
V_{IL} Low-level Input Voltage	I_{OVCC} = VDD5 = 5V	-	-	0.2*VDD5	V
Pull-up Resistor[2]	V_{IN} = 0V	-	33	-	kΩ
Pull-up Resistor[3]	V_{IN} = 0V	-	5	-	kΩ

Note

[1] When VDD5 = 5V, minimum value of VIH is 0.6*VDD5

[2] GPIOs except P0[1:0], P1[6:3] and P2[1]

[3] P0[1:0], P1[6:3] and P2[1]

5.3.3 FU6812S2

Table 5-25 GPIO Electrical Characteristics OF FU6812S2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, TA = 25℃	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, TA = 25℃	-	13	-	ns
V_{OH} High-level Output Voltage	I_{OH} = 4mA, I_{OVCC} = VDD5 = 5	VDD5 - 0.7	-	-	V
V_{OL} Low-level Output Voltage	I_{OL} = 4mA, I_{OVCC} = VDD5 = 5	-	-	0.7	V
V_{IH} High-level Input Voltage[1]		0.7*VDD5	-	-	V
V_{IL} Low-level Input Voltage	I_{OVCC} = VDD5 = 5V	-	-	0.2*VDD5	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Pull-up Resistor[2]	V_{IN} = 0V	-	33	-	kΩ
Pull-up Resistor[3]	V_{IN} = 0V	-	5	-	kΩ

Note

[1] When VDD5 = 5V, minimum value of VIH is 0.6*VDD5

[2] GPIOs except P1[4:3], P1[6] and P2[1]

[3] P1[4:3], P1[6], P2[1]

5.3.4 FU6812V

Table 5-26 GPIO Electrical Characteristics of FU6812V

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, TA = 25℃	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, TA = 25℃	-	13	-	ns
VOH High-level Output Voltage	I_{OH} = 4mA, I_{OVCC} = VDD5 = 5	VDD5 - 0.7	-	-	V
VOL Low-level Output Voltage	I_{OL} = 4mA, I_{OVCC} = VDD5 = 5	-	-	0.7	V
VIH High-level Input Voltage[1]		0.7*VDD5	-	-	V
VIL Low-level Input Voltage	I_{OVCC} = VDD5 = 5V	-	-	0.2*VDD5	V
Pull-up Resistor[2]	V_{IN} = 0V	-	33	-	kΩ
Pull-up Resistor[3]	V_{IN} = 0V	-	5	-	kΩ

Note

[1] When VDD5 = 5V, minimum value of VIH is 0.6*VDD5

[2] GPIOs except P1[4], P1[6] and P2[1]

[3] P1[4], P1[6], P2[1]

5.3.5 FU6861Q2

Table 5-27 GPIO Electrical Characteristics of FU6861Q2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, TA = 25℃	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, TA = 25℃	-	13	-	ns

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH} High-level Output Voltage	I_{OH} = 4mA， I_{OVCC} = VDD5 = 5	VDD5 - 0.7	-	-	V
V_{OL} Low-level Output Voltage	I_{OL} = 4mA， I_{OVCC} = VDD5 = 5	-	-	0.7	V
V_{IH} High-level Input Voltage[1]		0.7*VDD5	-	-	V
V_{IL} Low-level Input Voltage	I_{OVCC} = VDD5 = 5V	-	-	0.2*VDD5	V
Pull-up Resistor[2]	V_{IN} = 0V	-	33	-	kΩ
Pull-up Resistor[3]	V_{IN} = 0V	-	5	-	kΩ

Note

[1] When VDD5 = 5V, minimum value of VIH is 0.6*VDD5

[2] GPIOs except P0[2:0], P1[6:3], P2[1] and P3[7:6]

[3] P0[2:0], P1[6:3], P2[1] and P3[7:6]

5.3.6 FU6861L2

Table 5-28 GPIO Electrical Characteristics f FU6861L2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, TA = 25℃	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, TA = 25℃	-	13	-	ns
V_{OH} High-level Output Voltage	I_{OH} = 4mA， I_{OVCC} = VDD5 = 5	VDD5 - 0.7	-	-	V
V_{OL} Low-level Output Voltage	I_{OL} = 4mA， I_{OVCC} = VDD5 = 5	-	-	0.7	V
V_{IH} High-level Input Voltage[1]		0.7*VDD5	-	-	V
V_{IL} Low-level Input Voltage	I_{OVCC} = VDD5 = 5V	-	-	0.2*VDD5	V
Pull-up Resistor[2]	V_{IN} = 0V	-	33	-	kΩ
Pull-up Resistor[3]	V_{IN} = 0V	-	5	-	kΩ

Note

[1] When VDD5 = 5V, minimum value of VIH is 0.6*VDD5

[2] GPIOs except P0[1:0], P1[6:3] and P2[1]

[3] P0[1:0], P1[6:3] and P2[1]

5.3.7 FU6861N2

Table 5-29 GPIO Electrical Characteristics of FU6861N2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, TA = 25℃	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, TA = 25℃	-	13	-	ns
V_{OH} High-level Output Voltage	I_{OH} = 4mA, I_{OVCC} = VDD5 = 5	VDD5 - 0.7	-	-	V
V_{OL} Low-level Output Voltage	I_{OL} = 4mA, I_{OVCC} = VDD5 = 5	-	-	0.7	V
V_{IH} High-level Input Voltage[1]		0.7*VDD5	-	-	V
V_{IL} Low-level Input Voltage	I_{OVCC} = VDD5 = 5V	-	-	0.2*VDD5	V
Pull-up Resistor[2]	V_{IN} = 0V	-	33	-	kΩ
Pull-up Resistor[3]	V_{IN} = 0V	-	5	-	kΩ

Note

[1] When VDD5 = 5V, minimum value of VIH is 0.6*VDD5

[2] GPIOs except P0[1:0], P1[4:3], P1[6] and P2[1]

[3] P0[1:0], P1[4:3], P1[6], P2[1]

5.3.8 FU6861NF2

Table 5-30 GPIO Electrical Characteristics of FU6861NF2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, TA = 25℃	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, TA = 25℃	-	13	-	ns
V_{OH} High-level Output Voltage	I_{OH} = 4mA, I_{OVCC} = VDD5 = 5	VDD5 - 0.7	-	-	V
V_{OL} Low-level Output Voltage	I_{OL} = 4mA, I_{OVCC} = VDD5 = 5	-	-	0.7	V
V_{IH} High-level Input Voltage[1]		0.7*VDD5	-	-	V
V_{IL} Low-level Input Voltage	I_{OVCC} = VDD5 = 5V	-	-	0.2*VDD5	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Pull-up Resistor[2]	V_{IN} = 0V	-	33	-	kΩ
Pull-up Resistor[3]	V_{IN} = 0V	-	5	-	kΩ

Note

[1] When VDD5 = 5V, minimum value of VIH is 0.6*VDD5.

[2] GPIOs except P0[1:0], P1[4:3], P1[6] and P2[1]

[3] P0[1:0], P1[4:3], P1[6], P2[1]

5.3.9 FU6862L

Table 5-31 GPIO Electrical Characteristics of FU6862L

(T_A = 25℃ and VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, TA = 25℃	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, TA = 25℃	-	13	-	ns
V_{OH} High-level Output Voltage	I_{OH} = 4mA, I_{OVCC} = VDD5 = 5	VDD5 - 0.7	-	-	V
V_{OL} Low-level Output Voltage	I_{OL} = 4mA, I_{OVCC} = VDD5 = 5	-	-	VSS + 0.7	V
V_{IH} High-level Input Voltage[1]		0.7*VDD5	-	-	V
V_{IL} Low-level Input Voltage	VDD5 = 5V	-	-	0.2*VDD5	V
Pull-up Resistor[2]	VDD5 = 5V	-	33	-	kΩ
Pull-up Resistor[3]	VDD5 = 5V	-	5.6	-	kΩ

Note

[1] When VDD5 = 5V, minimum value of VIH is 0.6*VDD5

[2] GPIOs except P0[1], P1[6:3] and P2[1]

[3] P0[1], P1[6:3], P2[1]

5.3.10 FU6862Q

Table 5-32 GPIO Electrical Characteristics of FU6862Q

(T_A = 25℃ and VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, TA = 25℃	-	15	-	ns

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-off Fall Time	50pF load, from 90% to 10%, TA = 25℃	-	13	-	ns
V_{OH} High-level Output Voltage	I_{OH} = 4mA, I_{OVCC} = VDD5 = 5	VDD5 - 0.7	-	-	V
V_{OL} Low-level Output Voltage	I_{OL} = 4mA, I_{OVCC} = VDD5 = 5	-	-	VSS + 0.7	V
V_{IH} High-level Input Voltage[1]		0.7*VDD5	-	-	V
V_{IL} Low-level Input Voltage	VDD5 = 5V	-	-	0.2*VDD5	V
Pull-up Resistor[2]	VDD5 = 5V	-	33	-	kΩ
Pull-up Resistor[3]	VDD5 = 5V	-	5.6	-	kΩ

Note

[1] When VDD5 = 5V, minimum value of VIH is 0.6*VDD5

[2] GPIOs except P0[1], P1[6:3] and P2[1]

[3] P0[1], P1[6:3], P2[1]

5.3.11 FU6872P

Table 5-33 GPIO Electrical Characteristics of FU6872P

(T_A = 25℃ and VCC = 15V ~ 75V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, TA = 25℃	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, TA = 25℃	-	13	-	ns
V_{OH} High-level Output Voltage	I_{OH} = 4mA, I_{OVCC} = VDD5 = 5	VDD5 - 0.7	-	-	V
V_{OL} Low-level Output Voltage	I_{OL} = 4mA, I_{OVCC} = VDD5 = 5	-	-	VSS + 0.7	V
V_{IH} High-level Input Voltage[1]		0.7*VDD5	-	-	V
V_{IL} Low-level Input Voltage	VDD5 = 5V	-	-	0.2*VDD5	V
Pull-up Resistor[2]	VDD5 = 5V	-	33	-	kΩ
Pull-up Resistor[3]	VDD5 = 5V	-	5.6	-	kΩ

Note

[1] When VDD5 = 5V, minimum value of VIH is 0.6*VDD5

[2] GPIOs except P0[1:0], P1[6], P1[4] and P2[1]

[3] P0[1:0], P1[6], P1[4:3], P2[1]

5.4 PWM IO Electrical Characteristics (FU6812L2/FU6812N2/FU6812S2/FU6812V)

5.4.1 FU6812L2

Table 5-34 PWM IO Electrical Characteristics of FU6812L2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Output Source Current	P1_AN[HDIO] = 1	-	50	-	mA
Output Sink Current	P1_AN[HDIO] = 1	-	100	-	mA
Turn-on Rise Time	50pF load, from 10% to 90%, T_A = 25℃	-	18	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, T_A = 25℃	-	12	-	ns

5.4.2 FU6812N2

Table 5-35 PWM IO Electrical Characteristics of FU6812N2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Output Source Current	P1_AN[HDIO] = 1	-	50	-	mA
Output Sink Current	P1_AN[HDIO] = 1	-	100	-	mA
Turn-on Rise Time	50pF load, from 10% to 90%, T_A = 25℃	-	18	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, T_A = 25℃	-	12	-	ns

5.4.3 FU6812S2

Table 5-36 PWM IO Electrical Characteristics of FU6812S2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Output Source Current	P1_AN[HDIO] = 1	-	50	-	mA
Output Sink Current	P1_AN[HDIO] = 1	-	100	-	mA
Turn-on Rise Time	50pF load, from 10% to 90%, T_A = 25℃	-	18	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, T_A = 25℃	-	12	-	ns

5.4.4 FU6812V

Table 5-37 PWM IO Electrical Characteristics of FU6812V

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Output Source Current	P1_AN[HDIO] = 1	-	50	-	mA
Output Sink Current	P1_AN[HDIO] = 1	-	100	-	mA
Turn-on Rise Time	50pF load, from 10% to 90%, T_A = 25℃	-	18	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, T_A = 25℃	-	12	-	ns

5.5 6N Pre-driver IO Electrical Characteristics (FU6861Q2/FU6861L2/FU6861N2/FU6861NF2/FU6862L/FU6862Q/FU6872P)

5.5.1 FU6861Q2

Table 5-38 6N Pre-driver IO Electrical Characteristics of FU6861Q2

(T_A = 25℃, VCC = VDRV = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Peak Output Current		-	0.8	-	A
Low-level Peak Output Current		-	0.8	-	A
VDRV to VSS Voltage		5	-	20	V
High-side Floating Voltage $V_{BU,BV,BW}$		-	-	180	V
High-side Floating Offset Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 20	-	$V_{BU,BV,BW}$ - 5	V
VDRV UVLO Threshold Voltage		3.8	4.4	5	V
VDRV UVLO Release Voltage		3.5	4.1	4.7	V
VDRV UVLO Hysteresis Voltage		0.2	0.3	-	V
Turn-on Rise Time	1nF load, from 10% to 90%	-	30	70	ns
Turn-off Fall Time	1nF load, from 90% to 10%	-	30	70	ns
Deadtime		-	100	-	ns

5.5.2 FU6861L2

Table 5-39 6N Pre-driver IO Electrical Characteristics of FU6861L2

(T_A = 25℃, VCC = VDRV = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Peak Output Current		-	0.8	-	A
Low-level Peak Output Current		-	0.8	-	A
VDRV to VSS Voltage		5	-	20	V
High-side Floating Voltage $V_{BU,BV,BW}$		-	-	180	V
High-side Floating Offset Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 20	-	$V_{BU,BV,BW}$ - 5	V
VDRV UVLO Threshold Voltage		3.8	4.4	5	V
VDRV UVLO Release Voltage		3.5	4.1	4.7	V
VDRV UVLO Hysteresis Voltage		0.2	0.3	-	V
Turn-on Rise Time	1nF load, from 10% to 90%	-	30	70	ns
Turn-off Fall Time	1nF load, from 90% to 10%	-	30	70	ns
Deadtime		-	100	-	ns

5.5.3 FU6861N2

Table 5-40 6N Pre-driver IO Electrical Characteristics of FU6861N2

(T_A = 25℃, VCC = VDRV = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Peak Output Current		-	0.8	-	A
Low-level Peak Output Current		-	0.8	-	A
VDRV to VSS Voltage		5	-	20	V
High-side Floating Voltage $V_{BU,BV,BW}$		-	-	180	V
High-side Floating Offset Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 20	-	$V_{BU,BV,BW}$ - 5	V
VDRV UVLO Threshold Voltage		3.8	4.4	5	V
VDRV UVLO Release Voltage		3.5	4.1	4.7	V
VDRV UVLO Hysteresis Voltage		0.2	0.3	-	V
Turn-on Rise Time	1nF load, from 10% to 90%	-	30	70	ns
Turn-off Fall Time	1nF load, from 90% to 10%	-	30	70	ns
Deadtime		-	100	-	ns

5.5.4 FU6861NF2

Table 5-41 6N Pre-driver IO Electrical Characteristics of FU6861NF2

(T_A = 25℃, VCC = VDRV = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Peak Output Current		-	0.8	-	A
Low-level Peak Output Current		-	0.8	-	A
VDRV to VSS Voltage		5	-	20	V
High-side Floating Voltage $V_{BU,BV,BW}$		-	-	180	V
High-side Floating Offset Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 20	-	$V_{BU,BV,BW}$ - 5	V
VDRV UVLO Threshold Voltage		3.8	4.4	5	V
VDRV UVLO Release Voltage		3.5	4.1	4.7	V
VDRV UVLO Hysteresis Voltage		0.2	0.3	-	V
Turn-on Rise Time	1nF load, from 10% to 90%	-	30	70	ns
Turn-off Fall Time	1nF load, from 90% to 10%	-	30	70	ns
Deadtime		-	100	-	ns

5.5.5 FU6862L

Table 5-42 6N Pre-driver IO Electrical Characteristics of FU6862L

(T_A = 25℃ and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Peak Output Current		-	0.21	-	A
Low-level Peak Output Current		-	0.36	-	A
VCC Supply Voltage		12	-	20	V
High-side Floating Voltage $V_{BU,BV,BW}$		-	-	600	V
High-side Floating Offset Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 20	-	$V_{BU,BV,BW}$ - 12	V
VCC Quiescent Current		-	15	-	mA
VCC UVLO Threshold Voltage		8.1	9	9.9	V
VCC UVLO Release Voltage		7.5	8.4	9.3	V
VCC UVLO Hysteresis Voltage		0.4	0.6	-	V
Turn-on Rise Time	1nF load, from 10% to 90%	-	90	200	ns
Turn-off Fall Time	1nF load, from 90% to 10%	-	50	120	ns

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Deadtime		-	500	-	ns

5.5.6 FU6862Q

Table 5-43 6N Pre-driver IO Electrical Characteristics of FU6862Q

(T_A = 25℃ and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Peak Output Current		-	0.21	-	A
Low-level Peak Output Current		-	0.36	-	A
VCC Supply Voltage		12	-	20	V
High-side Floating Voltage $V_{BU,BV,BW}$		-	-	600	V
High-side Floating Offset Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 20	-	$V_{BU,BV,BW}$ - 12	V
VCC Quiescent Current		-	15	-	mA
VCC UVLO Threshold Voltage		8.1	9	9.9	V
VCC UVLO Release Voltage		7.5	8.4	9.3	V
VCC UVLO Hysteresis Voltage		0.4	0.6	-	V
Turn-on Rise Time	1nF load, from 10% to 90%	-	90	200	ns
Turn-off Fall Time	1nF load, from 90% to 10%	-	50	120	ns
Deadtime		-	500	-	ns

5.5.7 FU6872P

Table 5-44 6N Pre-driver IO Electrical Characteristics of FU6872P

(T_A = 25℃ and VCC = 15V ~ 75V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Peak Output Current		-	130	-	mA
Low-level Peak Output Current		-	660	-	mA
High-side gate driver voltage		-	11.3	-	V
Low-side gate driver voltage		-	12	-	V
H_t_{on} High-side Output Rising Edge Propagation Delay		-	100	-	ns
H_t_{on} High-side Output Falling Edge Propagation Delay		-	60	-	ns

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
L_t_{on} Low-side Output Rising Edge Propagation Delay		-	100	-	ns
L_t_{off} Low-side Output Falling Edge Propagation Delay		-	95	-	ns
Turn-on Rise Time	1nF load, from 10% to 90%	-	110	-	ns
Turn-off Fall Time	1nF load, from 90% to 10%	-	25	-	ns
Dead Time DT	High-side Output Falling Edge-Low-side Output Rising Edge	-	80	-	ns
	Low-side Output Falling Edge-High-side Output Rising Edge	-	60	-	ns

5.6 ADC Electrical Characteristics

5.6.1 FU6812L2

Table 5-45 ADC Electrical Characteristics of FU6812L2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	-	2	-	LSB
DNL (Differential Nonlinearity)	12-bit	-	1.5	-	LSB
OFFSET (Offset Error)	12-bit	-	10	-	LSB
SNR (Signal-to-noise Ratio)	f_{IN} = 350kHz	-	70.8	-	dB
ENOB (Effective Number of Bits)	f_{IN} = 350kHz	-	10.5	-	bit
SFDR (Spurious-free Dynamic Range)	f_{IN} = 350kHz	-	68.2	-	dB
THD (Total Harmonic Distortion)	f_{IN} = 350kHz	-	67	-	dB
RIN Input Resistance		-	500	-	Ω
CIN Input Capacitance		-	30	-	pF
Conversion Time		-	13	-	ADCLK[1]
Sampling Time		3	-	63	ADCLK2[2]

5.6.2 FU6812N2

Table 5-46 ADC Electrical Characteristics of FU6812N2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	-	2	-	LSB
DNL (Differential Nonlinearity)	12-bit	-	1.5	-	LSB
OFFSET (Offset Error)	12-bit	-	10	-	LSB
SNR (Signal-to-noise Ratio)	f_{IN} = 350kHz	-	70.8	-	dB
ENOB (Effective Number of Bits)	f_{IN} = 350kHz	-	10.5	-	bit
SFDR (Spurious-free Dynamic Range)	f_{IN} = 350kHz	-	68.2	-	dB
THD (Total Harmonic Distortion)	f_{IN} = 350kHz	-	67	-	dB
R_{IN} Input Resistance		-	500	-	Ω
C_{IN} Input Capacitance		-	30	-	pF
Conversion Time		-	13	-	ADCLK[1]
Sampling Time		3	-	63	ADCLK2[2]

5.6.3 FU6812S2

Table 5-47 ADC Electrical Characteristics of FU6812S2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	-	2	-	LSB
DNL (Differential Nonlinearity)	12-bit	-	1.5	-	LSB
OFFSET (Offset Error)	12-bit	-	10	-	LSB
SNR (Signal-to-noise Ratio)	f_{IN} = 350kHz	-	70.8	-	dB
ENOB (Effective Number of Bits)	f_{IN} = 350kHz	-	10.5	-	bit
SFDR (Spurious-free Dynamic Range)	f_{IN} = 350kHz	-	68.2	-	dB
THD (Total Harmonic Distortion)	f_{IN} = 350kHz	-	67	-	dB
R_{IN} Input Resistance		-	500	-	Ω
C_{IN} Input Capacitance		-	30	-	pF
Conversion Time		-	13	-	ADCLK[1]
Sampling Time		3	-	63	ADCLK2[2]

5.6.4 FU6812V

Table 5-48 ADC Electrical Characteristics of FU6812V

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	-	2	-	LSB
DNL (Differential Nonlinearity)	12-bit	-	1.5	-	LSB
OFFSET (Offset Error)	12-bit	-	10	-	LSB
SNR (Signal-to-noise Ratio)	f_{IN} = 350kHz	-	70.8	-	dB
ENOB (Effective Number of Bits)	f_{IN} = 350kHz	-	10.5	-	bit
SFDR (Spurious-free Dynamic Range)	f_{IN} = 350kHz	-	68.2	-	dB
THD (Total Harmonic Distortion)	f_{IN} = 350kHz	-	67	-	dB
R_{IN} Input Resistance		-	500	-	Ω
C_{IN} Input Capacitance		-	30	-	pF
Conversion Time		-	13	-	ADCLK[1]
Sampling Time		3	-	63	ADCLK2[2]

5.6.5 FU6861Q2

Table 5-49 ADC Electrical Characteristics of FU6861Q2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	-	2	-	LSB
DNL (Differential Nonlinearity)	12-bit	-	1.5	-	LSB
OFFSET (Offset Error)	12-bit	-	10	-	LSB
SNR (Signal-to-noise Ratio)	f_{IN} = 350kHz	-	70.8	-	dB
ENOB (Effective Number of Bits)	f_{IN} = 350kHz	-	10.5	-	bit
SFDR (Spurious-free Dynamic Range)	f_{IN} = 350kHz	-	68.2	-	dB
THD (Total Harmonic Distortion)	f_{IN} = 350kHz	-	67	-	dB
R_{IN} Input Resistance		-	500	-	Ω
C_{IN} Input Capacitance		-	30	-	pF
Conversion Time		-	13	-	ADCLK[1]
Sampling Time		3	-	63	ADCLK2[2]

5.6.6 FU6861L2

Table 5-50 ADC Electrical Characteristics of FU6861L2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	-	2	-	LSB
DNL (Differential Nonlinearity)	12-bit	-	1.5	-	LSB
OFFSET (Offset Error)	12-bit	-	10	-	LSB
SNR (Signal-to-noise Ratio)	f_{IN} = 350kHz	-	70.8	-	dB
ENOB (Effective Number of Bits)	f_{IN} = 350kHz	-	10.5	-	bit
SFDR (Spurious-free Dynamic Range)	f_{IN} = 350kHz	-	68.2	-	dB
THD (Total Harmonic Distortion)	f_{IN} = 350kHz	-	67	-	dB
R_{IN} Input Resistance		-	500	-	Ω
C_{IN} Input Capacitance		-	30	-	pF
Conversion Time		-	13	-	ADCLK[1]
Sampling Time		3	-	63	ADCLK2[2]

5.6.7 FU6861N2

Table 5-51 ADC Electrical Characteristics of FU6861N2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	-	2	-	LSB
DNL (Differential Nonlinearity)	12-bit	-	1.5	-	LSB
OFFSET (Offset Error)	12-bit	-	10	-	LSB
SNR (Signal-to-noise Ratio)	f_{IN} = 350kHz	-	70.8	-	dB
ENOB (Effective Number of Bits)	f_{IN} = 350kHz	-	10.5	-	bit
SFDR (Spurious-free Dynamic Range)	f_{IN} = 350kHz	-	68.2	-	dB
THD (Total Harmonic Distortion)	f_{IN} = 350kHz	-	67	-	dB
R_{IN} Input Resistance		-	500	-	Ω
C_{IN} Input Capacitance		-	30	-	pF
Conversion Time		-	13	-	ADCLK[1]
Sampling Time		3	-	63	ADCLK2[2]

5.6.8 FU6861NF2

Table 5-52 ADC Electrical Characteristics of FU6861NF2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	-	2	-	LSB
DNL (Differential Nonlinearity)	12-bit	-	1.5	-	LSB
OFFSET (Offset Error)	12-bit	-	10	-	LSB
SNR (Signal-to-noise Ratio)	f_{IN} = 350kHz	-	70.8	-	dB
ENOB (Effective Number of Bits)	f_{IN} = 350kHz	-	10.5	-	bit
SFDR (Spurious-free Dynamic Range)	f_{IN} = 350kHz	-	68.2	-	dB
THD (Total Harmonic Distortion)	f_{IN} = 350kHz	-	67	-	dB
R_{IN} Input Resistance		-	500	-	Ω
C_{IN} Input Capacitance		-	30	-	pF
Conversion Time		-	13	-	ADCLK[1]
Sampling Time		3	-	63	ADCLK2[2]

5.6.9 FU6862L

Table 5-53 ADC Electrical Characteristics of FU6862L

(T_A = 25℃ and VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	-	2	-	LSB
DNL (Differential Nonlinearity)	12-bit	-	1.5	-	LSB
OFFSET (Offset Error)	12-bit	-	6	-	LSB
SNR (Signal-to-noise Ratio)	f_{IN} = 350kHz	-	70.8	-	dB
ENOB (Effective Number of Bits)	f_{IN} = 350kHz	-	10.5	-	bit
SFDR (Spurious-free Dynamic Range)	f_{IN} = 350kHz	-	68.2	-	dB
THD (Total Harmonic Distortion)	f_{IN} = 350kHz	-	67	-	dB
R_{IN} Input Resistance		-	800	-	Ω
C_{IN} Input Capacitance		-	30	-	pF
Conversion Time		-	13	-	ADCLK[1]
Sampling Time		3	-	63	ADCLK2[2]

5.6.10 FU6862Q

Table 5-54 ADC Electrical Characteristics of FU6862Q

(T_A = 25℃ and VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	-	2	-	LSB
DNL (Differential Nonlinearity)	12-bit	-	1.5	-	LSB
OFFSET (Offset Error)	12-bit	-	6	-	LSB
SNR (Signal-to-noise Ratio)	f_{IN} = 350kHz	-	70.8	-	dB
ENOB (Effective Number of Bits)	f_{IN} = 350kHz	-	10.5	-	bit
SFDR (Spurious-free Dynamic Range)	f_{IN} = 350kHz	-	68.2	-	dB
THD (Total Harmonic Distortion)	f_{IN} = 350kHz	-	67	-	dB
R_{IN} Input Resistance		-	800	-	Ω
C_{IN} Input Capacitance		-	30	-	pF
Conversion Time		-	13	-	ADCLK[1]
Sampling Time		3	-	63	ADCLK2[2]

5.6.11 FU6872P

Table 5-55 ADC Electrical Characteristics of FU6872P

(T_A = 25℃ and VCC = 15V ~ 75V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	-	2	-	LSB
DNL (Differential Nonlinearity)	12-bit	-	1.5	-	LSB
OFFSET (Offset Error)	12-bit	-	6	-	LSB
SNR (Signal-to-noise Ratio)	f_{IN} = 350kHz	-	70.8	-	dB
ENOB (Effective Number of Bits)	f_{IN} = 350kHz	-	10.5	-	bit
SFDR (Spurious-free Dynamic Range)	f_{IN} = 350kHz	-	68.2	-	dB
THD (Total Harmonic Distortion)	f_{IN} = 350kHz	-	67	-	dB
R_{IN} Input Resistance		-	800	-	Ω
C_{IN} Input Capacitance		-	30	-	pF
Conversion Time		-	13	-	ADCLK[1]
Sampling Time		3	-	63	ADCLK2[2]

Note

[1] ADCLK = 24MHz

[2] ADCLK2 = 12MHz

5.7 VREF and VHALF Electrical Characteristics

5.7.1 FU6812L2

Table 5-56 VREF and VHALF Electrical Characteristics of FU6812L2

(T_A = -40℃ ~ 85℃, VCC = 15V and VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	VDD5	5.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4	4.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3	3.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 11	VREF/2 + 0.2	VREF/2	VREF/2 - 0.2	V

5.7.2 FU6812N2

Table 5-57 VREF and VHALF Electrical Characteristics of FU6812N2

(T_A = -40℃ ~ 85℃, VCC = 15V and VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	VDD5	5.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4	4.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3	3.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 11	VREF/2 + 0.2	VREF/2	VREF/2 - 0.2	V

5.7.3 FU6812S2

Table 5-58 VREF and VHALF Electrical Characteristics of FU6812S2

(T_A = -40℃ ~ 85℃, VCC = 15V and VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	VDD5	5.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4	4.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3	3.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 11	VREF/2 + 0.2	VREF/2	VREF/2 - 0.2	V

5.7.4 FU6812V

Table 5-59 VREF and VHALF Electrical Characteristics of FU6812V

(T_A = -40℃ ~ 85℃, VCC = 15V and VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	VDD5	5.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4	4.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3	3.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 11	VREF/2 + 0.2	VREF/2	VREF/2 - 0.2	V

5.7.5 FU6861Q2

Table 5-60 VREF and VHALF Electrical Characteristics of FU6861Q2

(T_A = -40℃ ~ 85℃, VCC = 15V and VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	VDD5	5.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4	4.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3	3.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 11	VREF/2 + 0.2	VREF/2	VREF/2 - 0.2	V

5.7.6 FU6861L2

Table 5-61 VREF and VHALF Electrical Characteristics of FU6861L2

(T_A = -40℃ ~ 85℃, VCC = 15V and VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	VDD5	5.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4	4.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3	3.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 11	VREF/2 + 0.2	VREF/2	VREF/2 - 0.2	V

5.7.7 FU6861N2

Table 5-62 VREF and VHALF Electrical Characteristics of FU6861N2

(T_A = -40℃ ~ 85℃, VCC = 15V and VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	VDD5	5.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4	4.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3	3.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 11	VREF/2 + 0.2	VREF/2	VREF/2 - 0.2	V

5.7.8 FU6861NF2

Table 5-63 VREF and VHALF Electrical Characteristics of FU6861NF2

(T_A = -40℃ ~ 85℃, VCC = 15V and VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	VDD5	5.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4	4.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3	3.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 11	VREF/2 + 0.2	VREF/2	VREF/2 - 0.2	V

5.7.9 FU6862L

Table 5-64 VREF and VHALF Electrical Characteristics of FU6862L

(T_A = -40℃ ~ 85℃ and VCC = 12V ~ 20V)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	VDD5	5.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4	4.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3	3.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 11	VREF/2 + 0.2	VREF/2	VREF/2 - 0.2	V

5.7.10 FU6862Q

Table 5-65 VREF and VHALF Electrical Characteristics of FU6862Q

(T_A = -40℃ ~ 85℃ and VCC = 12V ~ 20V)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	VDD5	5.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4	4.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3	3.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 11	VREF/2 + 0.2	VREF/2	VREF/2 - 0.2	V

5.7.11 FU6872P

Table 5-66 VREF and VHALF Electrical Characteristics of FU6872P

(T_A = -40℃ ~ 85℃, VCC = 15V ~ 75V)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 01	4.8	VDD5	5.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 11	VREF/2 + 0.2	VREF/2	VREF/2 - 0.2	V

5.8 Operational Amplifier Electrical Characteristics

5.8.1 FU6812L2

Table 5-67 Operational Amplifier Electrical Characteristics of FU6812L2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ICMR} Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
V_{OS} Operational Amplifier Offset Voltage	T_A = 25℃	-	5	10	mV
A_{OL} Open-loop Gain	R_L = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (U_{GBW})	C_L = 40pF	6	10	-	MHz
Slew Rate (SR)	C_L = 40pF	10	15	-	V/μs
Operational Amplifier Gain[1][2]	CMP_AMP[AMP0_GAIN] = 001	1.88	2	2.12	-
	CMP_AMP[AMP0_GAIN] = 010	3.76	4	4.24	-
	CMP_AMP[AMP0_GAIN] = 011	7.5	8	8.5	-
	CMP_AMP[AMP0_GAIN] = 100	15	16	17	-

5.8.2 FU6812N2

Table 5-68 Operational Amplifier Electrical Characteristics of FU6812N2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ICMR} Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
V_{OS} Operational Amplifier Offset Voltage	T_A = 25℃	-	5	10	mV
A_{OL} Open-loop Gain	R_L = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (U_{GBW})	C_L = 40pF	6	10	-	MHz
Slew Rate (SR)	C_L = 40pF	10	15	-	V/μs
Operational Amplifier Gain[1][2]	CMP_AMP[AMP0_GAIN] = 001	1.88	2	2.12	-
	CMP_AMP[AMP0_GAIN] = 010	3.76	4	4.24	-
	CMP_AMP[AMP0_GAIN] = 011	7.5	8	8.5	-
	CMP_AMP[AMP0_GAIN] = 100	15	16	17	-

5.8.3 FU6812S2

Table 5-69 Operational Amplifier Electrical Characteristics of FU6812S2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ICMR} Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
V_{OS} Operational Amplifier Offset Voltage	T_A = 25℃	-	5	10	mV
A_{OL} Open-loop Gain	R_L = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (U_{GBW})	C_L = 40pF	6	10	-	MHz
Slew Rate (SR)	C_L = 40pF	10	15	-	V/μs
Operational Amplifier Gain[1][2]	CMP_AMP[AMP0_GAIN] = 001	1.88	2	2.12	-
	CMP_AMP[AMP0_GAIN] = 010	3.76	4	4.24	-
	CMP_AMP[AMP0_GAIN] = 011	7.5	8	8.5	-
	CMP_AMP[AMP0_GAIN] = 100	15	16	17	-

5.8.4 FU6812V

Table 5-70 Operational Amplifier Electrical Characteristics of FU6812V

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ICMR} Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
V_{OS} Operational Amplifier Offset Voltage	T_A = 25℃	-	5	10	mV
A_{OL} Open-loop Gain	R_L = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (U_{GBW})	C_L = 40pF	6	10	-	MHz
Slew Rate (SR)	C_L = 40pF	10	15	-	V/μs
Operational Amplifier Gain[1][2]	CMP_AMP[AMP0_GAIN] = 001	1.88	2	2.12	-
	CMP_AMP[AMP0_GAIN] = 010	3.76	4	4.24	-
	CMP_AMP[AMP0_GAIN] = 011	7.5	8	8.5	-
	CMP_AMP[AMP0_GAIN] = 100	15	16	17	-

5.8.5 FU6861Q2

Table 5-71 Operational Amplifier Electrical Characteristics of FU6861Q2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ICMR} Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
V_{OS} Operational Amplifier Offset Voltage	T_A = 25℃	-	5	10	mV
A_{OL} Open-loop Gain	R_L = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (U_{GBW})	C_L = 40pF	6	10	-	MHz
Slew Rate (SR)	C_L = 40pF	10	15	-	V/μs
Operational Amplifier Gain[1][2]	CMP_AMP[AMP0_GAIN] = 001	1.88	2	2.12	-
	CMP_AMP[AMP0_GAIN] = 010	3.76	4	4.24	-
	CMP_AMP[AMP0_GAIN] = 011	7.5	8	8.5	-
	CMP_AMP[AMP0_GAIN] = 100	15	16	17	-

5.8.6 FU6861L2

Table 5-72 Operational Amplifier Electrical Characteristics of FU6861L2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ICMR} Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
V_{OS} Operational Amplifier Offset Voltage	T_A = 25℃	-	5	10	mV
A_{OL} Open-loop Gain	R_L = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (U_{GBW})	C_L = 40pF	6	10	-	MHz
Slew Rate (SR)	C_L = 40pF	10	15	-	V/μs
Operational Amplifier Gain[1][2]	CMP_AMP[AMP0_GAIN] = 001	1.88	2	2.12	-
	CMP_AMP[AMP0_GAIN] = 010	3.76	4	4.24	-
	CMP_AMP[AMP0_GAIN] = 011	7.5	8	8.5	-
	CMP_AMP[AMP0_GAIN] = 100	15	16	17	-

5.8.7 FU6861N2

Table 5-73 Operational Amplifier Electrical Characteristics of FU686N2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ICMR} Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
V_{OS} Operational Amplifier Offset Voltage	T_A = 25℃	-	5	10	mV
A_{OL} Open-loop Gain	R_L = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (U_{GBW})	C_L = 40pF	6	10	-	MHz
Slew Rate (SR)	C_L = 40pF	10	15	-	V/μs
Operational Amplifier Gain[1][2]	CMP_AMP[AMP0_GAIN] = 001	1.88	2	2.12	-
	CMP_AMP[AMP0_GAIN] = 010	3.76	4	4.24	-
	CMP_AMP[AMP0_GAIN] = 011	7.5	8	8.5	-
	CMP_AMP[AMP0_GAIN] = 100	15	16	17	-

5.8.8 FU6861NF2

Table 5-74 Operational Amplifier Electrical Characteristics of FU6861NF2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ICMR} Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
V_{OS} Operational Amplifier Offset Voltage	T_A = 25℃	-	5	10	mV
A_{OL} Open-loop Gain	R_L = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (U_{GBW})	C_L = 40pF	6	10	-	MHz
Slew Rate (SR)	C_L = 40pF	10	15	-	V/μs
Operational Amplifier Gain[1][2]	CMP_AMP[AMP0_GAIN] = 001	1.88	2	2.12	-
	CMP_AMP[AMP0_GAIN] = 010	3.76	4	4.24	-
	CMP_AMP[AMP0_GAIN] = 011	7.5	8	8.5	-
	CMP_AMP[AMP0_GAIN] = 100	15	16	17	-

5.8.9 FU6862L

Table 5-75 Operational Amplifier Electrical Characteristics of FU6862L

(T_A = 25℃ and VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ICMR} Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
V_{OS} Operational Amplifier Offset Voltage	T_A = 25℃	-	5	10	mV
A_{OL} Open-loop Gain	R_L = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (U_{GBW})	C_L = 40pF	6	10	-	MHz
Slew Rate (SR)	C_L = 40pF	10	15	-	V/μs
Operational Amplifier Gain[1][2]	CMP_AMP[AMP0_GAIN] = 001	1.88	2	2.12	-
	CMP_AMP[AMP0_GAIN] = 010	3.76	4	4.24	-
	CMP_AMP[AMP0_GAIN] = 011	7.5	8	8.5	-
	CMP_AMP[AMP0_GAIN] = 100	15	16	17	-

5.8.10 FU6862Q

Table 5-76 Operational Amplifier Electrical Characteristics of FU6862Q

(T_A = 25℃ and VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ICMR} Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
V_{OS} Operational Amplifier Offset Voltage	T_A = 25℃	-	5	10	mV
A_{OL} Open-loop Gain	R_L = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (U_{GBW})	C_L = 40pF	6	10	-	MHz
Slew Rate (SR)	C_L = 40pF	10	15	-	V/μs
Operational Amplifier Gain[1][2]	CMP_AMP[AMP0_GAIN] = 001	1.88	2	2.12	-
	CMP_AMP[AMP0_GAIN] = 010	3.76	4	4.24	-
	CMP_AMP[AMP0_GAIN] = 011	7.5	8	8.5	-
	CMP_AMP[AMP0_GAIN] = 100	15	16	17	-

5.8.11 FU6872P

Table 5-77 Operational Amplifier Electrical Characteristics of FU6872P

(T_A = 25℃ and VCC = 15V ~ 75V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ICMR} Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
V_{OS} Operational Amplifier Offset Voltage	T_A = 25℃	-	5	10	mV
A_{OL} Open-loop Gain	R_L = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (U_{GBW})	C_L = 40pF	6	10	-	MHz
Slew Rate (SR)	C_L = 40pF	10	15	-	V/μs
Operational Amplifier Gain[1][2]	CMP_AMP[AMP0_GAIN] = 001	1.88	2	2.12	-
	CMP_AMP[AMP0_GAIN] = 010	3.76	4	4.24	-
	CMP_AMP[AMP0_GAIN] = 011	7.5	8	8.5	-
	CMP_AMP[AMP0_GAIN] = 100	15	16	17	-

Note

[1] The operational amplifier gain is measured when both positive and negative inputs of the operational amplifier are connected in series with 1kΩ resistors. The operational amplifier gain varies with external resistors

[2] AMP0 is used as an example. For other operational amplifiers, see CMP_AMP (0x40F2) for the

configurationsCMP_AMP (0x40F2)

5.9 BEMF Electrical Characteristics

5.9.1 FU6812L2

Table 5-78 BEMF Electrical Characteristics of FU6812L2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor		5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.2 FU6812N2

Table 5-79 BEMF Electrical Characteristics of FU6812N2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor		5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.3 FU6812S2

Table 5-80 BEMF Electrical Characteristics of FU6812S2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor		5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.4 FU6812V

Table 5-81 BEMF Electrical Characteristics of FU6812V

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor		5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.5 FU6861Q2

Table 5-82 BEMF Electrical Characteristics of FU6861Q2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor		5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.6 FU6861L2

Table 5-83 BEMF Electrical Characteristics of FU6861L2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor		5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.7 FU6861N2

Table 5-84 BEMF Electrical Characteristics of FU6861N2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor		5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.8 FU6861NF2

Table 5-85 BEMF Electrical Characteristics of FU6861NF2

(T_A = 25℃, VCC = 15V and VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor		5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.9 FU6862L

Table 5-86 BEMF Electrical Characteristics of FU6862L

(T_A = 25℃ and VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor		5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.10 FU6862Q

Table 5-87 BEMF Electrical Characteristics of FU6862Q

(T_A = 25℃ and VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor		5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.11 FU6872P

Table 5-88 BEMF Electrical Characteristics of FU6872P

(T_A = 25℃ and VCC = 15V ~ 75V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor		5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.10 OSC Electrical Characteristics

5.10.1 FU6812L2

Table 5-89 OSC Electrical Characteristics of FU6812L2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.2 FU6812N2

Table 5-90 OSC Electrical Characteristics of FU6812N2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.3 FU6812S2

Table 5-91 OSC Electrical Characteristics of FU6812S2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.4 FU6812V

Table 5-92 OSC Electrical Characteristics of FU6812V

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.5 FU6861Q2

Table 5-93 OSC Electrical Characteristics of FU6861Q2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.6 FU6861L2

Table 5-94 OSC Electrical Characteristics of FU6861L2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.7 FU6861N2

Table 5-95 OSC Electrical Characteristics of FU6861N2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.8 FU6861NF2

Table 5-96 OSC Electrical Characteristics of FU6861NF2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.9 FU6862L

Table 5-97 OSC Electrical Characteristics of FU6862L

(T_A = -40℃ ~ 85℃ and VCC = 12V ~ 20V)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.10 FU6862Q

Table 5-98 OSC Electrical Characteristics of FU6862Q

(T_A = -40℃ ~ 85℃ and VCC = 12V ~ 20V)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.11 FU6872P

Table 5-99 OSC Electrical Characteristics of FU6872P

(T_A = -40℃ ~ 85℃, VCC = 15V ~ 75V)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
Low-speed Clock Rate		29	32.8	37	kHz

Note

Note SYSCLK refers to system clock rate, and T to system clock cycle. Unless otherwise specified, the system clock rate of chip is 24MHz and T = 1/SYSCLK

5.11 Reset Electrical Characteristics

5.11.1 FU6812L2

Table 5-100 Reset Electrical Characteristics of FU6812L2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time to Reset to Low Level		50	-	-	μs

5.11.2 FU6812N2

Table 5-101 Reset Electrical Characteristics of FU6812N2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time to Reset to Low Level		50	-	-	μs

5.11.3 FU6812S2

Table 5-102 Reset Electrical Characteristics of FU6812S2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time to Reset to Low Level		50	-	-	μs

5.11.4 FU6812V

Table 5-103 Reset Electrical Characteristics of FU6812V

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time to Reset to Low Level		50	-	-	μs

5.11.5 FU6861Q2

Table 5-104 Reset Electrical Characteristics of FU6861Q2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time to Reset to Low Level		50	-	-	μs

5.11.6 FU6861L2

Table 5-105 Reset Electrical Characteristics of FU6861L2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time to Reset to Low Level		50	-	-	μs

5.11.7 FU6861N2

Table 5-106 Reset Electrical Characteristics of FU6861N2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time to Reset to Low Level		50	-	-	μs

5.11.8 FU6861NF2

Table 5-107 Reset Electrical Characteristics of FU6861NF2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time to Reset to Low Level		50	-	-	μs

5.11.9 FU6862L

Table 5-108 Reset Electrical Characteristics of FU6862L

(T_A = -40℃ ~ 85℃, VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time to Reset to Low Level		50	-	-	μs

5.11.10 FU6862Q

Table 5-109 Reset Electrical Characteristics of FU6862Q

(T_A = -40℃ ~ 85℃, VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time to Reset to Low Level		50	-	-	μs

5.11.11 FU6872P

Table 5-110 Reset Electrical Characteristics of FU6872P

(T_A = -40℃ ~ 85℃, VCC = 15V ~ 75V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time for RSTN Released to Low		50	-	-	μs
VDD5 Reset Threshold	Reset Voltage LVR = 3.0V	2.8	3.0	3.2	V

5.12 LDO Electrical Characteristics

5.12.1 FU6812L2

Table 5-111 LDO Electrical Characteristics of FU6812L2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Voltage	VCC = 7V ~ 24V, VCC_MODE = 0	4.8	5	5.2	V
VDD18 Voltage		-	1.85	-	V

5.12.2 FU6812N2

Table 5-112 LDO Electrical Characteristics of FU6812N2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Voltage	VCC = 7V ~ 24V, VCC_MODE = 0	4.8	5	5.2	V
VDD18 Voltage		-	1.85	-	V

5.12.3 FU6812S2

Table 5-113 LDO Electrical Characteristics of FU6812S2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Voltage	VCC = 7V ~ 24V, VCC_MODE = 0	4.8	5	5.2	V
VDD18 Voltage		-	1.85	-	V

5.12.4 FU6812V

Table 5-114 LDO Electrical Characteristics of FU6812V

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Voltage	VCC = 7V ~ 24V, VCC_MODE = 0	4.8	5	5.2	V
VDD18 Voltage		-	1.85	-	V

5.12.5 FU6861Q2

Table 5-115 LDO Electrical Characteristics of FU6861Q2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Voltage	VCC = 7V ~ 24V, VCC_MODE = 0	4.8	5	5.2	V
VDD18 Voltage		-	1.85	-	V

5.12.6 FU6861L2

Table 5-116 LDO Electrical Characteristics of FU6861L2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Voltage	VCC = 7V ~ 24V, VCC_MODE = 0	4.8	5	5.2	V
VDD18 Voltage		-	1.85	-	V

5.12.7 FU6861N2

Table 5-117 LDO Electrical Characteristics of FU6861N2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Voltage	VCC = 7V ~ 24V, VCC_MODE = 0	4.8	5	5.2	V
VDD18 Voltage		-	1.85	-	V

5.12.8 FU6861NF2

Table 5-118 LDO Electrical Characteristics of FU6861NF2

(T_A = -40℃ ~ 85℃, VCC = 5V ~ 24V, VCC_MODE = 0 unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Voltage	VCC = 7V ~ 24V, VCC_MODE = 0	4.8	5	5.2	V
VDD18 Voltage		-	1.85	-	V

5.12.9 FU6862L

Table 5-119 LDO Electrical Characteristics of FU6862L

(T_A = -40℃ ~ 85℃, VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Voltage	VCC = 12V ~ 20V	4.7	5	5.2	V
VDD18 Voltage		-	1.85	-	V

5.12.10 FU6862Q

Table 5-120 LDO Electrical Characteristics of FU6862Q

(T_A = -40℃ ~ 85℃, VCC = 12V ~ 20V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Voltage	VCC = 12V ~ 20V	4.8	5	5.2	V
VDD18 Voltage		-	1.85	-	V

5.12.11 FU6872P

Table 5-121 LDO Electrical Characteristics of FU6872P

(T_A = -40℃ ~ 85℃, VCC = 15V ~ 75V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREG Voltage		10	12	13	V
VDD5 Voltage		4.8	5	5.2	V
VDD18 Voltage		-	1.85	-	V

5.13 Package Thermal Resistance

5.13.1 FU6812L2 LQFP48

Table 5-122 LQFP48 Package Thermal Resistance of FU6812L2

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	52.4	℃/W
	JEDEC standard, 1S0P PCB	72.2	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	17	℃/W

5.13.2 FU6861L2 LQFP48

Table 5-123 LQFP48 Package Thermal Resistance of FU6861L2

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	52.4	℃/W
	JEDEC standard, 1S0P PCB	72.2	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	17	℃/W

5.13.3 FU6862L LQFP48

Table 5-124 LQFP48 Package Thermal Resistance of FU6862L

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	52.4	℃/W
	JEDEC standard, 1S0P PCB	72.2	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	17	℃/W

5.13.4 FU6812N2 QFN32

Table 5-125 QFN32 Package Thermal Resistance of FU6812N2

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	47	℃/W
	JEDEC standard, 1S0P PCB	74	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	20	℃/W

5.13.5 FU6812S2 SSOP24

Table 5-126 SSOP24 Package Thermal Resistance of FU6812S2

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	75	℃/W

5.13.6 FU6812V SSOP24

Table 5-127 Package Thermal Resistance of FU6812V

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	75	℃/W

5.13.7 FU6811Q QFN56

Table 5-128 QFN56 Package Thermal Resistance of FU6861Q2

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	33	℃/W

Parameter	Test Conditions	Typ.	Unit
	JEDEC standard, 1S0P PCB	55	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	9.2	℃/W

5.13.8 FU6861N2 QFN40

Table 5-129 QFN40 Package Thermal Resistance of FU6861N2

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	40	℃/W
	JEDEC standard, 1S0P PCB	66	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	12	℃/W

5.13.9 FU6861NF2 QFN40

Table 5-130 QFN40 Package Thermal Resistance of FU6861NF2

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	40	℃/W
	JEDEC standard, 1S0P PCB	66	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	12	℃/W

5.13.10 FU6862Q QFN48-38

Table 5-131 QFN48_38 Package Thermal Resistance of FU6862Q

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	33	℃/W
	JEDEC standard, 1S0P PCB	55	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	9.2	℃/W

5.13.11 FU6872P PLQFN32

Table 5-132 LQFP52 Package Thermal Resistance of FU6872P

Parameter	Test Conditions	Typ.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	30	℃/W
	JEDEC standard, 1S0P PCB	40	℃/W
Junction-to-case Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	15	℃/W

Note

[1] The actual measurements may vary depending on the conditions

6 Reset Control

6.1 Reset Sources (RST_SR)

The chip includes a reset circuitry with 6 reset sources:

- Power-on reset (RSTPOW)
- External pin reset (RSTEXT)
- Low voltage detection reset (RSTLVD)
- Watchdog timer reset (RSTWDT)
- Flash error detector reset (RSTFED)
- Debug reset (RSTDBG)

The reset flag is queryable and recorded in register RST_SR. Following the last reset, the affected reset flag is set to “1” and all other reset flags are cleared to “0”. In order to clear reset flags, you can also set RST_SR[RSTCLR] flag to “1” so that RST_SR[7:3] are cleared.

6.2 Reset Enable

See the corresponding control registers. RSTLVD and RSTWDT are always enabled.

6.3 External Pin Reset and Power-on Reset

The chip resets when RSTN pin remains low for 50μs. After reset, MCU starts the program from address 0x0000. The chip resets when the chip powers on and the voltage settles above the reset voltage threshold.

6.4 Low Voltage Detection Reset

The chip’s internal circuitry monitors VCC voltage. When VCC voltage drops to a level below the reset voltage threshold, the internal monitor circuitry sends the reset signal to reset the chip.

Configuring corresponding register enables the low voltage monitor circuitry and sets the low voltage threshold.

6.5 Watchdog Timer Reset

After the watchdog timer (WDT) is enabled, the software periodically clears WDT to avoid timeout. If system error occurs, the timer generates an output pulse to reset the chip.

6.6 Flash Error Detector Reset

The Flash memory can be programmed for read/write/erase operations with MOVX instructions. A Flash error detector reset (RSTFED) occurs if a Flash erase is attempted targeting the last sector (0x3F80 ~ 0x3FFF) or a Flash write is attempted targeting the last byte (0x7FFF). RSTFED is always enabled and cannot be disabled.

6.7 Debug Reset

Click Reset button of IDE to send a debug reset signal when the chip enters the debug state.

6.8 Reset Registers

6.8.1 RST_SR (0xC9)

Bit	7	6	5	4	3	2	1	0
Name	RSTPOW	RSTEXT	RSTLVD	RSV	RSTWDT	RSTFED	RSTDBG	RSTCLR
Type	R	R	R	-	R	R	R	W1
Reset	-	-	-	-	-	-	-	0

Bit	Name	Description
[7]	RSTPOW	Power-On Reset Flag 0: Last reset was not a power-on reset. 1: Last reset was a power-on reset.
[6]	RSTEXT	External Pin Reset Flag 0: Last reset was not an external pin reset. 1: Last reset was an external pin reset.
[5]	RSTLVD	Low Voltage Detection (LVD) Reset Flag 0: Last reset was not an LVD reset. 1: Last reset was an LVD reset.
[4]	RSV	Reserved
[3]	RSTWDT	Watchdog Timer Reset Flag 0: Last reset was not a watchdog timer reset.

		1: Last reset was a watchdog timer reset.
[2]	RSTFED	Flash Error Detector Reset Flag 0: Last reset was not a Flash error detector reset. 1: Last reset was a Flash error detector reset.
[1]	RSTDBG	Debug Reset Flag 0: Last reset was not a debug reset. 1: Last reset was a debug reset.
[0]	RSTCLR	Reset Bits Clear Flag A write of “1” clears the reset bits RRST_SR[7:3]. It has no effect when this bit is read.

7 Interrupt

7.1 Interrupt Introduction

16 reset sources in FU6816_66Q1: Each interrupt source can be individually programmed in IP0 ~ IP3 registers with one of four priority levels. Interrupt flags (IF) are located in an SFRs or XSFRs. The associated IF is set by the hardware to 1 when the internal circuitry or an external source meets the interrupt conditions. If IE[EA] = 1 and both the associated interrupt EA and IF bits are set to 1, an interrupt request is generated and sent to CPU. If no other interrupt service routine (ISR) of greater priority is currently being serviced, the system enters interrupt state to service the requesting ISR.

Every interrupt source except the reset interrupt can be assigned a priority level. The low-priority interrupt can be preempted by the high-priority interrupt. When the high-priority interrupt service routine (ISR) completes, the system switches to the low-priority interrupt. Interrupts with the same priority cannot preempt each other. The interrupt priority register allows individual priority configuration for each interrupt. A setting value of 0 to 3 indicates priorities from low to high respectively, with 0 as the default value. If two interrupt requests occur simultaneously, the one with higher priority shall be serviced first. If two interrupt sources have the same priority, arbitration follows a fixed pre-defined order. The detailed list of interrupt sources and their arbitration order are shown in Table 7-1. Wherein, the smaller the number, the higher the priority.

7.2 Interrupt Source Enable

IE[EA] is global interrupt enable bit and no interrupt request is responded when IE[EA] = 0.

You can enable or disable a certain interrupt source individually via configuring a related interrupt enable bit in SFR or XSFR. The interrupt source shall only be recognized after enabling global interrupts. The interrupt register set to 1 shall be kept after the global interrupt enable register or individual interrupt enable bits are cleared to 0. When the corresponded enable bit is set to 1, the interrupt with bit set to 1 is immediately entered. Therefore, before enable bit is set to 1, you shall clear the corresponded interrupt bit to 0.

7.3 External Interrupt

The external interrupt has 2 interrupt sources: INT0 and INT1. They both can be configured as interrupt on rising edge, interrupt on falling edge or interrupt on edge changes (rise or fall).

GPIO ports that trigger INT1 vary by chip models. See more details in Pin Definitions. The digital input signals from P0.0 ~ P0.6 or P1.1 or the output signals from CMP4 can be used to trigger an INT0. If use P0.0~P0.6 or CMP4 output as interrupt source of INT0, you shall is configure LVSR[EXT0CFG] bit. If use P1.1 as interrupt source of INT0, you shall configure EXT0[EXT0_P11]. These trigger sources share one interrupt entry point, one interrupt flag bit TCON[IF0] and one interrupt enable bit IE[EX0]. TCON[IT0] bit selects the interrupt edge. IP0[PX0] bit configures the priority level.

The digital input signals from P1.0 ~ P1.7 or P2.0 ~ P2.7 can be used to trigger an INT1. If P1.1 is selected, EXT0[EXT0_P11] must be set as 1. P1_IF and P2_IF are interrupt flag bits, and P1_IE and P2_IE are interrupt enable bits. Each trigger source has a corresponding interrupt flag bit and an interrupt enable bit. INT1 can select multiple trigger sources that are recognized by P1_IF and P2_IF in the interrupt subroutine. These 16 interrupt sources share one interrupt entry and one interrupt enable bit IE[EX1]. To enable INT1, first set IE[EX1] to “1” and then configure the corresponding enable bit. The interrupt edge is configured by TCON[IT1] bit, and the priority level by IP0[PX1] bit. See 7.5.7 P1_IE (0xD1) ~ 7.5.10 P2_IF (0xD4) for INT1 interrupt flags and enable registers

7.4 Interrupt Introduction

Table 7-1 Interrupt Introduction

Interrupt Source	Priority Order	Vector Address	Interrupt Flag	Cleared by Software?	Enable Bit	Priority Control
Reset	Highest	0x0000	None	N	Always enabled	Highest
LVW Interrupt	0	0x0003	LVSR[0]	Y	CCFG1[6]	IP0[1:0]
INT0	1	0x000B	TCON[2]	Y	IE[0]	IP0[3:2]
INT1	2	0x0013	P1_IF[7:0] P2_IF[7:0]	Y	IE[2]	IP0[5:4]
FG Interrupt Driver CM Interrupt	3	0x001B	DRV_SR[5:4]	Y	DRV_SR[3] DRV_SR[2:0]	IP0[7:6]
Timer2 Interrupt	4	0x0023	TIM2_CR1[7:5]	Y	TIM2_CR1[4:3] TIM2_CR0[3]	IP1[1:0]

Interrupt Source	Priority Order	Vector Address	Interrupt Flag	Cleared by Software?	Enable Bit	Priority Control
Timer1 Interrupt	5	0x002B	TIM1_SR[5:0]	Y	TIM1_IER[5:0]	IP1[3:2]
ADC Interrupt	6	0x0033	ADC_CR[0]	Y	ADC_CR[1]	IP1[5:4]
CMP0/1/2/ CMP3 Interrupt5	7	0x003B	CMP_SR[7:4]	Y	CMP_CR0[7:0]	IP1[7:6]
RTC Interrupt	8	0x0043	RTC_STA[6]	Y	IE[6]	IP2[1:0]
Timer3 Interrupt	9	0x004B	TIM3_CR1[7:5]	Y	TIM3_CR1[4:3] TIM3_CR0[3]	IP2[3:2]
Systick Interrupt Timer4 Interrupt	10	0x0053	DRV_SR[7] TIM4_CR1[7:5]	Y	DRV_SR[6] TIM4_CR1[4:3] TIM4_CR0[3]	IP2[5:4]
TSD Interrupt	11	0x005B	TCON[5]	Y	IE[1]	IP2[7:6]
UART Interrupt	12	0x0063	UT_CR[1:0]	Y	IE[4]	IP3[1:0]
I^2C Interrupt	13	0x006B	I2C_SR[0]	Y	I2C_CR[0]	IP3[3:2]
SPI Interrupt	14	0x0073	SPI_CR1[7]	Y	SPI_CR1[0]	IP3[5:4]
DMA Interrupt	15	0x007B	DMA0_CR0[7] DMA1_CR0[7]	Y	DMA0_CR0[2]	IP3[7:6]

Note

[1] 16 reset sources in the chip as the table above shows. Each interrupt source can be individually programmed in IP0 ~ IP3 registers with one of four priority levels. If two interrupts are at the same level, their priority order follows the specifications in the table above, where a smaller index indicates higher priority. New interrupts cannot preempt ongoing interrupt processing of the same priority level

[2] IE[EA] is the global interrupt enable. When EA = 0, all interrupt requests are ignored

7.5 Interrupt Registers

7.5.1 IE (0xA8)

Bit	7	6	5	4	3	2	1	0
Name	EA	RTCIE	RSV	ES0	SPIIE	EX1	TSDIE	EX0
Type	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W
Reset	0	0	-	0	0	0	0	0

Bit	Name	Description
[7]	EA	All Interrupts Enable 0: Disable 1: Enable
[6]	RTCIE	RTC Interrupt Enable 0: Disable 1: Enable
[5]	RSV	Reserved
[4]	ES0	UART Interrupt Enable 0: Disable 1: Enable
[3]	SPIIE	SPI Interrupt Enable 0: Disable 1: Enable
[2]	EX1	INT1 Enable 0: Disable 1: Enable
[1]	TSDIE	TSD Interrupt Enable 0: Disable 1: Enable
[0]	EX0	INT0 Enable 0: Disable 1: Enable

7.5.2 IP0 (0xB8)

Bit	7	6	5	4	3	2	1	0
Name	PDRV		PX1		PX0		PLVW	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:6]	PDRV	Driver Compare Match Interrupt Priority Setting

[5:4]	PX1	External Interrupt 1 (INT1) Priority Setting
[3:2]	PX0	External Interrupt 0 (INT0) Priority Setting
[1:0]	PLVW	LVW Interrupt Priority Setting

Note

Priority level assigned ascends from 0 to 3, totaling 4 levels

7.5.3 IP1 (0xC0)

Bit	7	6	5	4	3	2	1	0
Name	PCMP		PADC		PTIM1		PTIM2	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:6]	PCMP	CMP0/1/2 and CMP3 Interrupt Priority Setting
[5:4]	PADC	ADC Interrupt Priority Setting
[3:2]	PTIM1	Timer1 Interrupt Priority Setting
[1:0]	PTIM2	Timer2 Interrupt Priority Setting

Note

Priority level assigned ascends from 0 to 3, totaling 4 levels

7.5.4 IP2 (0xC8)

Bit	7	6	5	4	3	2	1	0
Name	PTSD		PTIM4		PTIM3		PRTC	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:6]	PTSD	TSD Interrupt Priority Setting
[5:4]	PTIM4	Timer4 and Systick Interrupt Priority Setting
[3:2]	PTIM3	Timer3 Interrupt Priority Setting
[1:0]	PRTC	RTC Interrupt Priority Setting

Note

Priority level assigned ascends from 0 to 3, totaling 4 levels

7.5.5 IP3 (0xD8)

Bit	7	6	5	4	3	2	1	0
Name	PDMA		PSPI		PI2C		PUART	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:6]	PDMA	DMA Interrupt Priority Setting
[5:4]	PSPI	SPI Interrupt Priority Setting
[3:2]	PI2C	I^2C Interrupt Priority Setting
[1:0]	PUART	UART Interrupt Priority Setting

Note

Priority level assigned ascends from 0 to 3, totaling 4 levels

7.5.6 TCON (0x88)

Bit	7	6	5	4	3	2	1	0
Name	RSV		TSDIF	IT1		IF0	IT0	
Type	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	-	0	0	0	0	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5]	TSDIF	TSD Interrupt Flag This bit is set by hardware to “1” when an over-temperature event occurs. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[4:3]	IT1	INT1 Trigger Level Selection 00: Interrupt on rising edge 01: Interrupt on falling edge 1X: Interrupt on edge changes (rise or fall)
[2]	IF0	External Interrupt 0 (INT0) Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0”

		1: No effect
[1:0]	IT0	INT0 Trigger Level Selection 00: Interrupt on rising edge 01: Interrupt on falling edge 1X: Interrupt on edge changes (rise or fall)

7.5.7 P1_IE (0xD1)

Bit	7	6	5	4	3	2	1	0
Name	P17_IE	P16_IE	P15_IE	P14_IE	P13_IE	P12_IE	P11_IE	P10_IE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	P17_IE	P1.7 INT1 Enable 0: Disable 1: Enable
[6]	P16_IE	P1.6 INT1 Enable 0: Disable 1: Enable
[5]	P15_IE	P1.5 INT1 Enable 0: Disable 1: Enable
[4]	P14_IE	P1.4 INT1 Enable 0: Disable 1: Enable
[3]	P13_IE	P1.3 INT1 Enable 0: Disable 1: Enable
[2]	P12_IE	P1.2 INT1 Enable 0: Disable 1: Enable
[1]	P11_IE	P1.1 INT1 Enable 0: Disable 1: Enable
[0]	P10_IE	P1.0 INT1 Enable 0: Disable 1: Enable

7.5.8 P1_IF (0xD2)

Bit	7	6	5	4	3	2	1	0
Name	P17_IF	P16_IF	P15_IF	P14_IF	P13_IF	P12_IF	P11_IF	P10_IF
Type	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0

Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	P17_IF	P1.7 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect
[6]	P16_IF	P1.6 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect
[5]	P15_IF	P1.5 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect
[4]	P14_IF	P1.4 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect
[3]	P13_IF	P1.3 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect
[2]	P12_IF	P1.2 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write:

		0: This bit is cleared to 0 1: No effect
[1]	P11_IF	P1.1 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect
[0]	P10_IF	P1.0 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect

7.5.9 P2_IE (0xD3)

Bit	7	6	5	4	3	2	1	0
Name	P27_IE	P26_IE	P25_IE	P24_IE	P23_IE	P22_IE	P21_IE	P20_IE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	P27_IE	P2.7 INT1 Enable 0: Disable 1: Enable
[6]	P26_IE	P2.6 INT1 Enable 0: Disable 1: Enable
[5]	P25_IE	P2.5 INT1 Enable 0: Disable 1: Enable
[4]	P24_IE	P2.4 INT1 Enable 0: Disable 1: Enable
[3]	P23_IE	P2.3 INT1 Enable 0: Disable 1: Enable
[2]	P22_IE	P2.2 INT1 Enable 0: Disable 1: Enable

[1]	P21_IE	P2.1 INT1 Enable 0: Disable 1: Enable
[0]	P20_IE	P2.0 INT1 Enable 0: Disable 1: Enable

7.5.10 P2_IF (0xD4)

Bit	7	6	5	4	3	2	1	0
Name	P27_IF	P26_IF	P25_IF	P24_IF	P23_IF	P22_IF	P21_IF	P20_IF
Type	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	P27_IF	P2.7 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect
[6]	P26_IF	P2.6 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect
[5]	P25_IF	P2.5 INT1 Interrupt Flag 0: No Interrupt Pending 1: Interrupt Pending
[4]	P24_IF	P2.4 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect
[3]	P23_IF	P2.3 INT1 Interrupt Flag Read: 0: No Interrupt Pending

		1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect
[2]	P22_IF	P2.2 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect
[1]	P21_IF	P2.1 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect
[0]	P20_IF	P2.0 INT1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to 0 1: No effect

8 I²C

8.1 I²C Introduction

The I²C module provides an industry standard two-wire serial interface and is a simple bi-directional synchronous serial bus for communication between MCU and external I²C devices. The bus consists of two serial lines, SDA (serial data line) and SCL (serial clock line), with open-drain output, which works normally after the pull-up resistor is activated and the I/O pin turns its state to VDD5.

Features:

- Supports standard mode (up to 100kHz), fast mode (up to 400kHz) and fast plus mode (up to 1MHz)
- Supports master mode and slave mode
- Supports 7-bit address mode and general call address mode
- Supports DMA data transfer

Both SDA and SCL lines are high level when the bus is idle, which is the only basis for detecting whether the bus is idle or not. Only one master device and at least one slave device are active on the bus during the transmission. When the bus is occupied, other devices must wait for the bus idle to start an I²C communication. The master starts the bus to transfer data. Clock signal is sent to all devices via SCL and the slave address and read/write mode are sent via SDA. When a device on the bus matches the address, it acts as a slave. The relationships between masters and slaves or data transfer direction on the bus are not constant. The process for the master to send data to the slave is shown in Figure 8-1. The master first addresses the slave device and waits for the slave response. And then, it sends data to the slave. Finally, the master terminates the data transmission. The process for the master to receive data from the slave is shown in Figure 8-2. The master first addresses the slave and waits for the slave response. And then, it receives the data from the slave. Finally, the master terminates data transmission. In this case, the master generates timing clock and stops data transmission.

Figure 8-1 Master Sends Data to Slave

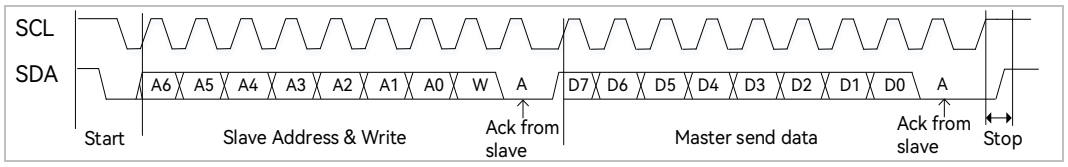
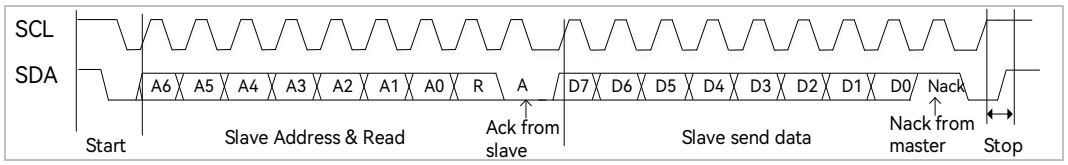


Figure 8-2 Master Receives Data from Slave



8.2 I²C Operations

8.2.1 Master Mode

1. Set I2C_CR[I2CMS] to “1” to select master mode;
2. Configure I2C_CR [I2CSPD] to set the clock rate of SCL;
3. Configure I2C_ID[I2CADD] to set the slave address;
4. Configure I2C_SR[DMOD] to set the read/write direction;
5. Set I2C_CR[I2CEN] to “1” to enable I²C;
6. Set I2C_SR[I2CSTA] to “1” to send START and address. After ACK/NACK is received, I2C_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the master;
7. Sending Data: Write the data to I2C_DR register. The master starts to send data after I2C_SR[STR] is cleared and SCL is released. After the data is transmitted and ACK/NACK is received, I2C_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the master;
8. Receiving Data: The master starts to receive data after I2C_SR[STR] is cleared and SCL is released. After the data is received, I2C_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the master. Configure ACK/NACK via I2C_SR[NACK], and then clear I2C_SR[STR] to release SCL to transmit ACK/NACK signal. After the data is received, I2C_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the master;

9. Stop Communication: Set I2C_SR[I2CSTP] to “1” when I2C_SR[STR] is “1”. The stop signal is sent after I2C_SR[STR] is reset.

8.2.2 Slave Mode

1. Set I2C_CR[I2CMS] to “0” to select slave mode;
2. Configure I2C_ID[I2CADD] to set the slave address or set I2C_ID[GC] to “1” to enable general call mode;
3. Set I2C_CR[I2CEN] to “1” to enable I²C;
4. After START signal and the correct address are received, I2C_SR[I2CSTA] and I2C_SR[STR] are set to “1” by hardware and SCL is pulled LOW by the slave. ACK/NACK is configured via I2C_SR[NACK] and the slave determines whether to receive or send the data via I2C_SR[DMOD];
5. Sending Data: Write the data to I2C_DR register, and clear I2C_SR[STR] to release SCL. The data is sent after ACK/NACK is transmitted. After the data is sent and ACK/NACK is received from the master, I2C_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the slave;
6. Receiving Data: Clear I2C_SR[STR] to release SCL to receive data. After the data is received, I2C_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the slave. ACK/NACK is configured via I2C_SR[NACK] and I2C_SR[STR] is cleared to release SCL for ACK/NACK transmission. If new data is received, I2C_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the slave;
7. RESTART: If the slave is processing a service when receiving START signal, it stops the current routine and waits for receiving address.

8.2.3 I²C Interrupt Sources

The interrupt sources of I²C include:

- I2C_SR[STR] = 1 generates an interrupt. This interrupt source is valid in both master and slave modes.
- I2C_SR[I2CSTP] = 1 generates an interrupt. This interrupt source is only valid in slave mode.

An I²C interrupt request is generated when the interrupt enable bit I2C_CR[I2CIE] is set to “1”.

8.3 I²C Registers

8.3.1 I2C_CR (0x4028)

Bit	7	6	5	4	3	2	1	0
Name	I2CEN	I2CMS	RSV			I2CSPD		I2CIE
Type	R/W	R/W	-	-	-	R/W	R/W	R/W
Reset	0	0	-	-	-	0	0	0

Bit	Name	Description
[7]	I2CEN	I²C Enable The associated GPIOs are enabled to switch to I²C mode, with open-drain output. The pull-up setting decides whether to pull I²C HIGH. 0: Disable 1: Enable
[6]	I2CMS	Master/Slave Mode Selection 0: Slave 1: Master
[5:3]	RSV	Reserved
[2:1]	I2CSPD	I²C Transfer Rate Setting, valid only in Master Mode 00: 100kHz 01: 400kHz 10: 1MHz 11: Reserved
[0]	I2CIE	I²C Interrupt Enable 0: Disable 1: Enable

8.3.2 I2C_ID (0x4029)

Bit	7	6	5	4	3	2	1	0
Name	I2CADD							GC
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	1	0	1	0	1	0

Bit	Name	Description
[7:1]	I2CADD	I²C address
[0]	GC	General call, valid only in Slave Mode 0: General call is disabled. 1: General call is enabled, namely, i.e., the receiving device also reads an ACK at address 0x00.

8.3.3 I2C_DR (0x402A)

Bit	7	6	5	4	3	2	1	0
Name	I2C_DR							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	I2C_DR	I²C Data Register Read: Data to be sent or received Write: Data to be sent

8.3.4 I2C_SR (0x402B)

Bit	7	6	5	4	3	2	1	0
Name	I2CBSY	DMOD	RSV	I2CSTA	I2CSTP	STR	NACK	I2CIF
Type	R	R/W	-	R/W	R/W	R/W0	R/W	R
Reset	0	0	-	0	0	0	0	0

Bit	Name	Description
[7]	I2CBSY	I²C Busy Flag When I2C_CR[I2CEN] = 0, I2C_SR[I2CBSY] is cleared to “0” by hardware. **Master Mode:** After START is transmitted, I2C_SR[I2CBSY] is set to “1” by hardware; after STOP is transmitted, I2C_SR[I2CBSY] is cleared to “0” by hardware. **Slave Mode:** After START is received and address matches, I2C_SR[I2CBSY] is set to “1” by hardware; after STOP is received, I2C_SR[I2CBSY] is cleared to “0” by hardware.
[6]	DMOD	I²C R/W Flag **Master Mode**: 0: Write (master sends the data, and slave receives the data) 1: Read (master receives the data, and slave sends the data) Note 1. This bit can be configured only after I2C_SR[I2CSTA] is set to “1”. 2. A write of “1” to I2C_SR[I2CSTA] changes this bit as well. **Slave Mode**: 0: Write (master sends the data, and slave receives the data) 1: Read (master receives the data, and slave sends the data)
[5]	RSV	Reserved

<table>
<tr>
<td>[4]</td>
<td>I2CSTA</td>
<td>
Master Mode:
When this bit is configured with “1” by the software, START and address bytes are sent after both SCL and SDA are HIGH confirmed by the hardware. This bit is cleared to “0” by hardware automatically when the transmission is completed, and I2C_SR[I2CSTA] writing is forbidden during data transmission. After the data is sent or received, I2C_SR[I2CSTA] is set to “1” to transmit RESTART.
0: Not START and address bytes
1: Transmit START or RESTART and address bytes
Slave Mode:
This bit is set to “1” after the hardware receives START and address matches, and cleared to “0” by software.
Table 8-1 Mapping between I²C Data Type and I2C_SR[I2CSTA] & I2C_SR[I2CSTP] in Slave Mode
<table>
<tr><th>START</th><th>STOP</th><th>I²C Data Type</th></tr>
<tr><td>0</td><td>0</td><td>Data byte</td></tr>
<tr><td>0</td><td>1</td><td>STOP</td></tr>
<tr><td>1</td><td>0</td><td>START + address bytes</td></tr>
<tr><td>1</td><td>1</td><td>STOP received first, then START + address bytes</td></tr>
</table>
Note
When I2C_CR[I2CEN] = 0, I2C_SR[I2CSTA] is automatically cleared to “0”.
</td>
</tr>
<tr>
<td>[3]</td>
<td>I2CSTP</td>
<td>
Master Mode:
This bit cannot be written to “1” by software unless I2C_SR[I2CBSY] = 1; STOP is transmitted after I2C_SR[STR] is cleared to release SCL. After the transmission, this bit is cleared to “0” automatically by hardware. If I2C_SR[I2CSTA] and I2C_SR[I2CSTP] are written to “1” at the same time and I2C_SR[I2CBSY] is “1”, I²C first sends STOP, then START and address bytes. After START and address bytes are transmitted, I2C_SR[STR] is set to “1” by hardware. I2C_SR[I2CSTP] writing is forbidden during data transmission.
0: STOP is not transmitted.
1: STOP is transmitted.
Slave Mode:
This bit is set to “1” by hardware after STOP is received, and cleared to “0” by software.
See Table 8-1 for status flags.
Note
When I2C_CR[I2CEN] = 0, I2C_SR[I2CSTP] is automatically cleared to “0” by hardware.
</td>
</tr>
<tr>
<td>[2]</td>
<td>STR</td>
<td>I²C Bus Pending Flag</td>
</tr>
</table>

		When this bit is set to “1”, SCL is pulled LOW for data transmission on bus. This bit is set to “1” by hardware and cleared to “0” by software. **Master Mode**: 1. After the hardware sends START + address byte and receives ACK/NACK; 2. After the hardware sends STOP and START + address bytes in sequence and receives ACK/NACK; 3. After the hardware sends data and receives ACK/NACK; 4. After the hardware receives the data; **Slave Mode**: 1. After the hardware receives START + address bytes; 2. After the hardware receives the data; 3. After the hardware sends ACK/NACK and data;  Note When I2C_CR[I2CEN] = 0, I2C_SR[I2CSTP] is automatically cleared to “0” by hardware.
[1]	NACK	This bit refers to the feedback from a receiver to a sender after a byte is transferred via I^2C, i.e., the 9^{th} bit of data. In sending mode, this bit is read-only and holds ACK/NACK from receiving device. In receiving mode, this bit can be read or written and is used to send ACK/NACK. Reading this bit obtains the written values. 0: ACK 1: NACK  Note When I2C_CR[I2CEN] = 0, I2C_SR[I2CSTP] is automatically cleared to “0” by hardware.
[0]	I2CIF	I^2C Interrupt Flag After this bit is cleared, the data continues to be transferred via I^2C. It is controlled by the hardware. 0: No Interrupt Pending 1: Interrupt Pending **Master Mode**: When I2C_SR[STR] = 1, this bit is set to “1”, otherwise, it is set to “0”. **Slave Mode**: When I2C_SR[I2CSTP] = 1 or I2C_SR[STR] = 1, this bit is set to “1”, otherwise, it is set to “0”.

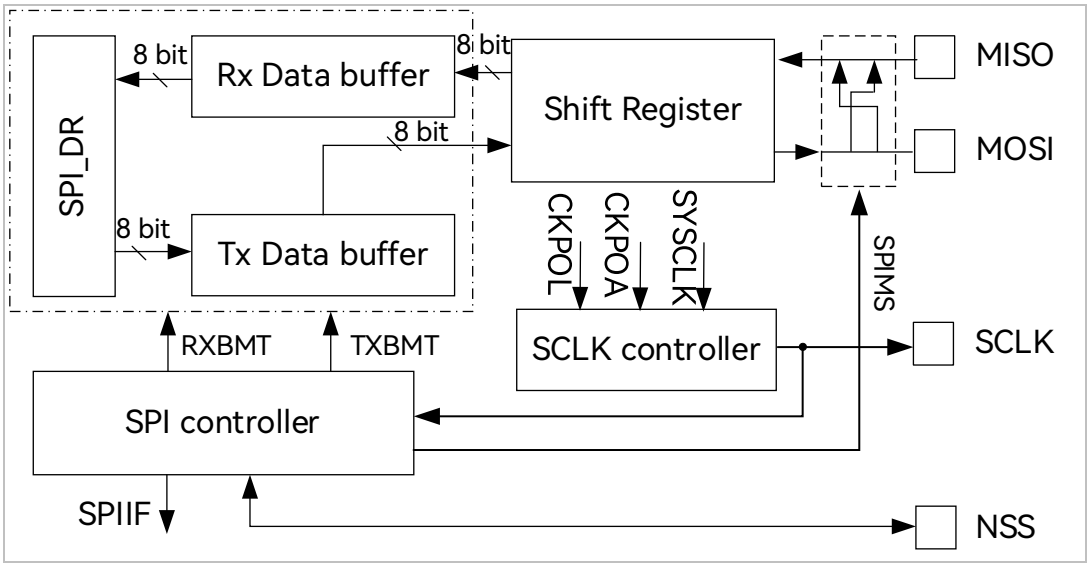
		Note When I2C_CR[I2CEN] = 0, I2C_SR[I2CSTP] is automatically cleared to “0” by hardware.

9 SPI

9.1 SPI Introduction

SPI provides access to a high-speed, full-duplex synchronous serial bus, with its block diagram shown in Figure 9-1. SPI can operate as a master or slave device in 3-wire or 4-wire mode, and supports multiple masters and slaves on a single SPI bus.

Figure 9-1 Block Diagram of SPI Module



9.2 SPI Operations

9.2.1 Signal Descriptions

The four signals for SPI are MOSI, MISO, SCLK and NSS.

9.2.1.1 Master Out, Slave In (MOSI)

The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. Data is transferred with most-significant bit (MSB) first, namely, the master begins its transmission by driving MSB of the shift register on its MOSI pin.

9.2.1.2 Master In, Slave Out (MISO)

The MISO signal is an output from a slave device and an input to the master device. The MISO pin is placed in a high-impedance state when the SPI module is disabled or when the SPI operates in 4-wire mode as a slave that is not selected. When the SPI acts as a slave in 3-wire mode that is selected, MISO is used to serially transfer data from the slave to the master. Data is transferred with most-significant bit (MSB) first, namely, the master begins its transmission by driving MSB of the shift register on its MISO pin.

9.2.1.3 Serial Clock (SCLK)

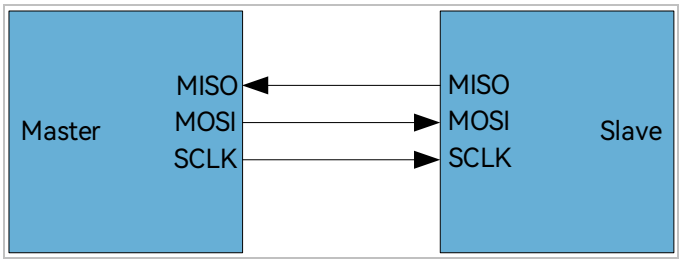
The serial clock (SCLK) signal is an output from the master device and an input to slave devices. It is used to synchronize serial data transmission between the master and slave. SCLK signal is generated by SPI operating as a master.

9.2.1.4 Slave Select (NSS)

The slave-select (NSS) is dependent on the configuration of SPI_CR1[NSSMOD]. SPI may operate in 3-wire Mode or 4-wire Single/multi- Master Mode. When SPI operates in 4-Wire Single Master Mode, the master NSS is configured as chip select output. When SPI operates in 3-wire Mode, NSS is disabled. When SPI operates as a master, multiple addressed slave devices can be selected using general-purpose I/O pins.

When SPI_CR1[NSSMOD] = 00, SPI operates in 3-wire mode. NSS port is not necessary in this mode and there is only one master and one slave on the SPI bus. The connection diagram is shown in Figure 9-2.

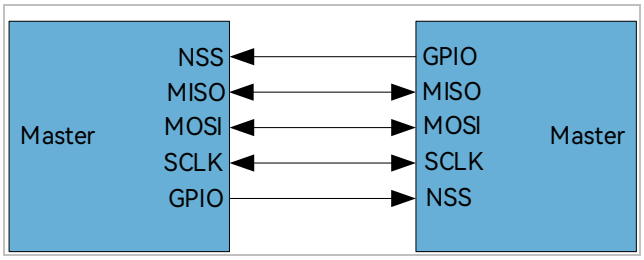
Figure 9-2 SPI Mode



When SPI_CR1[NSSMOD] = 01, SPI operates in 4-wire mode. In this mode, NSS pins on the SPI bus are configured as inputs, waiting to be addressed by the master. When SPI_CR0[SPIMS] = 0, SPI operates in 4-Wire Slave Mode. SPI starts the transfer when the slave NSS is pulled LOW by two system cycles. When SPI_CR0[SPIMS] = 1, SPI operates in Multi-Master Mode. In this mode, when NSS pin of a master on the SPI

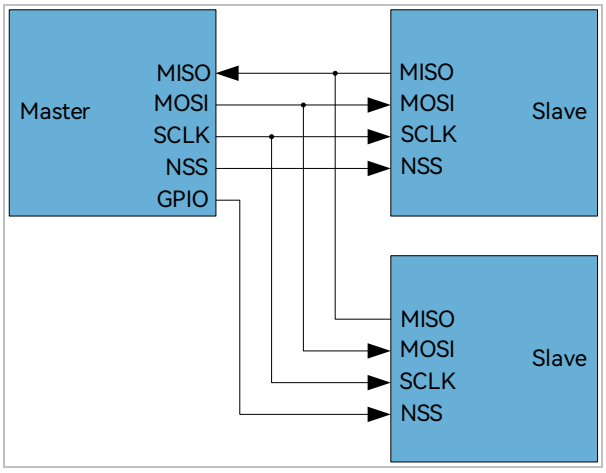
bus is pulled LOW, the Mode Fault Flag SPI_CR1[MODF] is set to “1” and the master works as a slave and SPI is disabled. The connection diagram of Multi-Master Mode is shown in Figure 9-3.

Figure 9-3 Connection Diagram of 4-wire Multi-Master Mode



When SPI_CR1[NSSMOD] = 1X, SPI operates in 4-wire mode. In this mode, NSS pin of the master on the bus is configured as an output, and NSS pin of the slave devices are configured as inputs. SPI_CR1[NSSMOD0] setting decides the output level of NSS pin serving as signal to select a slave. When SPI_CR1[NSSMOD0] = 1, NSS pin outputs a high level. When SPI_CR1[NSSMOD0] = 0, the pin outputs a low level. The connection diagram is shown in Figure 9-4.

Figure 9-4 Connection Diagram of 4-wire Single Master Mode



9.2.2 SPI Master Mode

When SPI_CR0[SPIMS] = 1, SPI operates in master mode, which provides SCLK signal for the bus. When the data is written to SPI_DR, it is firstly written to the transmit buffer and SPI_CR1[TXBMT] is cleared to “0”. If the shift register is empty, then the data in the transmit buffer will be transferred to the shift register for the transmission. The master SPI begins its transmission by driving the MSB of shift register on its MOSI pin. After the transmission is completed, SPI_CR1[SPIIF] and SPI_CR1[TXBMT] are set to “1”. While the SPI master transfers data to a slave on the MOSI line, the addressed SPI slave simultaneously transfers data in

the shift register to the SPI master on the MISO line in a full-duplex operation. Therefore, SPI_CR1[SPIIF] flag serves as both a transmit-complete flag and a receive-data-ready flag, and the data in the shift register is that received by MISO, which is transferred to the receive buffer. The data from SPI_DR is that of the receive buffer. If the data is written to SPI_DR when SPI_CR1[TXBMT] is "0", the write conflict flag bit SPI_CR1[WCOL] will be set to "1" and the data in the transmit buffer keeps unchanged.

9.2.2.1 Master Mode Configurations

1. Configure SPI_CR1[NSSMOD] to set the SPI operating mode;
2. Configure SPI_CR0[CPOL] to set the clock polarity;
3. Configure SPI_CR0[CPHA] to set the clock phase;
4. Set SPI_CR0[SPIMS] to "1" to select master mode;
5. Configure SPI_CLK to set the SCLK rate;
6. Set SPI_CR1[SPIEN] to "1" to enable SPI;
7. Write the data to SPI_DR. SPI transmits data for each write;
8. After SPI_CR1[SPIIF] is set to "1", SPI_DR is read to receive the data.

9.2.3 SPI Slave Mode

When SPI_CR0[SPIMS] = 0, SPI operates in slave mode. In this mode, SCLK signal is sent by the master SPI. The data is shifted in from MOSI pin and shifted out from MISO pin. If no SCLK signal is input, shift register of the slave is in the stop state. If SCLK signal is input, the shift register of slave starts to receive and send data through MOSI and MISO pins. The slave device cannot initiate data transfer. The data sent to the master device is pre-loaded into the shift register by writing to SPI_DR. If the shift register is empty, the data in the transit buffer is transferred into the shift register. After the transmission is completed, SPI_CR1[SPIIF] and SPI_CR1[TXBMT] are set to "1". The received data that is transferred into receive butter and receive buffer empty flag bit SPI_CR0[RXBMT] is cleared, indicating the new data has not been read. If SPI_CR0[RXBMT] is "0" and there is new data ready to be sent to the receive buffer, SPI_CR1[RXOVRN] is set to "1" and the data in the receive buffer remains unaffected. When data is written to SPI_DR,

SPI_CR1[TXBMT] is cleared. If data is written in this case, the write conflict flag bit SPI_CR1[WCOL] is set to “1” and the data in the transmit buffer keeps unchanged.

9.2.3.1 Slave Mode Configurations

1. Configure SPI_CR1[NSSMOD] to set the SPI operating mode;
2. Configure SPI_CR0[CPOL] to set the clock polarity;
3. Configure SPI_CR0[CPHA] to set the clock phase;
4. Set SPI_CR0[SPIMS] to 0 to select slave mode;
5. Set SPI_CR1[SPIEN] to 1 to enable SPI;
6. Write data to SPI_DR and wait for the master to send the clock signal.

9.2.4 SPI Interrupt Sources

After SPI interrupt is enabled (IE[SPIIE] = 1), an interrupt is generated when any of the three following flag bits are set to “1”.

Note

These flag bits can be cleared to “0” by software only.

1. SPI interrupt flag SPI_CR1[SPIIF] is set to “1” each time after the byte is transferred. It applies to all SPI modes.
2. If SPI_DR is written when the data in transmit buffer has not been transferred to the shift register, the write conflict flag SPI_CR1[WCOL] is set to “1” and the write operation will not be implemented. It applies to all SPI modes.
3. The receive overflow flag SPI_CR1[RXOVR] is set to “1” when SPI operates in slave mode and a transmission is completed while the receive buffer still holds unread data from a previous transfer. And the received data will not be transferred to the receive buffer.

9.2.5 Serial Clock Timing

Four combinations of serial clock phase and idle polarity can be selected using the CPHA and CPOL bits in the SPI_CR0 Register. SPI_CR0[CPHA] selects the clock phase (the edge of the SCLK signal used to latch

the data in shift register). SPI_CR0[CPOL] selects the polarity. Both master and slave devices must be configured with the same clock phase and polarity. When the clock phase and polarity is configured, SPI shall be disabled (SPI_CR1[SPIEN] = 0). The timing relationship between SCL and SDA in master mode is shown in Figure 9-5, and that in slave mode is shown in Figure 9-6 and Figure 9-7.

Figure 9-5 SDA/SCL Line Timing Diagram in Master Mode

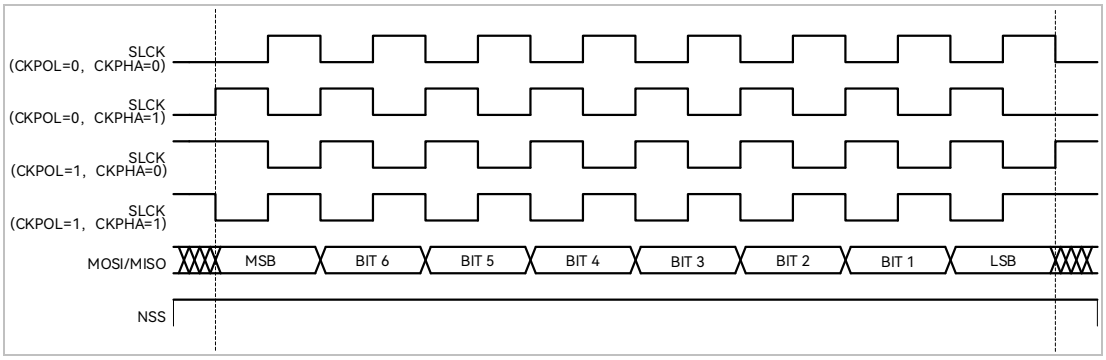


Figure 9-6 SDA/SCL Line Timing Diagram in Slave Mode (SPI_CR0[CPHA] = 0)

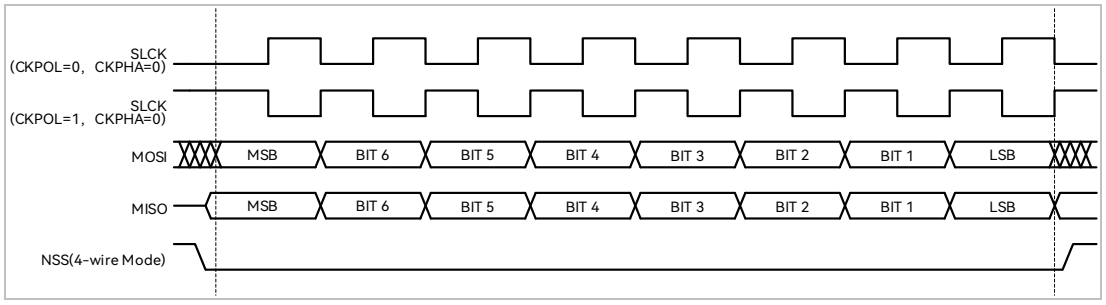
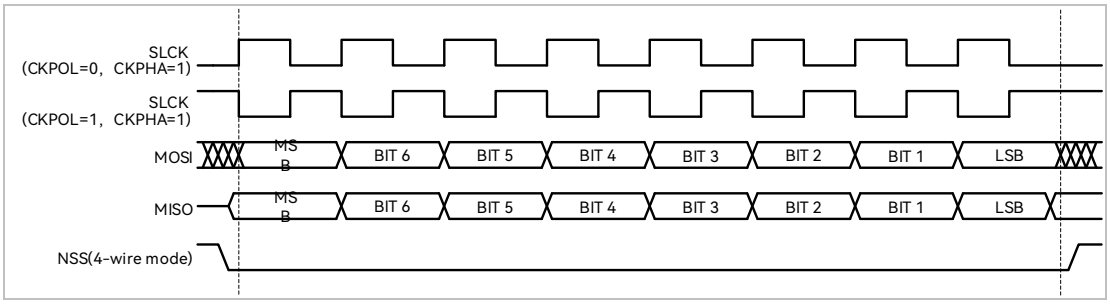


Figure 9-7 SDA/SCL Line Timing Diagram in Slave Mode (SPI_CR0[CPHA] = 1)



9.3 SPI Registers

9.3.1 SPI_CR0 (0x4030)

Bit	7	6	5	4	3	2	1	0
Name	SPIBSY	SPIMS	CPHA	CPOL	SLVSEL	NSSIN	SRMT	RXBMT
Type	R	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	1	0	1	1

Bit	Name	Description
[7]	SPIBSY	Busy Flag Bit 0: SPI transferring is disabled 1: SPI transferring is enabled
[6]	SPIMS	Master/Slave Mode Selection 0: Slave 1: Master
[5]	CPHA	SPI Clock Phase 0: Data is collected at the first edge of SCLK 1: Data is collected at the second edge of SCLK
[4]	CPOL	SPI Clock Polarity in Idle State 0: Low level 1: High level
[3]	SLVSEL	This bit is set to “1” when the NSS pin voltage is low, indicating that the device is selected as slave. It is cleared to “0” when the NSS pin voltage is high, indicating that the device is not selected as slave. This bit does not indicate instant value of the NSS pin, but the de-noising signal input by the pin.
[2]	NSSIN	NSS real-time signal, unfiltered
[1]	SRMT	Shift Register Empty Flag (valid only in Slave Mode) This bit is set to “0” after data has been shifted out of the Transit Buffer into the shift register or SCLK changes, and is set to “1” when there is no data in the shift register or transmit and receive buffer.  Note SPI_CR0[SRMT] = 1 in Master Mode
[0]	RXBMT	Receive Buffer Empty Flag (valid only in Slave Mode) This bit is set to “0” when the data in the receive buffer has not been read, and is set to “1” when the data has been read and there is no new data in the receive buffer.  Note

		SPI_CR0[RXBMT] = 1 in Master Mode

Note

Clock phase and idle polarity modes SPI_CR0[CPHA:CPOL]:

- 00: Receive data on rising edge, and send on falling edge. Idle level is low.
- 01: Send data on rising edge, and receive data on falling edge. Idle level is high.
- 10: Send data on rising edge, and receive data on falling edge. Idle level is low.
- 11: Receive data on rising edge, and send data on falling edge. Idle level is high.

9.3.2 SPI_CR1 (0x4031)

Bit	7	6	5	4	3	2	1	0
Name	SPIIF	WCOL	MODF	RXOVR	NSSMOD		TXBMT	SPIEN
Type	R/W0	R/W0	R/W0	R/W0	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	1	0

Bit	Name	Description
[7]	SPIIF	SPI Interrupt Flag This bit is set to “1” by hardware each time after a data frame (8-bit) is transferred. Read: 0: This bit is cleared to “0” 1: No effect Write: 0: This bit is cleared to “0” 1: No effect
[6]	WCOL	Write Conflict Interrupt Flag When SPI_CR1[TXBMT] is “0”, a write to SPI_DR sets this bit to “1”. This bit can be cleared to “0” by software only. Read: 0: This bit is cleared to “0” 1: No effect Write: 0: This bit is cleared to “0” 1: No effect
[5]	MODF	Master Mode Fault Interrupt Flag This bit is set to “1” when a master mode conflict is detected (SPI_CR0[NSSIN] = 0, SPI_CR1[SPIMS] = 1 and SPI_CR1[NSSMOD] = 01). This bit can be cleared to “0” by software only. Read: 0: This bit is cleared to “0” 1: No effect Write:

		0: This bit is cleared to “0” 1: No effect
[4]	RXOVR	Receive Overflow Interrupt Flag (Slave Mode only) This bit is set to “1” by hardware (and generates a SPI interrupt) when the Receive Buffer still holds unread data from a previous transfer and the last bit of the current transfer has been shifted into the SPI shift register. This bit cannot be clear to “0” automatically by hardware, and can be cleared by software only. Read: 0: This bit is cleared to “0” 1: No effect Write: 0: This bit is cleared to “0” 1: No effect
[3:2]	NSSMOD	SPI Mode Selection 00: 3-wire Slave or 3-wire Master Mode. NSS signal is not routed to a port pin. 01: 4-wire Slave Mode. NSS pin is configured as an input. 1X: 4-wire Single-Master Mode. NSS pin is configured as an output and outputs SPI_CR1[2] value.
[1]	TXBMT	Transmit Buffer Empty Flag This bit is cleared to “0” when new data is written to the Transit Buffer. It is set to “1” when the data in the Transit Buffer is transferred to the SPI shift register, indicating that it is safe to write data to the transmit buffer. 0: Data is written to the transmit buffer. 1: Data in the transmit buffer has been transferred to the shift register.
[0]	SPIEN	SPI Enable 0: Disable 1: Enable

9.3.3 SPI_CLK (0x4032)

Bit	7	6	5	4	3	2	1	0
Name	SPI_CLK							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	SPI_CLK	SPI Baud Rate Setting This bit is valid in master mode, and can be written only when SPI_CR1[SPIEN] = 0. Baud rate = SYSCLK/2/(SPI_CLK + 1) Example: If baud rate = 2400kHz, then SPI_CLK = (24M/2/2400k) - 1 = 4, i.e. 0x04. SPI Master Device Sending Maximum Baud Rate: 12M

		SPI Master Device Receving Maximum Baud Rate: 4M SPI Slave Device Sending Maximum Baud Rate: 2.4M SPI Slave Device Receving Maximum Baud Ratee: 2.4M Note When PI and slave SPI are active at the same time (using DMA transfer), the master SPI Baud Rate shall be less than 600kHz to prevent erroneous data transmitted from the slave SPI

9.3.4 SPI_DR (0x4033)

Bit	7	6	5	4	3	2	1	0
Name	SPI_DR							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	SPI_DR	SPI Data Register SPI_DR Register is used to transmit and receive SPI data. In master mode, when the date is written to SPI_DR, it's transferred to Transit Buffer for the transmission. When SPI_DR is read, the data held in Receive Buffer is obtained.

10 UART

10.1 UART Introduction

UART is a full-duplex or half-duplex serial data exchange interface as shown in Figure 10-1. The baud rate is configurable and supports DMA transmission. Figure 10-2 depicts the UART timing.

Figure 10-1 Block Diagram of UART Module

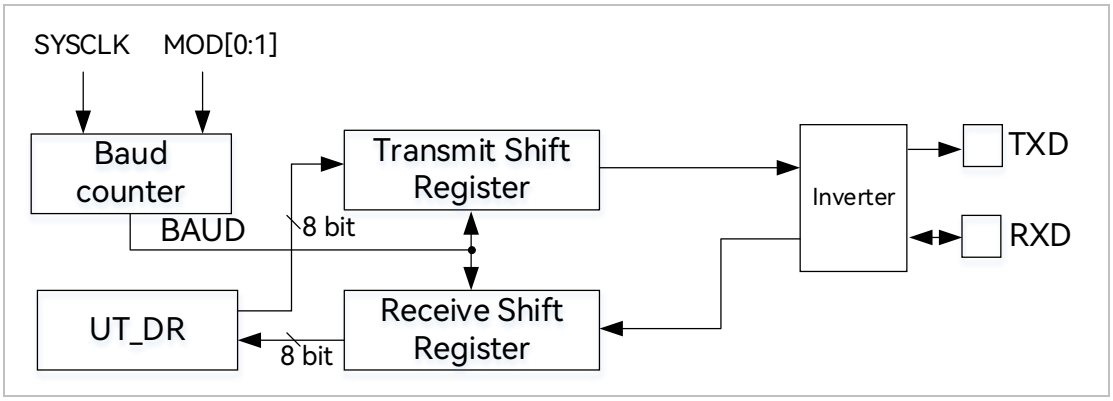
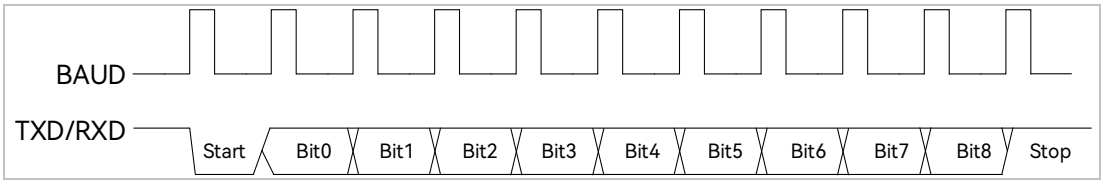


Figure 10-2 UART Timing Diagram



10.2 UART Operations

The corresponding registers shall be enabled before using UART feature. See 24.3.14 PH_SEL (0x404C) (bits [6] and [5]) for more details.

10.2.1 UART Mode0

UART mode0, or shifting mode, is mainly used to expand the IO ports. In this mode, TXD pin is configured as clock output, and RXD as data bus. The clock frequency is set at SYSCLK/12, and the data is sent starting from the least significant bit. UT_CR[REN] decides the data is received or sent. When UT_CR[REN] = 0, the data is sent, and when UT_CR[REN] = 1, the data is received.

Sending Data: Write the data to UT_DR and reset UT_CR[TI]. TXD pin outputs shift pulse, and RXD pin sends

the data held by UT_DR. The output clock frequency is SYSCLK/12. UT_CR[TI] is set to “1” after the transmission is completed.

Receiving Data: Set UT_CR[REN] to “1” to receive the data and clear UT_CR[RI]. TXD pin outputs shift pulse, and RXD pin receives the data. The shift pulse frequency is SYSCLK/12. After the data is received, UT_CR[RI] is set to “1” and UT_DR is read to obtain the data.

10.2.2 UART Mode1

UART mode1 works in full/half duplex mode. TXD pin is configured as an output (Transmit Data Bus), and RXD pin as an input (Receive Data Bus). It uses a total of 10 bits, or 1 start bit, 8 data bits (UT_DR) and 1 stop bit, to receive or transmit data. The baud rate is configured by UT_BAUD[BAUD].

Sending Data: Write the data to UT_DR and clear UT_CR[TI]. TXD outputs 10-bit data. UT_CR[TI] is set to "1" after the transmission is completed.

Receiving Data: Set UT_CR[REN] to "1" to receive the data and clear UT_CR[RI]. The data is received via RXD. After the data is received, UT_CR[RB8] and UT_CR[RI] are set to "1" and UT_DR is read to obtain the data.

10.2.3 UART Mode2

UART mode2 works in full/half duplex mode. TXD pin is configured as an output (Transmit Data Bus), and RXD pin as an input (Receive Data Bus). It uses a total of 11 bits, namely 1 start bit, 9 data bits (UT_DR + UT_CR[RB8] / UT_CR[TB8]) and 1 stop bit, to receive or transmit data. The baud rate is determined by SYSCLK / (32-16*UT_BAUD[BAUD_SEL]).

Sending Data: Write the data to UT_DR, set UT_CR[TB8] and reset UT_CR[TI]. TXD outputs 11-bit data. UT_CR[TI] is set to “1” after the transmission is completed.

Receiving Data: Set UT_CR[REN] to “1” to receive the data and clear UT_CR[RI]. The data is received via RXD. After the data is received, UT_CR[RI] is set to “1”. UT_CR[RB8] stores the 9th bit of the data, and UT_DR stores the first 8 bits.

10.2.4 UART Mode3

The operations are the same as those for UART mode2, but baud rate settings are the same as those for

UART mode1.

10.2.5 UART Interrupt Sources

After UART interrupt is enabled (IE[ES0] = 1), an interrupt is generated when any of the two following flag bits are set to “1”.

Note

These flag bits can be cleared to “0” by software only.

- After the data (8-bit data for UART mode0 and mode1 and 9-bit data for UART mode2 and mode3) is transmitted via UART, UT_CR[TI] is set to “1” by hardware.
- After the data and STOP are received via UART, UT_CR[RI] is set to “1” by hardware.

10.3 UART Registers

10.3.1 UT_CR (0x98)

Bit	7	6	5	4	3	2	1	0
Name	MOD		SM2	REN	TB8	RB8	TI	RI
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:6]	MOD	Mode Selection 00: UART Mode0--Shift Register Baud rate = SYSCLK/12 01: UART Mode1--8-bit UART Baud rate: SYSCLK / (16 /(1 + UT_BAUD[BAUD])) / (UT_BAUD[BAUD_SEL] + 1) 10: UART Mode2--9-bit UART Baud rate: SYSCLK/(32 – 16*UT_BAUD[BAUD_SEL]) 11: UART Mode3--9-bit UART Baud rate: SYSCLK / (16 / (1 + UT_BAUD[BAUD])) / (UT_BAUD[BAUD_SEL] + 1)
[5]	SM2	Communication Mode Selection 0: Single-device Communication 1: Multi-device Communication
[4]	REN	UART Receive Enable 0: Disable 1: Enable. This bit can be cleared to “0” by software only.
[3]	TB8	Bit9 of the sent data in UART Mode2 and UART Mode3. This bit can be cleared by hardware as required.

[2]	RB8	Bit9 of the received data in UART Mode2 and UART Mode3. If the bit SM2 is set as “0”, it serves as the STOP bit. It does not work in UART Mode0.
[1]	TI	Data Sending Completed Interrupt Flag. This bit is set to “1” after the data is sent, and can be cleared to “0” by software only.
[0]	RI	Data Receiving Completed Interrupt Flag. This bit is set to “1” after the data is received, and can be cleared to “0” by software only.

10.3.2 UT_DR (0x99)

Bit	7	6	5	4	3	2	1	0
Name	UT_DR							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	UT_DR	Transmit/Receive Data

10.3.3 UT_BAUD (0x9A, 0x9B)

UT_BAUDH (0x9B)								
Bit	15	14	13	12	11	10	9	8
Name	BAUD_SEL	RSV			BAUDH[11:8]			
Type	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset	0	-	-	-	0	0	0	0
UT_BAUDL(0x9A)								
Bit	7	6	5	4	3	2	1	0
Name	BAUDL[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	1	1	0	1	1

Bit	Name	Description
[15]	BAUD_SEL	Frequency Multiplier Enable 0: Disable 1: Enable
[14:12]	RSV	Reserved
[11:0]	BAUD	Baud rate setting in UART Mode1 and UART Mode3

11 MDU

11.1 MDU Introduction

Multiply and Division Unit (MDU) is a built-in multiply and division co-processor for 16bit×16bit multiplication and 32bit/16bit division. It supports both unsigned and signed multiplication and unsigned division. MDU mode is determined by register MDU_CR.

Multiply Mode: MD_MC3 ~ 0 = {MD_MAH、MD_MAL} * {MD_MBH、MD_MBL}

Note

Since MD_MC3 ~ 2 multiplexes MD_MAH and MD_MAL, and MD_MC1 ~ 0 multiplexes MD_MBH and MD_MBL, multiplicand and multiplier are written to MD_MAH and MD_MAL, and MD_MBH and MD_MBL respectively, and the result is accessed by reading the register.

Division Mode: MD_DC3 ~ 0, MD_DD1 ~ 0 = MD_DA3 ~ 0 / MD_DB1 ~ 0

The quotient is saved in MD_DC3 ~ 0 and the remainder is saved in MD_DD1 ~ 0.

Note

Since MD_DC3 ~ 0 multiplexes MD_DA3 ~ 0 and MD_DD1 ~ 0 multiplexes MD_DB1 ~ 0, dividend and divisor are written to MD_DA3 ~ 0 and MD_DB1 ~ 0 respectively, and the quotient and the remainder are accessed by reading the corresponding registers.

One multiplication process takes about one clock cycle, and the result can be shifted to the right according to MDU_CR[ALIGN]. One division process takes about 16 clock cycles. MDU_CR[DIVSTA] shall be configured to start the division. The software determines whether the division is completed by MDU_CR[DIVDONE].

11.2 Multiplication Configurations

8. Set MDU_CR[MDSN] according to the multiplication type. It is set to 0 for unsigned multiplication, and 1 for signed multiplication. The right-shift bit of the result is set by MDU_CR[ALIGN];
9. Write multiplicand to MD_MA, and multiplier to MD_MB;
10. Read MD_MA to obtain 16 high-order bits of the product, and MD_MB to obtain 16 low-order bits of the

product

11. Start from step 2 if multiplication type and right-shift bit are the same.

11.3 Division Configurations

12. Write dividend to MD_DA, and divisor to MD_DB;
13. Write “1” to MDU_CR[DIVSTA] to start 32-bit/16-bit division;
14. The division is completed after about 16 clock cycles. MDU_CR[DIVDONE] = 1 means the division process has been completed, otherwise, you have to wait for the result;
15. Read MD_DA to obtain the quotient, and MD_DB to obtain the remainder.

11.4 Important Matters

- If “0” is written to MD_DB as the divisor, MDU produces MDU_CR[DIVERR] flag bit and keeps it stays at “1” until a non-zero divisor is written;
- The quotient and the remainder are uncertain or incorrect when the divider of MDU module is working (MDU_CR[DIVDONE] = 0). They are stable and correct only when division process is completed, that is the divider is idle.
- When the divider of MDU module is working (MDU_CR[DIVDONE] = 0), changing the value of divisor or division will not affect the final result, unless MD_CR[DIVSTA] is configured to “1” again to restart a new division process.
- Because data input register of the multiplier or divider in MDU module is only one level deep, interrupts can change the result. For example, an interrupt is generated after the multiplicand is written to MD_MA but before the multiplier is written to MD_MB. The interrupt requires the multiplier in the service routine. In this case, after the interrupt is implemented, MD_MA is changed and the multiplication result is wrong. Therefore, software developers shall take proper measures to avoid such situation.

11.5 MDU Registers

11.5.1 MDU_CR (0xC1)

Bit	7	6	5	4	3	2	1	0
Name	DIVDONE	DIVERR	RSV		ALIGN		MDSN	DIVSTA
Type	R	R	-	-	R/W	R/W	R/W	R/W
Reset	1	0	-	-	0	0	0	0

Bit	Name	Description
[7]	DIVDONE	0: The division is in progress. 1: The division is completed.
[6]	DIVERR	0: Last division is correct (a non-zero divisor is written). 1: Last division is wrong (“0” is written as the divisor).
[5:4]	RSV	Reserved
[3:2]	ALIGN	Right-shift Bit for the Result of Multiplication 00: Right shift is not supported. 01: The result is right shifted by 8 bits. 10: The result is right shifted by 12 bits. 11: The result is right shifted by 15 bits.
[1]	MDSN	Multiplication Type Selection 0: Unsigned Multiplication 1: Signed Multiplication
[0]	DIVSTA	Division Start Bit This bit is valid only for division and is set to “1” by software during division. It is automatically cleared to “0” by hardware after the division is completed. 0: The divider does not start. 1: 32-bit division starts.

11.5.2 MD_MBL (0xCA)

Bit	7	6	5	4	3	2	1	0
Name	MD_MBL							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	MD_MBL	Multiplier bit [7:0] (write only) or product bit [7:0] (read only)

11.5.3 MD_MBH (0xCB)

Bit	7	6	5	4	3	2	1	0
Name	MD_MBH							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	MD_MBH	Multiplier bit [15: 8] (write only) or product bit [15: 8] (read only)

11.5.4 MD_MAL (0xC2)

Bit	7	6	5	4	3	2	1	0
Name	MD_MAL							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	MD_MAL	Multiplicand bit [7:0] (write only) or product bit [23:16] (read only)

11.5.5 MD_MAH (0xC3)

Bit	7	6	5	4	3	2	1	0
Name	MD_MAH							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	MD_MAH	Multiplicand bit [15:8] (write only) or product bit [31:24] (read only)

11.5.6 MD_DA0 (0xC4)

Bit	7	6	5	4	3	2	1	0
Name	MD_DA0							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	MD_DA0	Dividend bit [7:0] (write only) or quotient bit [7:0] (read only)

11.5.7 MD_DA1 (0xC5)

Bit	7	6	5	4	3	2	1	0
Name	MD_DA1							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	MD_DA1	Dividend bit [15:8] (write only) or quotient bit [15:8] (read only)

11.5.8 MD_DA2 (0xC6)

Bit	7	6	5	4	3	2	1	0
Name	MD_DA2							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	MD_DA2	Dividend bit [23:16] (write only) or quotient bit [23:16] (read only)

11.5.9 MD_DA3 (0xC7)

Bit	7	6	5	4	3	2	1	0
Name	MD_DA3							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	MD_DA3	Dividend bit [31:24] (write only) or quotient bit [31:24] (read only)

11.5.10 MD_DB0 (0xCC)

Bit	7	6	5	4	3	2	1	0
Name	MD_DB0							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	MD_DB0	Divisor bit [7:0] (write only) or remainder bit [7:0] (read only)

11.5.11 MD_DB1 (0xCD)

Bit	7	6	5	4	3	2	1	0
Name	MD_DB1							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	MD_DB1	Divisor bit [15:8] (write only) or remainder bit [15:8] (read only)

12 PI

12.1 PI Introduction

PI controller is a linear controller, where the output is generated by linear combination of error proportional, integral and differential actions, and then implemented by an actuator. In motor control system, it is used to for speed and position control.

PI algorithm:

$$U_k = U_{k-1} + Kp \times (E_k - E_{k-1}) + Ki \times E_k$$

Where,

U_k: Output for round k of calculation

U_{k-1}: Output for round k-1 of calculation

E_k: Deviation for round k of input

E_{k-1} and E_{k-2}: Deviations for round k-1 and round k-2 of calculation

K_p, and K_i: Proportional (P) and integral (I) coefficients of the controller

The maximum U_k is represented as PIx_UKMAX (x=0 ~ 3) and the minimum value as PIx_UKMIN

12.2 PI Operations

1. Configure PI_LPF_CR[PISTA] = 1 to enable PI. After four clock cycles, the calculation is completed and PI_UK is updated.
2. Q12 (default) or Q15 can be selected for PI parameters. It means data format of PI_KP and PI_KI is Q12 and that of other registers are Q15.
3. U_{k-1} and E_{k-1} default to the previous U_k and E_k. You can write the data to PI_EK register and start PI to change E_{k-1}, or write the data to PI_UK register to change U_{k-1}.

When PI controller is invoked repeatedly, relevant parameters shall be saved after each PI operation, and

initialized before the next PI operation. Initialization codes are shown as below:

```
PI_EK = X;                      //Initialize E_{k-1}
SetBit(PI_LPF_CR , PISTA);      //Start PI
_nop_();
_nop_();
_nop_();
_nop_();                        //Wait for PI controller to complete operations
PI_UK = X;                      //Initialize U_{k-1}
```

12.3 PI Registers

12.3.1 PI_LPF_CR (0xF9)

Bit	7	6	5	4	3	2	1	0
Name	T2SS	RSV				PIRANGE	PISTA	LPFSTA
Type	R/W	-	-	-	-	R/W	R/W	R/W
Reset	0	-	-	-	-	0	0	0

Bit	Name	Description
[7]	T2SS	Input Mode Selection of Timer2 Step Motor 0: P1.0 for direction input, and P0.7 for pulse input 1: P1.0 for backward pulse input, and P0.7 for forward pulse input
[6:3]	RSV	Reserved
[2]	PIRANGE	Data Format of PI Parameters 0: Q12. The value range of *KP* and *KI* [-32768,32767] corresponds to range [-8,8]. 1: Q15. The value range of *KP* and *KI* [-32768,32767] corresponds to range [-1,1].
[1]	PISTA	PI controller Enable It is set to “1” by software, and can be automatically cleared to “0” by hardware. 0: Disable 1: Enable
[0]	LPFSTA	LPF Enable It is set to “1” by software, and can be automatically cleared to “0” by hardware. 0: Disable 1: Enable

12.3.2 PI_EK (0xEA, 0xEB)

PI_EKH(0xEB)								
Bit	15	14	13	12	11	10	9	8
Name	PI_EK[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI_EKL(0xEA)								
Bit	7	6	5	4	3	2	1	0
Name	PI_EK[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI_EK	Input Deviation Range [-32768,32767]

12.3.3 PI_UK (0xEC, 0xED)

PI_UKH(0xED)								
Bit	15	14	13	12	11	10	9	8
Name	PI_UK[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI_UKL(0xEC)								
Bit	7	6	5	4	3	2	1	0
Name	PI_UK[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI_UK	Calculation Result of PI Controller Range [-32768,32767]

12.3.4 PI_KP (0xEE, 0xEF)

PI_ KPH(0xEF)								
Bit	15	14	13	12	11	10	9	8
Name	PI_KP[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI_ KPL(0xEE)								
Bit	7	6	5	4	3	2	1	0

Name	PI_KP[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI_KP	KP Coefficient Range [-32768,32767]

12.3.5 PI_KI (0XF2, 0xF3)

PI_KIH(0xF3)								
Bit	15	14	13	12	11	10	9	8
Name	PI_KI[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI_KIL(0xF2)								
Bit	7	6	5	4	3	2	1	0
Name	PI_KI[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI_KI	KI Coefficient Range [-32768,32767]

12.3.6 PI_UKMAX (0xF4, 0xF5)

PI_UKMAXH(0xF5)								
Bit	15	14	13	12	11	10	9	8
Name	PI_UKMAX[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI_UKMAXL[7:0]								
Bit	7	6	5	4	3	2	1	0
Name	PI_UKMAX[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI_UKMAX	UK Maximum Value Range [-32768,32767]

12.3.7 PI_UKMIN (0xF6, 0xF7)

PI_UKMINH(0xF7)								
Bit	15	14	13	12	11	10	9	8
Name	PI_UKMIN[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI_UKMINL(0xF6)								
Bit	7	6	5	4	3	2	1	0
Name	PI_UKMIN[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI_UKMIN	UK Minimum Value Range [-32768,32767]

13 LPF

13.1 LPF Introduction

A low-pass filter (LPF) is an electronic circuit that allows low-frequency signals to pass through while attenuating high-frequency signals.

LPF algorithm:

$$Y_k = Y_{k-1} + K \times (X_k - Y_{k-1})$$

Where,

Y_k: Filtered data

Y_{k-1}: Previous filtered output

K: Filter coefficient

Xk: Data to be filtered

13.2 LPF Operations

1. Configure PI_LPF_CR[LPFSTA] = 1 to enable LPF for the descriptions on the register PI_LPF_CR). After four clock cycles, the calculation is completed and LPF_Y is updated.
2. Y_{k-1} default to the previous Y_k. You can write the data to LPF_Y register to change Y_{k-1}.

13.3 LPF Registers

13.3.1 PI_LPF_CR (0xF9)

Bit	7	6	5	4	3	2	1	0
Name	T2SS	RSV				PIRANGE	PISTA	LPFSTA
Type	R/W	-	-	-	-	R/W	-	-
Reset	0	-	-	-	-	0	-	-

Bit	Name	Description
[7:1		See 12.3.1 PI_LPF_CR (0xF9)
[0]	LPFSTA	LPF Startup (Software written to “1” and then hardware is cleared to “0”

		automatically) 0: Disable 1: Enable

13.3.2 LPF_K (0xDD)

Bit	7	6	5	4	3	2	1	0
Name	LPF_K							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	LPF_K	LPF Coefficient The value range [-128,127] corresponds to range [-1,1]

13.3.3 LPF_X (0xDE, 0xDF)

LPF_XH(0xDF)								
Bit	15	14	13	12	11	10	9	8
Name	LPF_X[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF_XL(0xDE)								
Bit	7	6	5	4	3	2	1	0
Name	LPF_X[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	LPF_X	Input Value Range [-32768,32767]

13.3.4 LPF_Y (0xE6, 0xE7)

LPF_YH(0xE7)								
Bit	15	14	13	12	11	10	9	8
Name	LPF_Y[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF_YL(0xE6)								
Bit	7	6	5	4	3	2	1	0
Name	LPF_Y[7:0]							

Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	LPF_Y	Output Value Range [-32768,32767]

14 SMDU

SMDU is a built-in computing co-processor that assists the CPU in processing complex operations efficiently. It supports multiplication, division, trigonometric operation, LPF operation and PI operation. SMDU module can be invoked in different interrupt services and master programs, and the results are independent from each other.

14.1 SMDU Features

The SMDU module has the following features:

- Support invocation with nested interrupt
- Hardware acceleration to reduce CPU load
- Support the following modes:
  - 16-bit signed multiplication
  - 16-bit signed multiplication (result shifted left by one-bit)
  - 16-bit unsigned multiplication
  - 32-bit/16-bit unsigned division
  - SMDU LPF
  - Coordinate transformation (SIN/COS)
  - Arctangent (ATAN)
  - PI

14.2 SMDU Instructions

14.2.1 SMDU Operations

SMDU is operated as follows.

1. Set TIM234_CTRL[MDU_EN_N] to “1” to enable SMDU module. After that, MDU, LPF and PI modules are disabled;
2. Select an operation mode by MDU_CR[MDUMOD];

3. Write the data to the associated computing units, select computing unit of the SMDU module by MDU_CR[MDUSTA], and start SMDU computing;

4. Wait for MDU_CR[MDUBUSY] to be cleared to “0” by hardware.

Note

When using SMDU, ensure that the computing mode and other data have been written before configuring MDU_CR[MDUSTA].

14.2.2 16-bit Signed Multiplication with the Result Shifted Left by One-bit

When MDU_CR[MDUMOD] = 000, SMDU module works in the 16-bit signed multiplication mode with the result shifted left by one-bit. As shown in Table 14-1, after 16-bit signed data is written to MULx_MA and MULx_MB as multiplicand and multiplier respectively, 32-bit signed data is obtained by the product shifting left by one bit. The result is accessed by reading MULx_MC register.

Table 14-1 Register Definitions in 16-bit Signed Multiplication Mode with Result Shifted Left by One-bit

Data Register	Input	Output
MULx_MA	Multiplicand	-
MULx_MB	Multiplier	-
MULx_MC	-	Product

14.2.3 16-bit Signed Multiplication

When MDU_CR[MDUMOD] = 001, SMDU module works in the 16-bit signed multiplication mode. As shown in Table 14-2, 32-bit signed data is obtained after 16-bit signed data is written to MULx_MA and MULx_MB as multiplicand and multiplier respectively. The result is accessed by reading MULx_MC register.

Table 14-2 Register Definitions in 16-bit Signed Multiplication Mode

Data Register	Input	Output
MULx_MA	Multiplicand	-
MULx_MB	Multiplier	-
MULx_MC	-	Product

14.2.4 16-bit Unsigned Multiplication

When MDU_CR[MDUMOD] = 010, SMDU module works in the 16-bit unsigned multiplication mode. As shown in Table 14-3, 32-bit unsigned data is obtained after 16-bit unsigned data is written to MULx_MA

and MULx_MB as multiplicand and multiplier respectively. The result is accessed by reading MULx_MC register.

Table 14-3 Register Definitions in 16-bit Unsigned Multiplication Mode

Data Register	Input	Output
MULx_MA	Multiplicand	-
MULx_MB	Multiplier	-
MULx_MC	-	Product

14.2.5 32-bit/16-bit Unsigned Division

When MDU_CR[MDUMOD] = 011, SMDU module works in the 32-bit/16-bit unsigned division mode. As shown in Table 14-4, 32-bit unsigned quotient and 16-bit unsigned remainder are obtained after 32-bit dividend and a 16-bit divisor are written to DIVx_DA and DIVx_DB registers respectively. The quotient and remainder are accessed by reading DIVx_DQ and DIVx_DR registers respectively.

Table 14-4 Register Definitions in the Unsigned Division Mode

Data Register	Input	Output
DIVx_DA	Dividend	-
DIVx_DB	Divisor	-
DIVx_DQ	-	Quotient
DIVx_DR	-	Remainder

14.2.6 SMDU LPF

SMDU LPF is enabled when MDU_CR[MDUMOD] = 110.

SMDU LPF has the same function as LPF. But read-write data of SMDU LPF is stored in XSFR, while that of LPF in SFR.

As shown in Table 14-5, K are 16-bit signed data. Y_k is obtained after Y_{k-1} is written to LPFx_Y, K to LPFx_K and X_k to LPFx_X, and is accessed by reading LPFx_Y.

Table 14-5 Register Definitions in LPF Mode

Data Register	Input	Output
LPFx_X	X_k	-
LPFx_K	K	-
LPFx_Y	Y_{k-1}	Y_k

14.2.7 Coordinate Transformation (SIN/COS)

When MDU_CR[MDUMOD] = 100, SMDU module works in Coordinate Transformation mode. As shown in Figure 14-1, the coordinate transformation converts the components cos_i and sin_i of vector A under the x-y axis to the components cos_o and sin_o under the x'-y' axis, with the x'-y' axis lagging the x-y axis by θ.

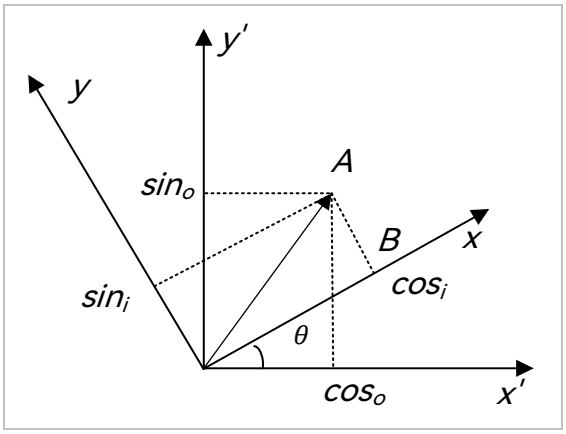
The formula for coordinate transformation is:

$$cos_o = cos_i \times cos\,\theta - sin_i \times sin\,\theta$$
$$sin_o = cos_i \times sin\,\theta + sin_i \times cos\,\theta$$

In particular, when sin_i = 0, the coordinate transformation is a sine and cosine calculation with cos_i as the amplitude, calculated as:

$$cos_o = cos_i \times cos\,\theta$$
$$sin_o = cos_i \times sin\,\theta$$

Figure 14-1 Coordinate Transformation



As shown in Table 14-6, cos_i, sin_i, θ, cos_o and sin_o are all 16-bit signed data. cos_i is written to SCATx_COS, sin_i to SCATx_SIN and θ to SCATx_THE to calculate cos_o and sin_o. The results cos_o and sin_o are accessed by reading SCATx_RES1 and SCATx_RES2 respectively.

Table 14-6 Register Definitions in the Coordinate Transformation Mode

Data Register	Input	Output
SCATx_COS	cos_i	-
SCATx_SIN	sin_i	-
SCATx_THE	θ	-
SCATx_RES1	-	cos_o
SCATx_RES2	-	sin_o

14.2.8 Arctangent

When MDU_CR[MDUMOD] = 101, SMDU module works in arctangent (ATAN) mode.

ATAN calculates the amplitude and angle of a vector based on sine and cosine inputs as following formula.

$$U = \sqrt{(Usin\,\theta)^2 + (U\,cos\,\theta)^2}$$

$$\theta = tan^{-1}\left(\frac{U\,sin\,\theta}{Ucos\,\theta}\right)$$

Where,

Usinθ: Sin component of the vector

Ucosθ: Cosine component of the vector

θ: Calculated vector angle

U: Calculated vector amplitude

As shown in Table 14-7, *Ucosθ* and *Usinθ*, *U* and *θ* are 16-bit signed data. $Ucos_\theta$ is written to SCATx_COS and $Usin_\theta$ to SCATx_SIN to calculate *U* and *θ*. *U* and *θ* are accessed by reading SCATx_RES1 and SCATx_RES2 respectively.

Table 14-7 Register Definitions in ATAN Mode

Data Register	Input	Output
SCATx_COS	*Ucosθ*	-
SCATx_SIN	*Usinθ*	-
SCATx_RES1	-	*U*
SCATx_RES2	-	*θ*

14.2.9 PI

14.2.9.1 PI Introduction

PI controller is a linear controller, where the output is generated by linear combination of error proportional, integral and differential actions, and then implemented by an actuator. In motor control system, it is used to for speed and position control.

PI algorithm:

$$U_k = U_{k-1} + Kp \times (E_k - E_{k-1}) + Ki \times E_k$$

Where,

U_k: Output for round k of calculation

U_{k-1}: Output for round k-1 of calculation

E_k: Deviation for round k of input

E_{k-1} and E_{k-2}: Deviations for round k-1 and round k-2 of calculation

K_p and K_i: Proportional (P) and integral (I) coefficients of the controller

Maximum U_k is represented as PIx_UKMAX (x = 0 ~ 3) and the minimum value as PIx_UKMIN.

14.2.9.2 PI Features

- Parameter range is configurable
- Support multiple invocations but not with nested interrupt
- Produce a 32-bit result PIx_UK
- Results are read after Busy Flag is reset to “0”.

14.2.9.3 PI Operations

1. Initialize SMDU before operations, and configure K_p, K_i and the maximum and minimum values of U_k;
2. Set MDU_CR[MDUMOD] to 111, and then configure MDU_CR[MDUSTA] bit to select the desired computing unit and start PI computing. At this time, the busy flag MDU_CR[MDUBUSY] is automatically set to “1”;
3. Read MDU_CR[MDUBUSY] bit by software. When this bit is 0, it indicates that the calculation is completed, and calculation result PIx_UK is updated;
4. Read PIx_UK to obtain the output.

Note

- The data format of PI_KP is Q12 and that of other registers are Q15
- PIx_UK and PIx_EK1 values default to the previous calculated U_K and E_k The related values change after PIx_EK1 and PIx_UK are written
- When PI controller is invoked repeatedly, relevant parameters shall be saved after each PI operation, and

initialized before the next PI operation. Initialization codes are shown as below:

```
PIx_KP = KP;                    //Initialize Kp
PIx_KI = KI;                    //Initialize Ki
PIx_UKMAX = UKMAX;              //Initialize maximum output
PIx_UKMIN = UKMIN;              //Initialize minimum output
PIx_EK1 = X;                    //Initialize Ek-1
PIx_UKH = Y1;                   //Initialize 16 high-order bits of Uk-1
PIx_UKL = Y2;                   //Initialize 16 low-order bits of Uk-1
```

14.3 SMDU Registers

14.3.1 MDU_CR (0xC1)

Bit	7	6	5	4	3	2	1	0
Name	MDUBSY	MDUSTA				MDUMOD		
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	MDUBSY	After SMDU module is enabled, this bit is used to show operating status of the module. 0: Idle 1: Busy
[6:3]	MDUSTA	This bit is used to configure computing unit of the SMDU. Four options are available. SMDU module starts operation after initiating the computing. 0001: Comp_Unit0 is activated 0010: Comp_Unit1 is activated 0100: Comp_Unit2 is activated 1000: Comp_Unit3 is activated
[2:0]	MDUMOD	After SMDU module is enabled, this bit is used to select operating mode of the module. 000: Signed Multiplication (the result shifted left by one-bit) 001: Signed Multiplication 010: Unsigned Multiplication 011: 32-bit/16-bit Unsigned Division 100: Coordinate Transformation (SIN/COS) 101: ATAN 110: LPF 111: PI

Note

Configuring TIM234_CTRL[6] enables or disables SMDU module

14.3.2 TIM234_CTRL(0x40F1)

Bit	7	6	5	4	3	2	1	0
Name	RSV	MDU_EN_N	TIM2_FAST_DIR	TIM2_DR_SEL	TIM4_RCTRL	TIM3_RCTRL	TIM2_RCTRL	TIM3_48M
Type	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	0	0	0	0	0	0	0

Bit	Name	Description
[7]	RSV	Reserved
[6]	MDU_EN_N	When this bit is set to “1”, SMDU module is enabled and MDU module is disabled. 0: Disable 1: Enable
[5]	TIM2_FAST_DIR	After this bit is enabled in Timer2 QEP mode, SMDU module can quickly identify the direction. 0: Disable 1: Enable
[4]	TIM2_DR_SEL	After this bit is enabled in Timer2 QEP mode, the timer is reset to 0 or TIM2__DR when it reaches to TIM2__DR or 0. 0: Disable 1: Enable
[3]	TIM4_RCTRL	After this bit is enabled, DR = 0/0xFFFF when TIM4__ARR overflows. 0: Disable 1: Enable
[2]	TIM3_RCTRL	After this bit is enabled, DR = 0/0xFFFF when TIM3__ARR overflows. 0: Disable 1: Enable
[1]	TIM2_RCTRL	After this bit is enabled, DR = 0/0xFFFF when TIM2__ARR overflows. 0: Disable 1: Enable
[0]	TIM3_48M	TIM3_48M Input Capture Enable 0: Disable 1: Enable

14.3.3 MUL0_MA (0x03C8, 0x03C9)

MUL0_MAH(0x03C8)								
Bit	15	14	13	12	11	10	9	8
Name	MUL0_MA[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL0_MAL(0x03C9)								
Bit	7	6	5	4	3	2	1	0
Name	MUL0_MA[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	MUL0_MA	Data register A of MUL0; Multiplicand of the multiplication

14.3.4 MUL0_MB (0x03CA 0x03CB)

MUL0_MBH(0x03CA)								
Bit	15	14	13	12	11	10	9	8
Name	MUL0_MB[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL0_MBL(0x03CB)								
Bit	7	6	5	4	3	2	1	0
Name	MUL0_MB[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	MUL0_MB	Data register B of MUL0; Multiplier of the multiplication

14.3.5 MUL0_MC (0x03CC, 0x03CD, 0x03CE, 0x03CF)

MUL0_MCHH(0x03CC)								
Bit	31	30	29	28	27	26	25	24
Name	MUL0_MC[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL0_MCHL(0x03CD)								
Bit	23	22	21	20	19	18	17	16
Name	MUL0_MC[13:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset	0	0	0	0	0	0	0	0
MUL0_MCLH(0x03CE)								
Bit	15	14	13	12	11	10	9	8
Name	MUL0_MC[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL0_MCLL(0x03CF)								
Bit	7	6	5	4	3	2	1	0
Name	MUL0_MC[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	MUL0_MC	Product of MUL0. The 16 high-order bits of the data are held by MUL0_MCH, and the 16 low-order bits by MUL0_MCL.

14.3.6 MUL1_MA (0x03C0, 0x03C1)

MUL1_MAH(0x03C0)								
Bit	15	14	13	12	11	10	9	8
Name	MUL1_MA[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL1_MAL(0x03C1)								
Bit	7	6	5	4	3	2	1	0
Name	MUL1_MA[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	MUL1_MA	Data register A of MUL1; Multiplicand of the multiplication

14.3.7 MUL1_MB (0x03C2, 0x03C3)

MUL1_MBH(0x03C2)								
Bit	15	14	13	12	11	10	9	8
Name	MUL1_MB[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL1_MBL(0x03C3)								
Bit	7	6	5	4	3	2	1	0
Name	MUL1_MB[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	MUL1_MB	Data register B of MUL1; Multiplier of the multiplication

14.3.8 MUL1_MC (0x03C4, 0x03C5, 0x03C6, 0x03C7)

MUL1_MCHH(0x03C4)								
Bit	31	30	29	28	27	26	25	24
Name	MUL1_MC[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL1_MCHL(0x03C5)								
Bit	23	22	21	20	19	18	17	16
Name	MUL1_MC[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL1_MCLH(0x03C6)								
Bit	15	14	13	12	11	10	9	8
Name	MUL1_MC[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL1_MCLL(0x03C7)								
Bit	7	6	5	4	3	2	1	0
Name	MUL1_MC[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	MUL1_MC	Product of MUL1. The 16 high-order bits of the data are held by MUL1_MCH, and the 16 low-order bits by MUL1_MCL.

14.3.9 MUL2_MA (0x0370, 0x0371)

MUL2_MAH(0x0370)								
Bit	15	14	13	12	11	10	9	8
Name	MUL2_MA[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL2_MAL(0x0371)								
Bit	7	6	5	4	3	2	1	0
Name	MUL2_MA[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	MUL2_MA	Data register A of MUL2; Multiplicand of the multiplication

14.3.10 MUL2_MB (0x0372, 0x0373)

MUL2_MBH(0x0372)								
Bit	15	14	13	12	11	10	9	8
Name	MUL2_MB[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL2_MBL(0x0373)								
Bit	7	6	5	4	3	2	1	0
Name	MUL2_MB[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	MUL2_MB	Data register B of MUL2; Multiplier of the multiplication

14.3.11 MUL2_MC (0x0374, 0x0375, 0x0376, 0x0377)

MUL2_MCHH(0x0374)								
Bit	31	30	29	28	27	26	25	24
Name	MUL2_MC[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL2_MCHL(0x0375)								
Bit	23	22	21	20	19	18	17	16
Name	MUL2_MC[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL2_MCLH(0x0376)								
Bit	15	14	13	12	11	10	9	8
Name	MUL2_MC[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL2_MCLL(0x0377)								
Bit	7	6	5	4	3	2	1	0
Name	MUL2_MC[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	MUL2_MC	Product of MUL2. The 16 high-order bits of the data are held by MUL2_MCH, and the 16 low-order bits by MUL2_MCL.

14.3.12 MUL3_MA (0x0368, 0x0369)

MUL3_MAH(0x0368)								
Bit	15	14	13	12	11	10	9	8
Name	MUL3_MA[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL3_MAL(0x0369)								
Bit	7	6	5	4	3	2	1	0
Name	MUL3_MA[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	MUL3_MA	Data register A of MUL3; Multiplicand of the multiplication

14.3.13 MUL3_MB (0x036A, 0x036B)

MUL3_MBH(0x036A)								
Bit	15	14	13	12	11	10	9	8
Name	MUL3_MB[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL3_MBL(0x036B)								
Bit	7	6	5	4	3	2	1	0
Name	MUL3_MB[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	MUL3_MB	Data register B of MUL3; Multiplier of the multiplication

14.3.14 MUL3_MC (0x036C, 0x036D, 0x036E, 0x036F)

MUL3_MCHH(0x036C)								
Bit	31	30	29	28	27	26	25	24
Name	MUL3_MC[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL3_MCHL(0x036D)								
Bit	23	22	21	20	19	18	17	16

Name	MUL3_MC[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL3_MCLH(0x036E)								
Bit	15	14	13	12	11	10	9	8
Name	MUL3_MC[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
MUL3_MCLL(0x036F)								
Bit	7	6	5	4	3	2	1	0
Name	MUL3_MC[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	MUL3_MC	Product of MUL3. The 16 high-order bits of the data are held by MUL3_MCH, and the 16 low-order bits by MUL3_MCL.

14.3.15 DIV0_DA (0x03B4, 0x03B5, 0x03B6, 0x03B7)

DIV0_DAHH(0x03B4)								
Bit	31	30	29	28	27	26	25	24
Name	DIV0_DA[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV0_DAHL(0x03B5)								
Bit	23	22	21	20	19	18	17	16
Name	DIV0_DA[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV0_DALH(0x03B6)								
Bit	15	14	13	12	11	10	9	8
Name	DIV0_DA[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV0_DALL(0x03B7)								
Bit	7	6	5	4	3	2	1	0
Name	DIV0_DA[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	DIV0_DA	Dividend of DIV0. The 16 high-order bits of the data are held by DIV0_DAH, and the 16 low-order bits by DIV0_DAL.

14.3.16 DIV0_DB (0x03B8, 0x03B9)

DIV0_DBH(0x03B8)								
Bit	15	14	13	12	11	10	9	8
Name	DIV0_DB[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV0_DBL(0x03B9)								
Bit	7	6	5	4	3	2	1	0
Name	DIV0_DB[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	DIV0_DB	Data register B of DIV0; Divisor of the division

14.3.17 DIV0_DQ (0x03BA, 0x03BB, 0x03BC, 0x03BD)

DIV0_DQHH(0x03BA)								
Bit	31	30	29	28	27	26	25	24
Name	DIV0_DQ[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV0_DQHL(0x03BB)								
Bit	23	22	21	20	19	18	17	16
Name	DIV0_DQ[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV0_DQLH(0x03BC)								
Bit	15	14	13	12	11	10	9	8
Name	DIV0_DQ[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV0_DQLL(0x03BD)								
Bit	7	6	5	4	3	2	1	0
Name	DIV0_DQ[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	DIV0_DQ	Quotient of DIV0. The 16 high-order bits of the data are held by DIV0_DQH, and the 16 low-order bits by DIV0_DQL.

14.3.18 DIV0_DR (0x03BE, 0x03BF)

DIV0_DRH(0x03BE)								
Bit	15	14	13	12	11	10	9	8
Name	DIV0_DR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV0_DRL(0x03BF)								
Bit	7	6	5	4	3	2	1	0
Name	DIV0_DR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	DIV0_DR	Remainder of DIV0

14.3.19 DIV1_DA (0x03A8, 0x03A9, 0x03AA, 0x03AB)

DIV1_DAHH(0x03A8)								
Bit	31	30	29	28	27	26	25	24
Name	DIV1_DA[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV1_DAHL(0x03A9)								
Bit	23	22	21	20	19	18	17	16
Name	DIV1_DA[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV1_DALH(0x03AA)								
Bit	15	14	13	12	11	10	9	8
Name	DIV1_DA[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV1_DALL(0x03AB)								
Bit	7	6	5	4	3	2	1	0
Name	DIV1_DA[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	DIV1_DA	Dividend of DIV1. The 16 high-order bits of the data are held by DIV1_DAH, and the 16 low-order bits by DIV1_DAL

14.3.20 DIV1_DB (0x03AC, 0x03AD)

DIV1_DBH(0x03AC)								
Bit	15	14	13	12	11	10	9	8
Name	DIV1_DB[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV1_DBL(0x03AD)								
Bit	7	6	5	4	3	2	1	0
Name	DIV1_DB[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	DIV1_DB	Data register B of DIV1; Divisor of the division

14.3.21 DIV1_DQ (0x03AE, 0x03AF, 0x03B0, 0x03B1)

DIV1_DQHH(0x03AE)								
Bit	31	30	29	28	27	26	25	24
Name	DIV1_DQ[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV1_DQHL(0x03AF)								
Bit	23	22	21	20	19	18	17	16
Name	DIV1_DQ[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV1_DQLH(0x03B0)								
Bit	15	14	13	12	11	10	9	8
Name	DIV1_DQ[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV1_DQLL(0x03B1)								
Bit	7	6	5	4	3	2	1	0
Name	DIV1_DQ[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	DIV1_DQ	Quotient of DIV1. The 16 high-order bits of the data are held by DIV1_DQH, and the 16 low-order bits by DIV1_DQL

14.3.22 DIV1_DR (0x03B2, 0x03B3)

DIV1_DRH(0x03B2)								
Bit	15	14	13	12	11	10	9	8
Name	DIV1_DR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV1_DRL(0x03B3)								
Bit	7	6	5	4	3	2	1	0
Name	DIV1_DR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	DIV1_DR	Remainder of DIV1

14.3.23 DIV2_DA (0x035C, 0x035D, 0x035E, 0x035F)

DIV2_DAHH(0x035C)								
Bit	31	30	29	28	27	26	25	24
Name	DIV2_DA[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV2_DAHL(0x035D)								
Bit	23	22	21	20	19	18	17	16
Name	DIV2_DA[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV2_DALH(0x035E)								
Bit	15	14	13	12	11	10	9	8
Name	DIV2_DA[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV2_DALL(0x035F)								
Bit	7	6	5	4	3	2	1	0
Name	DIV2_DA[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	DIV2_DA	Dividend of DIV2. The 16 high-order bits of the data are held by DIV2_DAH, and the 16 low-order bits by DIV2_DAL

14.3.24 DIV2_DB (0x0360, 0x0361)

DIV2_DBH(0x0360)								
Bit	15	14	13	12	11	10	9	8
Name	DIV2_DB[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV2_DBL(0x0361)								
Bit	7	6	5	4	3	2	1	0
Name	DIV2_DB[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	DIV2_DB	Data register B of DIV2; Divisor of the division

14.3.25 DIV2_DQ (0x0362, 0x0363, 0x0364, 0x0365)

DIV2_DQHH(0x0362)								
Bit	31	30	29	28	27	26	25	24
Name	DIV2_DQ[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV2_DQHL(0x0363)								
Bit	23	22	21	20	19	18	17	16
Name	DIV2_DQ[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV2_DQLH(0x0364)								
Bit	15	14	13	12	11	10	9	8
Name	DIV2_DQ[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV2_DQLL(0x0365)								
Bit	7	6	5	4	3	2	1	0
Name	DIV2_DQ[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	DIV2_DQ	Quotient of DIV2. The 16 high-order bits of the data are held by DIV2_DQH, and the 16 low-order bits by DIV2_DQL

14.3.26 DIV2_DR (0x0366, 0x0367)

DIV2_DRH(0x0366)								
Bit	15	14	13	12	11	10	9	8
Name	DIV2_DR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV2_DRL(0x0367)								
Bit	7	6	5	4	3	2	1	0
Name	DIV2_DR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	DIV2_DR	Remainder of DIV2

14.3.27 DIV3_DA (0x0350, 0x0351, 0x0352, 0x0353)

DIV3_DAHH(0x0350)								
Bit	31	30	29	28	27	26	25	24
Name	DIV3_DA[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV3_DAHL(0x0351)								
Bit	23	22	21	20	19	18	17	16
Name	DIV3_DA[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV3_DALH(0x0352)								
Bit	15	14	13	12	11	10	9	8
Name	DIV3_DA[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV3_DALL(0x0353)								
Bit	7	6	5	4	3	2	1	0
Name	DIV3_DA[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	DIV3_DA	Dividend of DIV3. The 16 high-order bits of the data are held by DIV3_DAH, and the 16 low-order bits by DIV3_DAL

14.3.28 DIV3_DB (0x0354, 0x0355)

DIV3_DBH(0x0354)								
Bit	15	14	13	12	11	10	9	8
Name	DIV3_DB[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV3_DBL(0x0355)								
Bit	7	6	5	4	3	2	1	0
Name	DIV3_DB[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	DIV3_DB	Data register B of DIV3; Divisor of the division

14.3.29 DIV3_DQ (0x0356, 0x0357, 0x0358, 0x0359)

DIV3_DQHH(0x0356)								
Bit	31	30	29	28	27	26	25	24
Name	DIV3_DQ[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV3_DQHL(0x0357)								
Bit	23	22	21	20	19	18	17	16
Name	DIV3_DQ[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV3_DQLH(0x0358)								
Bit	15	14	13	12	11	10	9	8
Name	DIV3_DQ[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV3_DQLL(0x0359)								
Bit	7	6	5	4	3	2	1	0
Name	DIV3_DQ[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	DIV3_DQ	Quotient of DIV3. The 16 high-order bits of the data are held by DIV3_DQH, and the 16 low-order bits by DIV3_DQL

14.3.30 DIV3_DR (0x035A, 0x035B)

DIV3_DRH(0x035A)								
Bit	15	14	13	12	11	10	9	8
Name	DIV3_DR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DIV3_DRL(0x035B)								
Bit	7	6	5	4	3	2	1	0
Name	DIV3_DR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	DIV3_DR	Remainder of DIV3

14.3.31 SCAT0_COS (0x0346, 0x0347)

SCAT0_COSH(0x0346)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT0_COS[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT0_COSL(0x0347)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT0_COS[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT0_COS	COS input in SIN/COS or ATAN mode of computing unit SCAT0

14.3.32 SCAT0_SIN (0x0348, 0x0349)

SCAT0_SINH(0x0348)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT0_SIN[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SCAT0_SINL(0x0349)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT0_SIN[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT0_SIN	SIN input in SIN/COS or ATAN mode of computing unit SCAT0

14.3.33 SCAT0_THE (0x034A, 0x034B)

SCAT0_THEH(0x034A)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT0_THE[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT0_THEL(0x034B)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT0_THE[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT0_THE	THE input in SIN/COS mode of computing unit SCAT0

14.3.34 SCAT0_RES1 (0x034C, 0x034D)

SCAT0_RES1H(0x034C)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT0_RES1[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT0_RES1L(0x034D)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT0_RES1[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT0_RES1	COS output in SIN/COS mode of computing unit SCAT0; U output in ATAN mode

14.3.35 SCAT0_RES2 (0x034E, 0x034F)

SCAT0_RES2H(0x034E)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT0_RES2[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT0_RES2L(0x034F)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT0_RES2[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT0_RES2	SIN output in SIN/COS mode of computing unit SCAT0; θ output in ATAN mode

14.3.36 SCAT1_COS (0x033C, 0x033D)

SCAT1_COSH(0x033C)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT1_COS[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT1_COSL(0x033D)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT1_COS[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT1_COS	COS input in SIN/COS or ATAN mode of computing unit SCAT1

14.3.37 SCAT1_SIN (0x033E, 0x033F)

SCAT1_SINH(0x033E)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT1_SIN[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT1_SINL(0x033F)								
Bit	7	6	5	4	3	2	1	0

Name	SCAT1_SIN[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT1_SIN	SIN input in SIN/COS or ATAN mode of computing unit SCAT1

14.3.38 SCAT1_THE (0x0340, 0x0341)

SCAT1_THEH(0x0340)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT1_THE[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT1_THEL(0x0341)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT1_THE[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT1_THE	THE input in SIN/COS mode of computing unit SCAT1

14.3.39 SCAT1_RES1 (0x0342, 0x0343)

SCAT1_RES1H(0x0342)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT1_RES1[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT1_RES1L(0x0343)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT1_RES1[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT1_RES1	COS output in SIN/COS mode of computing unit SCAT1; U output in ATAN mode

14.3.40 SCAT1_RES2 (0x0344, 0x0345)

SCAT1_RES2H(0x0344)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT1_RES2[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT1_RES2L(0x0345)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT1_RES2[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT1_RES2	SIN output in SIN/COS mode of computing unit SCAT1; θ output in ATAN mode

14.3.41 SCAT2_COS (0x0332, 0x0333)

SCAT2_COSH(0x0332)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT2_COS[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT2_COSL(0x0333)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT2_COS[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT2_COS	COS input in SIN/COS or ATAN mode of computing unit SCAT2

14.3.42 SCAT2_SIN (0x0334, 0x0335)

SCAT2_SINH(0x0334)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT2_SIN[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT2_SINL(0x0335)								
Bit	7	6	5	4	3	2	1	0

Name	SCAT2_SIN[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT2_SIN	SIN input in SIN/COS or ATAN mode of computing unit SCAT2

14.3.43 SCAT2_THE (0x0336, 0x0337)

SCAT2_THEH(0x0336)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT2_THE[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT2_THEL(0x0337)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT2_THE[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT2_THE	THE input in SIN/COS mode of computing unit SCAT2

14.3.44 SCAT2_RES1 (0x0338, 0x0339)

SCAT2_RES1H(0x0338)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT2_RES1[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT2_RES1L(0x0339)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT2_RES1[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT2_RES1	COS output in SIN/COS mode of computing unit SCAT2; U output in ATAN mode

14.3.45 SCAT2_RES2 (0x033A, 0x033B)

SCAT2_RES2H(0x033A)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT2_RES[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT2_RES2L(0x033B)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT2_RES[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT2_RES2	SIN output in SIN/COS mode of computing unit SCAT2; θ output in ATAN mode

14.3.46 SCAT3_COS (0x0328, 0x0329)

SCAT3_COSH(0x0328)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT3_COS[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT3_COSL(0x0329)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT3_COS[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT3_COS	COS input in SIN/COS or ATAN mode of computing unit SCAT3

14.3.47 SCAT3_SIN (0x032A, 0x032B)

SCAT3_SINH(0x032A)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT3_SIN[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT3_SINL(0x032B)								
Bit	7	6	5	4	3	2	1	0

Name	SCAT3_SIN[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT3_SIN	SIN input in SIN/COS or ATAN mode of computing unit SCAT3

14.3.48 SCAT3_THE (0x032C, 0x032D)

SCAT3_THEH(0x032C)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT3_THE[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT3_THEL(0x032D)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT3_THE[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT3_THE	THE input in SIN/COS mode of computing unit SCAT3

14.3.49 SCAT3_RES1 (0x032E, 0x032F)

SCAT3_RES1H(0x032E)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT3_RES1[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT3_RES1L(0x032F)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT3_RES1[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT3_RES1	COS output in SIN/COS mode of computing unit SCAT3; U output in ATAN mode

14.3.50 SCAT3_RES2 (0x0330, 0x0331)

SCAT3_RES2H(0x0330)								
Bit	15	14	13	12	11	10	9	8
Name	SCAT3_RES[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
SCAT3_RES2L(0x0331)								
Bit	7	6	5	4	3	2	1	0
Name	SCAT3_RES[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	SCAT3_RES2	SIN output in SIN/COS mode of computing unit SCAT3; θ output in ATAN mode

14.3.51 LPF0_K (0x03F8, 0x03F9)

LPF0_KH(0x03F8)								
Bit	15	14	13	12	11	10	9	8
Name	LPF0_K[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF0_KL(0x03F9)								
Bit	7	6	5	4	3	2	1	0
Name	LPF0_K[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	LPF0_K	K input of LPF0

14.3.52 LPF0_X (0x03FA, 0x03FB)

LPF0_XH(0x03FA)								
Bit	15	14	13	12	11	10	9	8
Name	LPF0_X[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF0_XL(0x03FB)								
Bit	7	6	5	4	3	2	1	0

Name	LPF0_X[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	LPF0_X	X input of LPF0

14.3.53 LPF0_Y (0x03FC, 0x03FD, 0x03FE, 0x03FF)

LPF0_YHH(0x03FC)								
Bit	31	30	29	28	27	26	25	24
Name	LPF0_Y[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF0_YHL(0x03FD)								
Bit	23	22	21	20	19	18	17	16
Name	LPF0_Y[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF0_YLH(0x03FE)								
Bit	15	14	13	12	11	10	9	8
Name	LPF0_Y[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF0_YLL(0x03FF)								
Bit	7	6	5	4	3	2	1	0
Name	LPF0_Y[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	LPF0_Y	Input and output of the register in LPF0 Input: LPF0_Y_{k-1} Output: LPF0_Y_k

14.3.54 LPF1_K (0x03F0, 0x03F1)

LPF1_KH(0x03F0)								
Bit	15	14	13	12	11	10	9	8
Name	LPF1_K[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

LPF1_KL(0x03F1)								
Bit	7	6	5	4	3	2	1	0
Name	LPF1_K[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	LPF1_K	K input of LPF1

14.3.55 LPF1_X (0x03F2, 0x03F3)

LPF1_XH(0x03F2)								
Bit	15	14	13	12	11	10	9	8
Name	LPF1_X[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF1_XL(0x03F3)								
Bit	7	6	5	4	3	2	1	0
Name	LPF1_X[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	LPF1_X	X input of LPF1

14.3.56 LPF1_Y (0x03F4, 0x03F5, 0x03F6, 0x03F7)

LPF1_YHH(0x03F4)								
Bit	31	30	29	28	27	26	25	24
Name	LPF1_Y[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF1_YHL(0x03F5)								
Bit	23	22	21	20	19	18	17	16
Name	LPF1_Y[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF1_YLH(0x03F6)								
Bit	15	14	13	12	11	10	9	8
Name	LPF1_Y[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF1_YLL(0x03F7)								

Bit	7	6	5	4	3	2	1	0
Name	LPF1_Y[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	LPF1_Y	Input and output of the register in LPF1 Input: LPF1_Y_{k-1} Output: LPF1_Y_k

14.3.57 LPF2_K (0x03A0, 0x03A1)

LPF2_KH(0x03A0)								
Bit	15	14	13	12	11	10	9	8
Name	LPF2_K[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF2_KL(0x03A1)								
Bit	7	6	5	4	3	2	1	0
Name	LPF2_K[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	LPF2_K	K input of LPF2

14.3.58 LPF2_X (0x03A2, 0x03A3)

LPF2_XH(0x03A2)								
Bit	15	14	13	12	11	10	9	8
Name	LPF2_X[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF2_XL(0x03A3)								
Bit	7	6	5	4	3	2	1	0
Name	LPF2_X[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	LPF2_X	X input of LPF2

14.3.59 LPF2_Y (0x03A4, 0x03A5, 0x03A6, 0x03A7)

LPF2_YHH(0x03A4)								
Bit	31	30	29	28	27	26	25	24
Name	LPF2_Y[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF2_YHL(0x03A5)								
Bit	23	22	21	20	19	18	17	16
Name	LPF2_Y[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF2_YLH(0x03A6)								
Bit	15	14	13	12	11	10	9	8
Name	LPF2_Y[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF2_YLL(0x03A7)								
Bit	7	6	5	4	3	2	1	0
Name	LPF2_Y[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	LPF2_Y	Input and output of the register in LPF2 Input: LPF2_Y_{k-1} Output: LPF2_Y_k

14.3.60 LPF3_K (0x0398, 0x0399)

LPF3_KH(0x0398)								
Bit	15	14	13	12	11	10	9	8
Name	LPF3_K[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF3_KL(0x0399)								
Bit	7	6	5	4	3	2	1	0
Name	LPF3_K[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	LPF3_K	K input of LPF3

14.3.61 LPF3_X (0x039A, 0x039B)

LPF3_XH(0x039A)								
Bit	15	14	13	12	11	10	9	8
Name	LPF3_X[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF3_XL(0x039B)								
Bit	7	6	5	4	3	2	1	0
Name	LPF3_X[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	LPF3_K	X input of LPF3

14.3.62 LPF3_Y (0x039C, 0x039D, 0x039E, 0x039F)

LPF3_YHH(0x039C)								
Bit	31	30	29	28	27	26	25	24
Name	LPF3_Y[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF3_YHL(0x039D)								
Bit	23	22	21	20	19	18	17	16
Name	LPF3_Y[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF3_YLH(0x039E)								
Bit	15	14	13	12	11	10	9	8
Name	LPF3_Y[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
LPF3_YLL(0x039F)								
Bit	7	6	5	4	3	2	1	0
Name	LPF3_Y[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	LPF3_Y	Input and output of the register in LPF3 Input: LPF3_Y_{k-1} Output: LPF3_Y_k

14.3.63 PI0_KP (0x03E0, 0x03E1)

PI0_KPH(0x03E0)								
Bit	15	14	13	12	11	10	9	8
Name	PI0_KP[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI0_KPL(0x03E1)								
Bit	7	6	5	4	3	2	1	0
Name	PI0_KP[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI0_KP	Proportional coefficient of PI0

14.3.64 PI0_EK1 (0x03E2, 0x03E3)

PI0_EK1H(0x03E2)								
Bit	15	14	13	12	11	10	9	8
Name	PI0_EK1[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI0_EK1L(0x03E3)								
Bit	7	6	5	4	3	2	1	0
Name	PI0_EK1[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI0_EK1	Previous input deviation of PI0

14.3.65 PI0_EK (0x03E4, 0x03E5)

PI0_EKH(0x03E4)								
Bit	15	14	13	12	11	10	9	8
Name	PI0_EK[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI0_EKL(0x03E5)								
Bit	7	6	5	4	3	2	1	0
Name	PI0_EK[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI0_EK	Present input deviation of PI0

14.3.66 PI0_KI (0x03E6, 0x03E7)

PI0_KIH(0x03E6)								
Bit	15	14	13	12	11	10	9	8
Name	PI0_KI[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI0_KIL(0x03E7)								
Bit	7	6	5	4	3	2	1	0
Name	PI0_KI[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI0_KI	Integral coefficient of PI0

14.3.67 PI0_UKH (0x03E8, 0x03E9)

PI0_UKHH(0x03E8)								
Bit	15	14	13	12	11	10	9	8
Name	PI0_UKH[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI0_UKHL(0x03E9)								
Bit	7	6	5	4	3	2	1	0

Name	PI0_UKH[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI0_UKH	16 high-order bits of PI0 output

14.3.68 PI0_UKL (0x03EA, 0x03EB)

PI0_UKLH(0x03EA)								
Bit	15	14	13	12	11	10	9	8
Name	PI0_UKL[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI0_UKLL(0x03EB)								
Bit	7	6	5	4	3	2	1	0
Name	PI0_UKL[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI0_UKL	16 low-order bits of PI0 output

14.3.69 PI0_UKMAX (0x03EC, 0x03ED)

PI0_UKMAXH(0x03EC)								
Bit	15	14	13	12	11	10	9	8
Name	PI0_UKMAX[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI0_UKMAXL(0x03ED)								
Bit	7	6	5	4	3	2	1	0
Name	PI0_UKMAX[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI0_UKMAX	Maximum output of PI0

14.3.70 PI0_UKMIN (0x03EE, 0x03EF)

PI0_UKMINH(0x03EE)								
Bit	15	14	13	12	11	10	9	8
Name	PI0_UKMIN[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI0_UKMINL(0x03EF)								
Bit	7	6	5	4	3	2	1	0
Name	PI0_UKMIN[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI0_UKMIN	Minimum output of PI0

14.3.71 PI1_KP (0x03D0, 0x03D1)

PI1_KPH(0x03D0)								
Bit	15	14	13	12	11	10	9	8
Name	PI1_KP[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI1_KPL(0x03D1)								
Bit	7	6	5	4	3	2	1	0
Name	PI1_KP[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI1_KP	Proportional coefficient of PI1

14.3.72 PI1_EK1 (0x03D2, 0x03D3)

PI1_EK1H(0x03D2)								
Bit	15	14	13	12	11	10	9	8
Name	PI1_EK1[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI1_EK1L(0x03D3)								
Bit	7	6	5	4	3	2	1	0

Name	PI1_EK1[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI1_EK1	Previous input deviation of PI1

14.3.73 PI1_EK (0x03D4, 0x03D5)

PI1_EKH(0x03D4)								
Bit	15	14	13	12	11	10	9	8
Name	PI1_EK[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI1_EKL(0x03D5)								
Bit	7	6	5	4	3	2	1	0
Name	PI1_EK[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI1_EK	Present input deviation of PI1

14.3.74 PI1_KI (0x03D6, 0x03D7)

PI1_KIH(0x03D6)								
Bit	15	14	13	12	11	10	9	8
Name	PI1_KI[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI1_KIL(0x03D7)								
Bit	7	6	5	4	3	2	1	0
Name	PI1_KI[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI1_KI	Integral coefficient of PI1

14.3.75 PI1_UKH (0x03D8, 0x03D9)

PI1_UKHH(0x03D8)								
Bit	15	14	13	12	11	10	9	8
Name	PI1_UKH[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI1_UKHL(0x03D9)								
Bit	7	6	5	4	3	2	1	0
Name	PI1_UKH[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI1_UKH	16 high-order bits of PI1 output

14.3.76 PI1_UKL (0x03DA, 0x03DB)

PI1_UKLH(0x03DA)								
Bit	15	14	13	12	11	10	9	8
Name	PI1_UKL[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI1_UKLL(0x03DB)								
Bit	7	6	5	4	3	2	1	0
Name	PI1_UKL[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI1_UKL	16 low-order bits of PI1 output

14.3.77 PI1_UKMAX (0x03DC, 0x03DD)

PI1_UKMAXH(0x03DC)								
Bit	15	14	13	12	11	10	9	8
Name	PI1_UKMAX[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI1_UKMAXL(0x03DD)								
Bit	7	6	5	4	3	2	1	0

Name	PI1_UKMAX[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI1_UKMAX	Maximum output of PI1

14.3.78 PI1_UKMIN (0x03DE, 0x03DF)

PI1_UKMINH(0x03DE)								
Bit	15	14	13	12	11	10	9	8
Name	PI1_UKMIN[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI1_UKMINL(0x03DF)								
Bit	7	6	5	4	3	2	1	0
Name	PI1_UKMIN[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI1_UKMIN	Minimum output of PI1

14.3.79 PI2_KP (0x0388, 0x0389)

PI2_KPH(0x0388)								
Bit	15	14	13	12	11	10	9	8
Name	PI2_KP[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI2_KPL(0x0389)								
Bit	7	6	5	4	3	2	1	0
Name	PI2_KP[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI2_KP	Proportional coefficient of PI2

14.3.80 PI2_EK1 (0x038A, 0x038B)

PI2_EK1H(0x038A)								
Bit	15	14	13	12	11	10	9	8
Name	PI2_EK1[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI2_EK1L(0x038B)								
Bit	7	6	5	4	3	2	1	0
Name	PI2_EK1[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI2_EK1	Previous input deviation of PI2

14.3.81 PI2_EK (0x038C, 0x038D)

PI2_EKH(0x038C)								
Bit	15	14	13	12	11	10	9	8
Name	PI2_EK[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI2_EKL(0x038D)								
Bit	7	6	5	4	3	2	1	0
Name	PI2_EK[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI2_EK	Present input deviation of PI2

14.3.82 PI2_KI (0x038E, 0x038F)

PI2_KIH(0x038E)								
Bit	15	14	13	12	11	10	9	8
Name	PI2_KI[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI2_KIL(0x038F)								
Bit	7	6	5	4	3	2	1	0

Name	PI2_KI[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI2_KI	Integral coefficient of PI2

14.3.83 PI2_UKH (0x0390, 0x0391)

PI2_UKHH(0x0390)								
Bit	15	14	13	12	11	10	9	8
Name	PI2_UKH[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI2_UKHL(0x0391)								
Bit	7	6	5	4	3	2	1	0
Name	PI2_UKH[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI2_UKH	16 high-order bits of PI2 output

14.3.84 PI2_UKL (0x0392, 0x0393)

PI2_UKLH(0x0392)								
Bit	15	14	13	12	11	10	9	8
Name	PI2_UKL[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI2_UKLL(0x0393)								
Bit	7	6	5	4	3	2	1	0
Name	PI2_UKL[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI2_UKL	16 low-order bits of PI2 output

14.3.85 PI2_MAX (0x0394, 0x0395)

PI2_MAXH(0x0394)								
Bit	15	14	13	12	11	10	9	8
Name	PI2_MAX[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI2_MAXL(0x0395)								
Bit	7	6	5	4	3	2	1	0
Name	PI2_MAX[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI2_MAX	Maximum output of PI2

14.3.86 PI2_MIN (0x0396, 0x0397)

PI2_MINH(0x0396)								
Bit	15	14	13	12	11	10	9	8
Name	PI2_MIN[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI2_MINL(0x0397)								
Bit	7	6	5	4	3	2	1	0
Name	PI2_MIN[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI2_MIN	Minimum output of PI2

14.3.87 PI3_KP (0x0378, 0x0379)

PI3_KPH(0x0378)								
Bit	15	14	13	12	11	10	9	8
Name	PI3_KP[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI3_KPL(0x0379)								
Bit	7	6	5	4	3	2	1	0

Name	PI3_KP[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI3_KP	Proportional coefficient of PI3

14.3.88 PI3_EK1 (0x037A, 0x037B)

PI3_EK1H(0x037A)								
Bit	15	14	13	12	11	10	9	8
Name	PI3_EK1[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI3_EK1L(0x037B)								
Bit	7	6	5	4	3	2	1	0
Name	PI3_EK1[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI3_EK1	Previous input deviation of PI3

14.3.89 PI3_EK (0x037C, 0x037D)

PI3_EKH(0x037C)								
Bit	15	14	13	12	11	10	9	8
Name	PI3_EK[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI3_EKL(0x037D)								
Bit	7	6	5	4	3	2	1	0
Name	PI3_EK[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI3_EK	Present input deviation of PI3

14.3.90 PI3_KI (0x037E, 0x037F)

PI3_KIH(0x037E)								
Bit	15	14	13	12	11	10	9	8
Name	PI3_KI[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI3_KIL(0x037F)								
Bit	7	6	5	4	3	2	1	0
Name	PI3_KI[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI3_KI	Integral coefficient of PI3

14.3.91 PI3_UKH (0x0380, 0x0381)

PI3_UKHH(0x0380)								
Bit	15	14	13	12	11	10	9	8
Name	PI3_UKH[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI3_UKHL(0x0381)								
Bit	7	6	5	4	3	2	1	0
Name	PI3_UKH[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI3_UKH	16 high-order bits of PI3 output

14.3.92 PI3_UKL (0x0382, 0x0383)

PI3_UKLH(0x0382)								
Bit	15	14	13	12	11	10	9	8
Name	PI3_UKL[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI3_UKLL(0x0383)								
Bit	7	6	5	4	3	2	1	0

Name	PI3_UKL[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI3_UKL	16 low-order bits of PI3 output

14.3.93 PI3_UKMAX (0x0384, 0x0385)

PI3_UKMAXH(0x0384)								
Bit	15	14	13	12	11	10	9	8
Name	PI3_UKMAX[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI3_UKMAXL(0x0385)								
Bit	7	6	5	4	3	2	1	0
Name	PI3_UKMAX[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI3_UKMAX	Maximum output of PI3

14.3.94 PI3_UKMIN (0x0386, 0x0387)

PI3_UKMINH(0x0386)								
Bit	15	14	13	12	11	10	9	8
Name	PI3_UKMIN[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
PI3_UKMINL(0x0387)								
Bit	7	6	5	4	3	2	1	0
Name	PI3_UKMIN[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	PI3_UKMIN	Minimum output of PI3

15 FOC

15.1 FOC Overview

FU6861NF2 does not support the functions in this chapter.

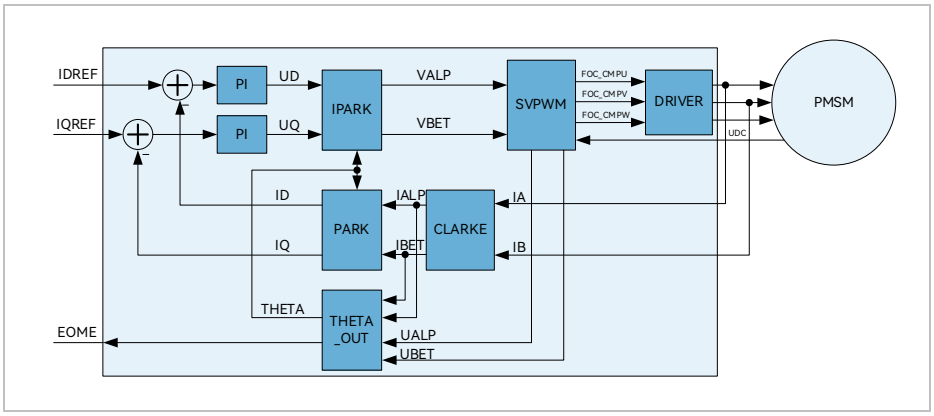
15.1.1 FOC Introduction

The FOC/SVPWM module is used in sensorless and sensored FOC motor drive applications and SVPWM-based motor control applications. Since SVPWM is a subset of FOC module, the following FOC/SVPWM module is referred to as FOC module for short. When DRV_CR[FOCEN] = 0, FOC module is inactivated, and FOC clock stops. The relevant FOC registers are forced into the reset state and cannot be written.

FOC module consists of angle estimator, PI controller, coordinate transform module and PWM output module. The internal angle estimator can be used to implement sensorless FOC-based control. MCU can also process Hall signals to implement sensored FOC-based control. Moreover, FOC module contains a closed current loop, which outputs six-channel PWM signals to drive the motor based on user-defined ID and IQ. Meanwhile, ADC automatically samples current signals to fulfill closed loop current control.

- Sensorless FOC: Angle for coordinate transformation is obtained by angle estimator, the motor speed is estimated for speed closed-loop control and BEMF is sensed for startup detection.
- Sensor-based FOC (Single/Dual/Triple Hall Sensors): FOC module provides the angle input interface. MCU samples Hall signals and calculates electrical angle of the motor, and sends the result to FOC module for coordinate transformation.

Figure 15-1 Block Diagram of FOC Module



15.1.2 Reference Input

The FOC module uses the d-axis current reference value FOC_IDREF and the q-axis current reference value FOC_IQREF as the reference, and uses the d-axis current sampling value FOC_ID and the q-axis current sampling value FOC_IQ as the feedback to realize current closed-loop control. FOC module outputs real-time estimated motor speed FOC_ EOME, and MCU can use FOC_EOME as the feedback to build speed loop and send the output of speed loop to FOC_IQREF to implement speed-current dual closed loop control.

15.1.3 PI Controller

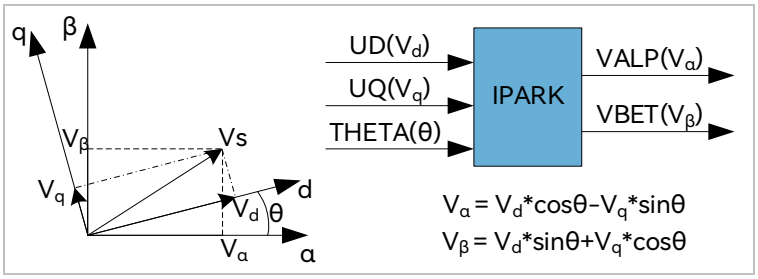
FOC module uses 4 PI controllers, which are respectively applied to:

5. Rotor flux control: PI controller of d-axis current, with reference current FOC_IDREF minus feedback current FOC_ID as deviation input, proportional coefficient FOC_DKP and integral coefficient FOC_DKI for the adjustment of PI controller performance, FOC_DMAX and FOC_DMIN for limiting of the output amplitude. The output is voltage reference of d-axis FOC_UD.
6. Torque control: PI controller of q-axis current, with current reference FOC_IQREF minus feedback current FOC_IQ as deviation input, proportional coefficient FOC_DQKP and the integral coefficient FOC_DQKI for the adjustment of PI controller performance, and FOC_QMAX and FOC_QMIN for limiting of the output amplitude. The output is voltage reference of q-axis FOC_UQ.
7. Angle estimation: PI controller of the estimator, with proportional coefficient FOC_EKP and integral coefficient FOC_EKI for the adjustment of PI controller performance. The output is estimated angle FOC_ETHETA.
8. PLL estimation: PI controller of PLL estimator, with proportional coefficient FOC_PLLKP and integral coefficient FOC_PLLKI for the adjustment of PI controller performance. The output is estimated BEMF FOC_EALP and FOC_EBET.

15.1.4 Coordinate Transformation

15.1.4.1 Inverse Park Transformation

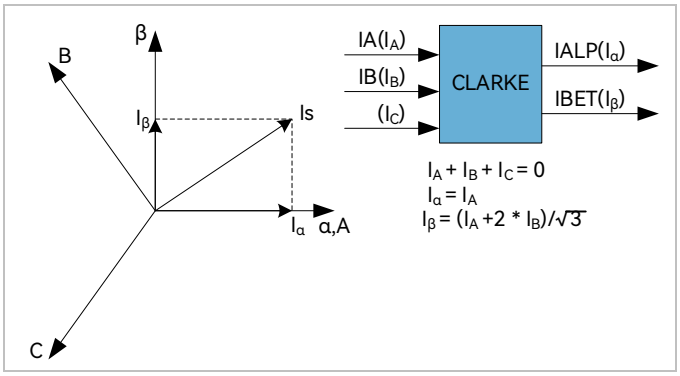
Figure 15-2 Inverse Park Transformation



Inverse Park transformation is used to transform two voltage vectors obtained by PI controller, FOC_UD and FOC_UQ, from d/q-axis coordinate to α/β-axis coordinate.

15.1.4.2 Clarke Transformation

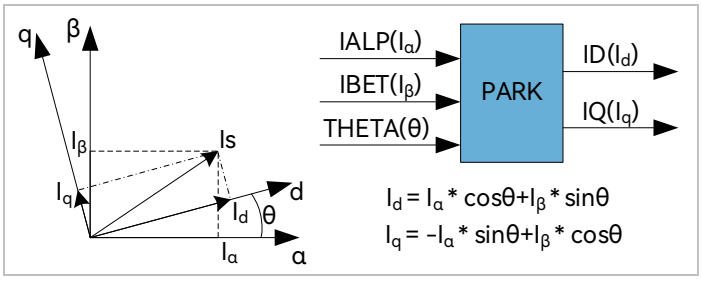
Figure 15-3 Clarke Transformation



Clarke transformation is used to transform the sampled current from 3-phase stationary coordinate to α/β-axis coordinate.

15.1.4.3 Park Transformation

Figure 15-4 Park Transformation



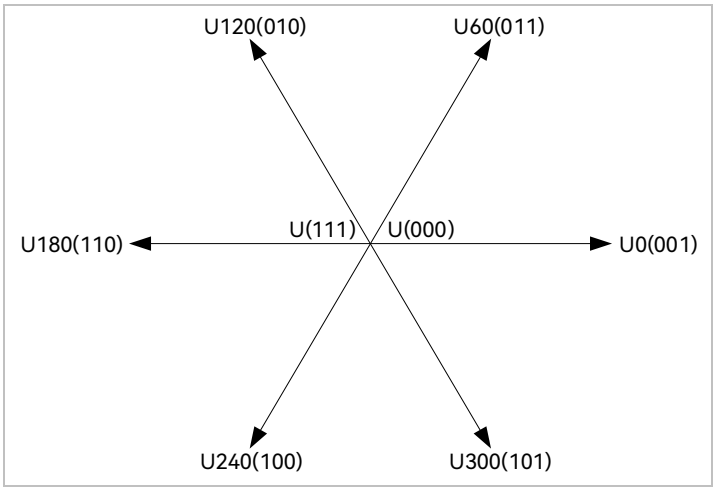
Park transformation is used to transform the current vectors, obtained after Clarke transformation, from α/β-axis coordinate to d/q-axis coordinate to get the sampled d/q-axis current FOC_ID and FOC_IQ.

15.1.5 SVPWM

SVPWM algorithm is an important part of FOC. The main idea is to obtain quasi-circular rotating magnetic field by switching the inverter space voltage vectors. This method decreases harmonic components of the phase current, harmonic losses of the motor and torque ripple, and achieves high voltage utilization.

SVPWM generates pulse-width modulation signals for the three-phase motor voltage control, whose process can be reduced to a few simple equations. Since high side and low side of the three-phase inverter cannot be turned on simultaneously, there are two states for a phase, i.e., phase connected to bus voltage (+) or phase connected to ground (-). Therefore, voltage vector output of the inverter has a total of $2^3 = 8$ possible states. When all three phases are connected to bus voltage (+) or ground (-), no voltage drop exists between two phases and the two states are called inactive state or zero voltage vector. The other six states which have voltage output are active voltage vectors with an adjacent state rotation offset of 60 degrees.

Figure 15-5 SVPWM Voltage Vector



SVPWM uses the sum of two adjacent vectors to generate any voltage vector located in the voltage vector space. U_{OUT} is the desired vector and it is in the sector between U60 and U0. In defined PWM cycle (T), the effect, U0 applied 2T1/T time and U60 applied 2T2/T time, is equivalent to the U_{OUT}. The rest of time (T0) is applied by zero voltage vector.

Figure 15-6 SVPWM Voltage Vector Synthesis

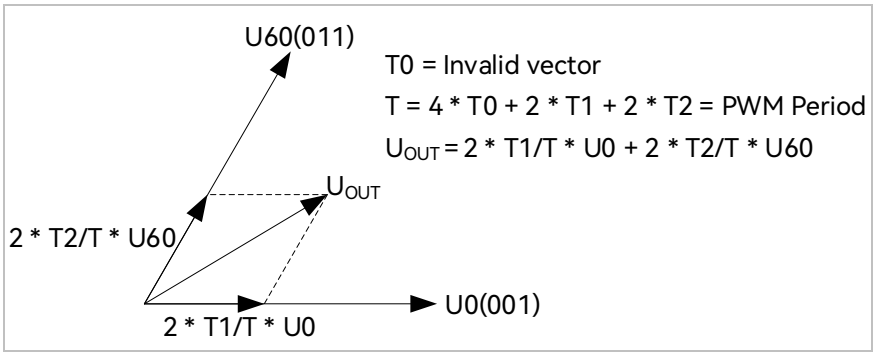


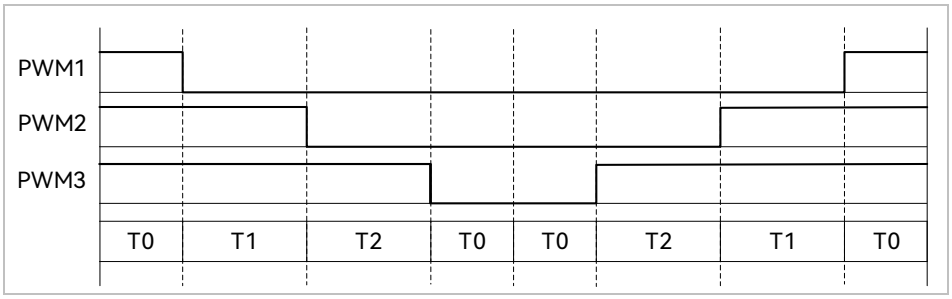
Table 15-1 States of SVPWM Inverter

Phase C	Phase B	Phase A	V_{ab}	V_{bc}	V_{ca}	V_{ds}	V_{qs}	Vector
0	0	0	0	0	0	0	0	U(000)
0	0	1	V_{DC}	0	$-V_{DC}$	$2/3V_{DC}$	0	U0
0	1	1	0	V_{DC}	$-V_{DC}$	$1/3V_{DC}$	$1/3V_{DC}$	U60
0	1	0	$-V_{DC}$	V_{DC}	0	$-1/3V_{DC}$	$1/3V_{DC}$	U120
1	1	0	$-V_{DC}$	0	V_{DC}	$-2/3V_{DC}$	0	U180
1	0	0	0	$-V_{DC}$	V_{DC}	$-1/3V_{DC}$	$-1/3V_{DC}$	U240
1	0	1	V_{DC}	$-V_{DC}$	0	$1/3V_{DC}$	$-1/3V_{DC}$	U300
1	1	1	0	0	0	0	0	U(111)

15.1.5.1 Continuous SVPWM

In single-shunt current sampling mode, continuous SVPWM is always used. In dual-shunt current sampling mode, FOC_CR2[F5SEG] is set to “0” to select continuous SVPWM as the output mode.

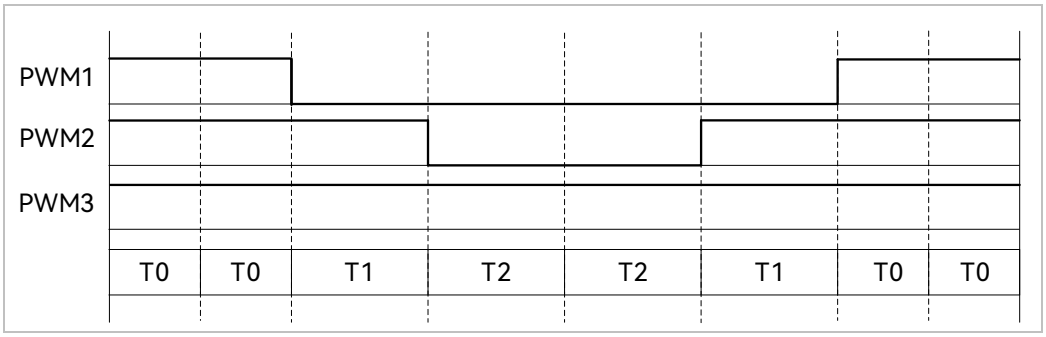
Figure 15-7 Output Level of Continuous SVPWM



15.1.5.2 Discontinuous SVPWM

Discontinuous SVPWM is available in dual/triple-shunt current sampling mode. FOC_CR2[F5SEG] is set to “1” to activate this mode.

Figure 15-8 Output Level of Discontinuous SVPWM



15.1.6 Overmodulation

Overmodulation is available in single/dual/triple-shunt current sampling mode. FOC_CR1[OVMDL] is set to "1" to enable overmodulation feature. The voltage output, FOC_UD, FOC_UQ and related limit amplitudes (MAX/MIN) are multiplied by 1.15 in this mode.

15.1.7 Deadtime Compensation

Deadtime compensation is available in dual/triple-shunt current sampling mode. This mode improves sinusoidal waveform of the current at low-speed.

15.1.8 Current and Voltage Sampling

In FOC mode, bus voltage and phase current are sampled by hardware automatically. Before FOC module operates, ADC and operational amplifier shall be enabled and the corresponding control registers be configured. No configuration is required for ADC channel and scan mode. Single/dual/triple-shunt current sampling mode is selected by setting FOC_CR1[CSM]. In single-shunt current sampling mode, channel 4 is the default sampling channel of the bus current (itrip). In dual-shunt current sampling mode, channel 0 and channel 1 are the default sampling channels of A-phase current (ia) and B-phase current (ib) respectively. In triple-shunt current sampling mode, channel 0, channel 1 and channel 4 are the default sampling channels of ia, ib and C-phase current (ic) respectively. Channel 2 is used for bus voltage sampling.

15.1.8.1 Single-shunt Current Sampling Mode

FOC_CR1[CSM] is set to "00" to select the single-shunt current sampling mode. In this mode, FOC module samples itrip (channel 4) twice during the Driver timer counting-up operation, and samples bus voltage during the Driver timer counting-down operation and after FOC module completes the calculation.

Since deadtime affects the accuracy of current sampling, FOC module samples within T1' and T2', which is the applied time of active voltage vector with deadtime removed. FOC_TRGDLY is the register which advances or delays the current sampling time, and this register shall be configured reasonably to ensure sampling is completed within T1' and T2'. For example, when MCU clock rate = 24MHz(41.67ns) and FOC_TRGDLY = 5, the sampling time is delayed by 41.67*5 = 208ns; and when FOC_TRGDLY = 0xFB(−5), the sampling time is advanced by 208ns.

Figure 15-9 Single-shunt Current Sampling Timing

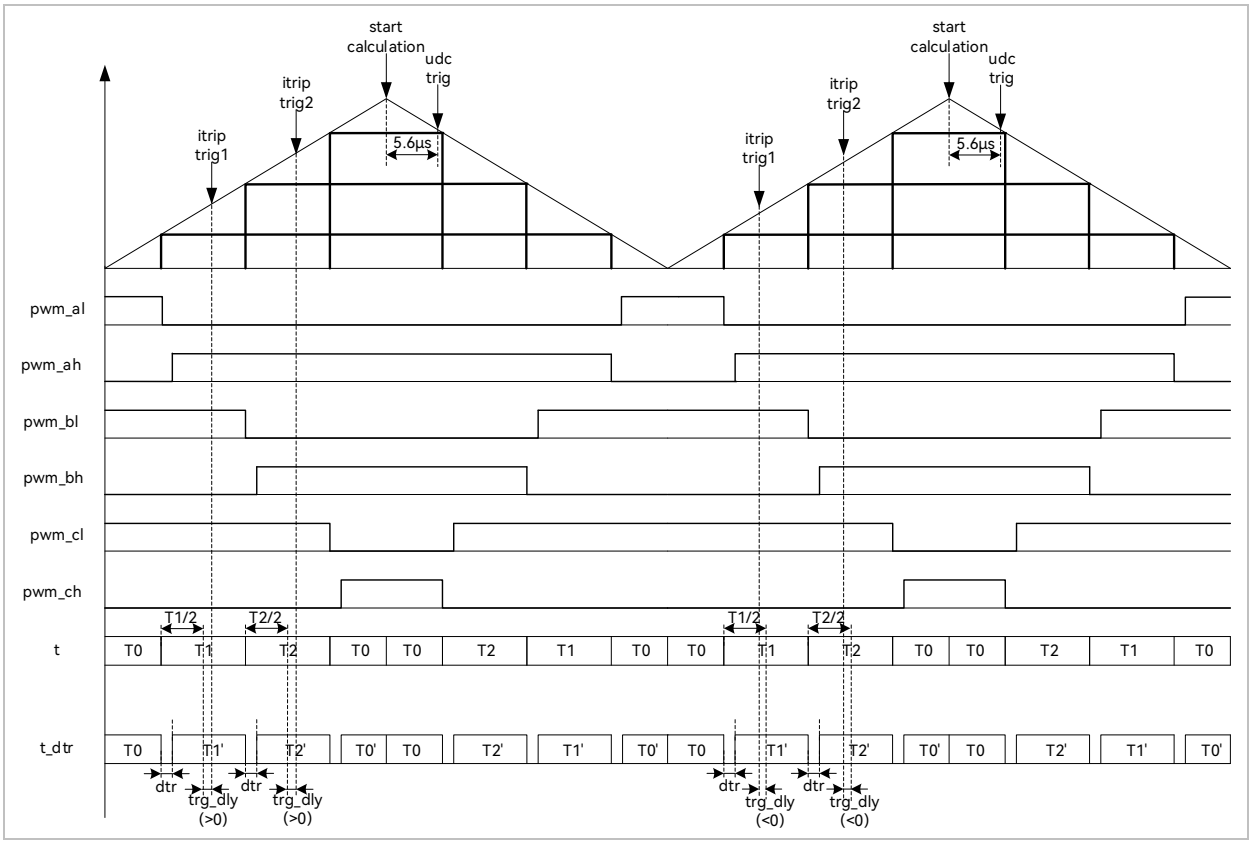
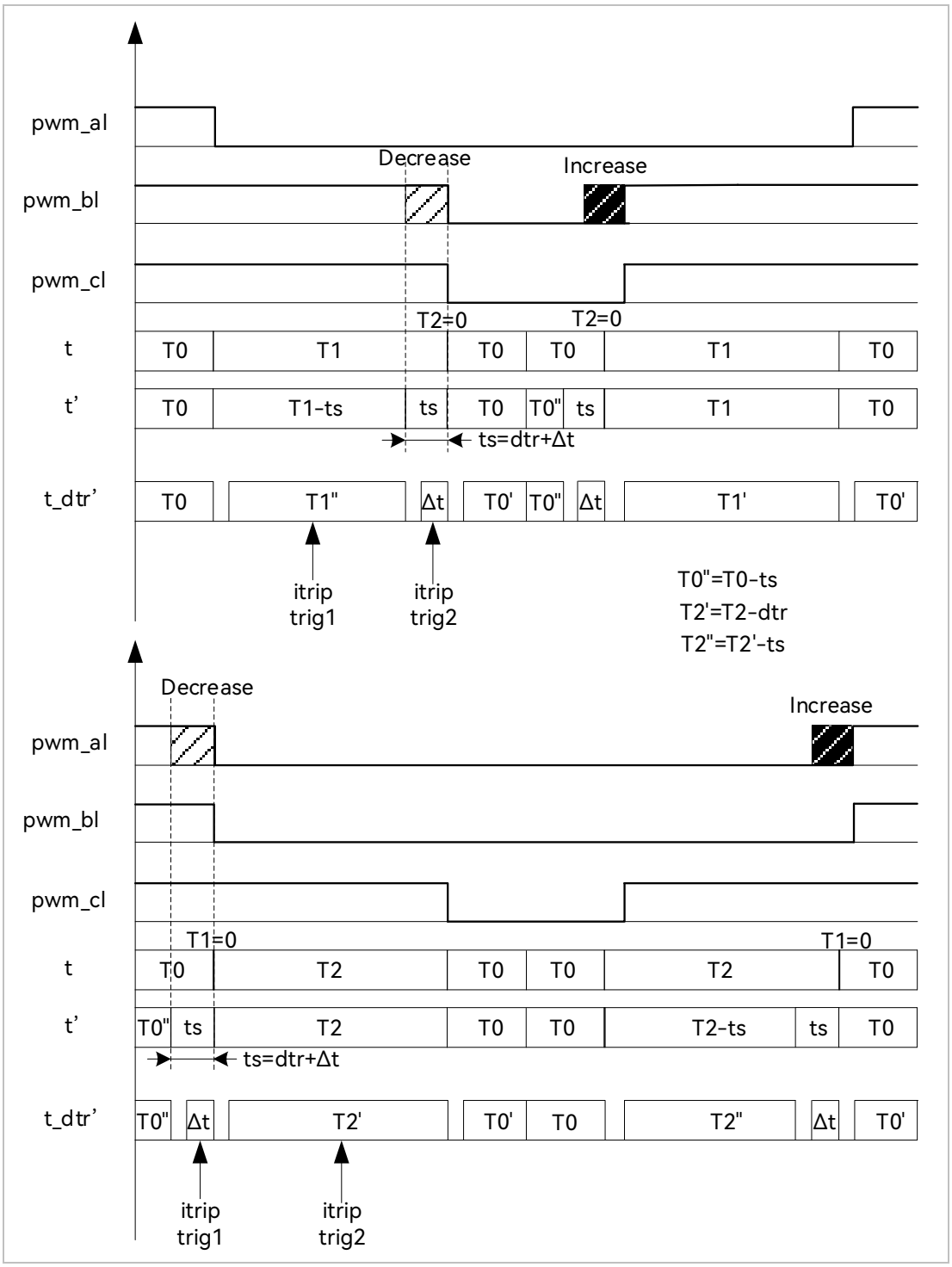


Figure 15-10 Single-shunt Current Sampling Time Compensation

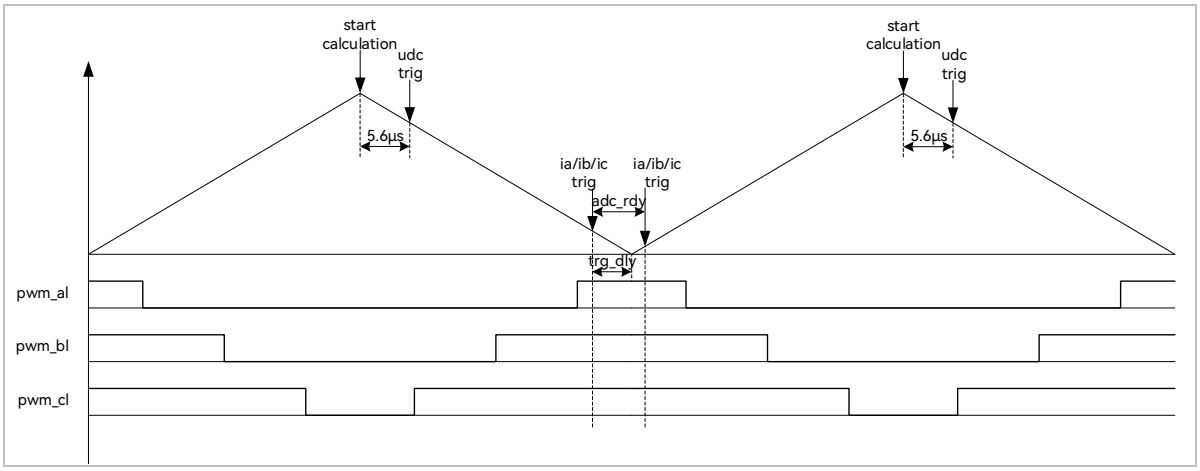


The time of single-shunt current sampling window may be not enough to sample the current in low modulation index and sector switching area. PWM waveform shall be adjusted to ensure the minimum sampling window required in the case. FOC_TSMIN (FOC_TSMIN = minimum sampling window + deadtime)

is used to configure the compensation value of deadtime, and FOC module adjusts the PWM waveform automatically.

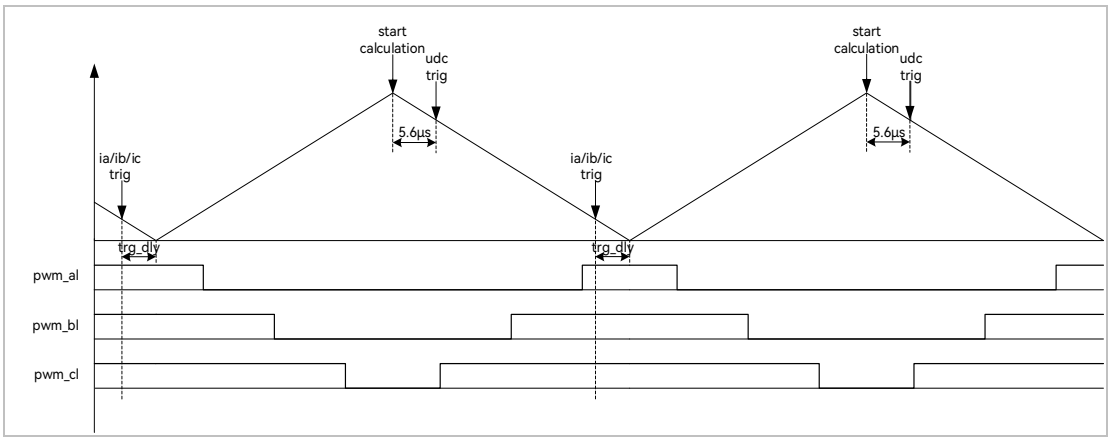
15.1.8.2 Dual/Triple-shunt Current Sampling Mode

Figure 15-11 Dual/Triple-shunt Sequential Current Sampling Mode



FOC_CR1[CSM] is set to “10/11” and FOC_CR2[DSS] to “0” to select dual/triple-shunt sequential current sampling mode. FOC_TRGDLY is used to configure the sampling time of a phase current (ia/ib/ic is determined according to the sector), and other phases are sampled at the end of previous sampling. The bus voltage is sampled during the timer counting-down operation and after FOC module completes the calculation. FOC_TRGDLY shall be configured reasonably to ensure current sampling time is within zero voltage vector (i.e. pwm_al,pwm_bl, pwm_cl = 111). For example, when MCU clock rate = 24MHz(41.67ns), FOC_TRGDLY = 0xB2 and FOC timer counts down, ia/ib/ic is sampled at 41.67*50 = 2.08μs before an underflow event, and then the other phases of ia/ib/ic are sampled.

Figure 15-12 Dual/Triple-shunt Alternate Current Sampling Mode



FOC_CR1[CSM] is set to “10/11” and FOC_CR2[DSS] to “1” to select dual/triple-shunt alternating current sampling mode. In this mode, FOC module performs calculation in every PWM cycle. However, only one phase current is sampled at each PWM cycle (ia/ib/ic is determined according to the sector). The first carrier cycle samples one phase of the ia/ib/ic, and the second carrier cycle samples the current of the other phase, so as to alternately sample the current of two phases in three phases. FOC_TRGDLY is used to configure the sampling time of ia (channel 0), ib (channel 1) and ic (channel 4). FOC_TRGDLY shall be configured reasonably to ensure sampling time for the ia/ib/ic current is within zero voltage vector (i.e. pwm_al,pwm_bl,pwm_cl = 111). For example, when MCU clock rate = 24MHz(41.67ns), FOC_TRGDLY = 0xB2 and FOC timer counts down, phase current is sampled at 41.67*50 = 2.08μs before an underflow event.

15.1.8.3 Current Sampling Offset

The current sampling offset voltage shall be added to sample full range of current due to the existence of the positive and negative phase current. When phase current is 0, ADC result is the offset value. ADC result minus this value, 0x4000 by default, is the sampling current. Since ADC reference voltage and hardware are nonideal, there is a deviation between the default value and the real value. Therefore, it is necessary to calibrate the offset. The calibration procedure is as follows. When FOC module does not work and there is no current in three phases, MCU starts to sample the corresponding channel several times, averages all the sampled value, and writes the averaged value to FOC_CSO. Providing ADC sampling range is 0 ~ 5V and the reference is 2.5V, FOC_CSO = 2.5V/5V*32768= 16384 (0x4000).

- When FOC_CR2[CSOC] = 00/11, FOC_CSO is written to modify the offset of itrip and ic.
- When FOC_CR2[CSOC] = 01, FOC_CSO is written to modify the offset of ia.
- When FOC_CR2[CSOC] = 10, FOC_CSO is written to modify the offset of ib.

15.1.9 Angle Mode

Angle module includes angle estimation module, ramping module and estimated angle smooth switching module. The sources of angle are as follows:

- Forced ramping angle
- Forced pulling angle

- Estimated angle of estimator
- Forced angle of estimator

Table 15-2 Sources of Angle

FOC_CR1[RFAE]	FOC_CR1[ANGM]	FOC_CR1[EFAE]	Source
1	X	X	Forced ramping angle
0	0	X	Forced pulling angle
0	1	0	Estimated angle of estimator
0	1	1	- omega > FOC_EFREQMIN: Estimated angle of estimator - omega < FOC_EFREQMIN: Forced angle of estimator

15.1.9.1 Forced Ramping Angle

Forced ramping angle is controlled by angle register FOC_THETA, speed register FOC_RTHESTEP, acceleration register FOC_RTHEACC and ramping counter FOC_RTHECNT. The formula is:

FOC_RTHESTEP(32 bits) = FOC_RTHESTEP(32 bits) + FOC_RTHEACC(32 bits, 16 high-order bits are always 0 and 16 low-order bits are configurable)

THETA_OL(16 bits) = FOC_THETA_OL(16 bits) + FOC_RTHESTEP(16 high-order bits)

Forced ramping angle has the highest priority. Configuring FOC_CR1[RFAE] to “1” enables the ramping feature. Ramping module makes a ramping operation in every PWM cycle and the counter is added by 1. When the value of the counter reaches the set value by FOC_RTHECNT, FOC_CR1[RFAE] is cleared by hardware, and then the ramping is completed. Thereafter, according to the value of FOC_CR1[ANGM], the angle comes from estimator (FOC_CR1[ANGM] = 1) or forced pulling angle (FOC_CR1[ANGM] = 0).

15.1.9.2 Forced Pulling Angle

Forced pulling angle is controlled by angle FOC_THETA and speed FOC_RTHESTEP.

The formula is: THETA_OL(16 bits) = THETA_OL(16 bits) + FOC_RTHESTEP(16 high-order bits)

There are two scenarios for forced pulling angle.

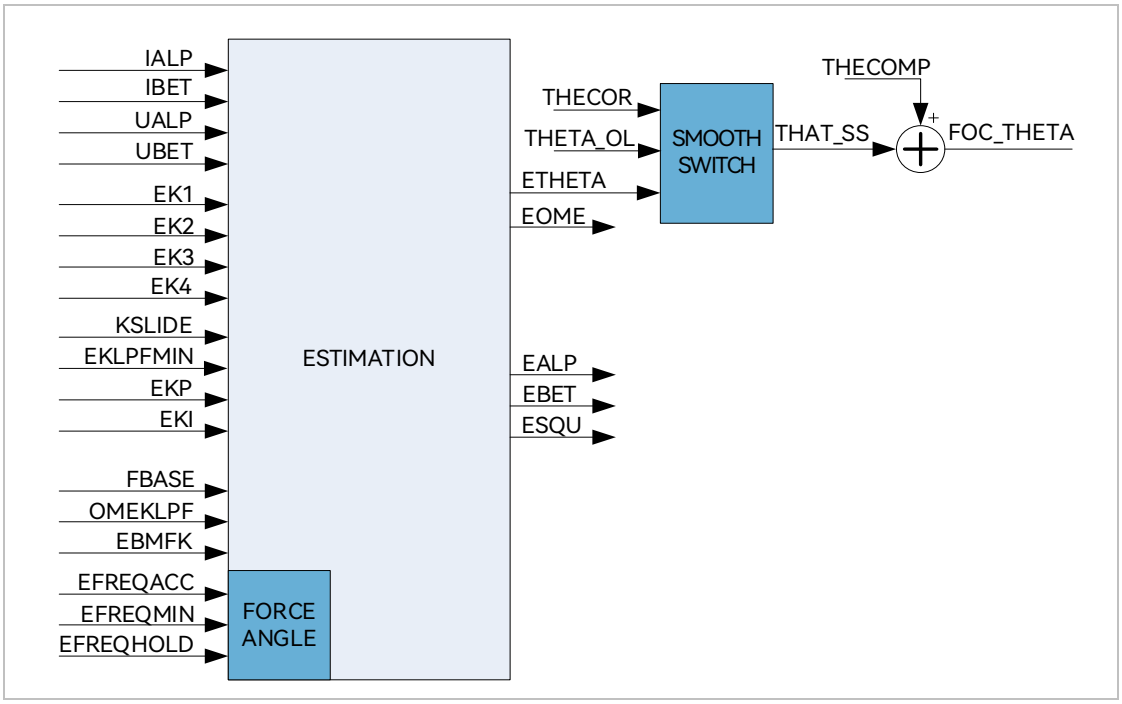
- When FOC_CR1[RFAE] is set to “1” and FOC_CR1[ANGM] to “0”, MCU switches to forced pulling angle mode after forced ramping angle mode. The speed is the cumulative result after ramp force angle

mode. This mode implements a forced uniform speed control.

- When FOC_CR1[RFAE] is set to “0” and FOC_CR1[ANGM] to “0”, the angle is the forced pulling angle and the speed FOC_RTHESTEP is the initial speed written by software. Configuring FOC_RTHESTEP = 0 enables the pre-position feature. Configuring FOC_RTHESTEP != 0 implements Hall-based FOC (Principle of Hall-based FOC: MCU calculates the angle and speed based on the received Hall signals, and writes them to FOC_THETA and FOC_RTHESTEP for calibration).

15.1.9.3 Estimator Output Angle

Figure 15-13 Schematic Block Diagram of Estimator



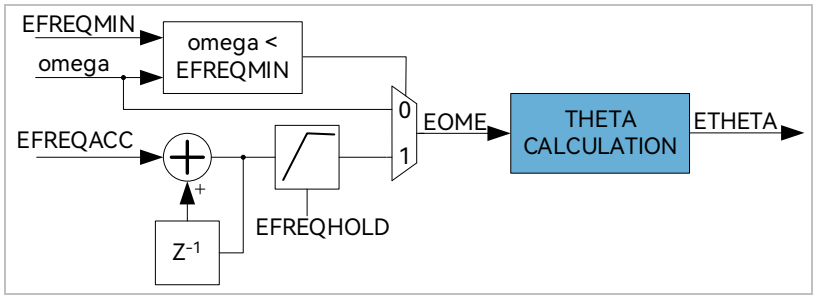
The estimator collects the motor current and voltage and outputs the angle, speed and BEMF based on user-defined motor parameters and other control parameters.

15.1.9.3.1 Estimated Angle of Estimator

The estimator builds the motor model based on the motor parameters and control parameters, and outputs the estimated angle based on the sampled current and voltage. The estimator works in PLL mode or SMO mode by configuring the FOC_CR2[ESEL].

15.1.9.3.2 Forced Angle of Estimator

Figure 15-14 Schematic Diagram of Forced Angle of Estimator

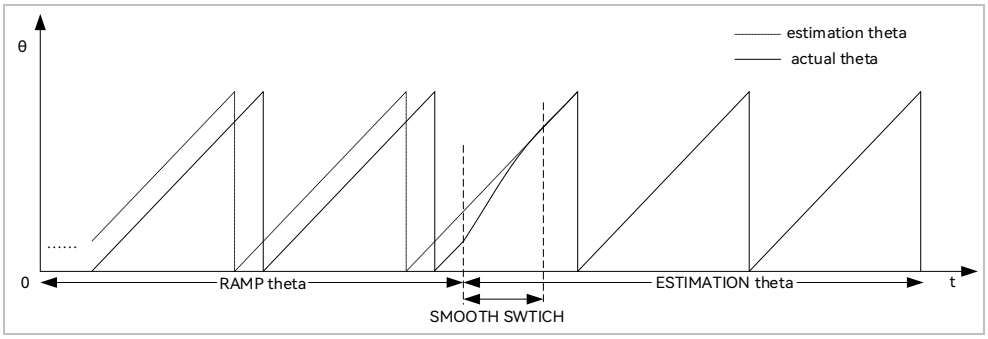


This feature is similar to the ramping feature. Due to the low speed at motor starting process, there may be a deviation in angle and speed estimation with the small effective signal, resulting in startup failure. In this case, the estimator outputs the forced angle to ensure the motor start normally.

When FOC_CR1[EFAE] = 1, if omega < FOC_EFREQMIN, the forced speed is selected as EOME. The forced speed starts with 0 and increases by FOC_EFREQACC in each PWM cycle, with the maximum value FOC_EFREQHOLD. When omega ≥ FOC_EFREQMIN, omega is selected as EOME.

15.1.9.3.3 Angle Smooth Switching

Figure 15-15 Angle Smooth Switching Curve



When FOC_CR1[RFAE] is set to “1” and FOC_CR1[ANGM] to “1”, the motor starts with ramping feature, and it switches to estimator angle mode after the ramping. However, there is usually a deviation between the estimated angle (FOC_ETHETA) and the forced ramping angle (THETA_OL). If the angle is switched from forced ramping angle to estimated angle directly, motor jitter may occur due to such a sudden change. To deal with this problem, a smooth switching is preferred.

After ramping, if the deviation between FOC__ETHETA and THETA_OL is less than or equal to FOC_THECOR, FOC__ETHETA is selected as the output angle. But if the deviation is larger than FOC_THECOR, THETA_OL is modified smoothly with the step of FOC_THECOR at every PWM cycle until it is close to FOC__ETHETA. After the deviation is less than FOC_THECOR, FOC__ETHETA is selected as the output angle.

15.1.9.3.4 Angle Compensation

Angle compensation value FOC_THECOMP is used to compensate for the estimated angle FOC_ETHETA. If FOC_THECOMP is negative (MSB is 1), the lag angle is compensated; if it is positive (MSB is 0), the lead angle is compensated.

15.1.10 Motor Real-time Parameters

MCU monitors the state of motor using the following real time variables provided by FOC module:

- Used angle FOC_THETA
- Estimated angle FOC_ETHETA and estimated speed FOC_EOME
- d-axis voltage FOC_UD and q-axis voltage FOC_UQ
- d-axis current FOC_ID and q-axis current FOC_IQ
- α-axis voltage FOC_VALP and β-axis voltage FOC_VBET
- Bus voltage FOC_UDCFLT
- Phase current FOC_IA, FOC_IB, FOC_IC and maximum phase current FOC_IAMAX, FOC_IBMAX, FOC_ICMAX
- α-axis current (equal to FOC_IA) and β-axis current FOC_IBET
- α-axis BEMF FOC_EALP and β-axis BEMF FOC_EBET
- Square of BEMF FOC_ESQU
- Magnitude of BEMF FOC_EMF
- Motor power FOC_POW

15.1.10.1 Tailwind/Headwind Detection

FOC module provides tailwind/headwind detection feature. FOC module starts to operate when FOC_CR3[ESCMS] is set to “1”, FOC_IDREF to “0” and FOC_IQREF to “0”. Motor’s rotor state is detected by FOC_ETHETA and FOC_EOME. If FOC_ETHETA decreases or FOC_EOME is a negative value, the motor rotates in the headwind state and it is necessary to brake first and then start the motor with ramping forced angle mode. If FOC_ETHETA increases or FOC_EOME is a positive value, the motor rotates in the

tailwind state and starts using estimated angle directly.

15.1.10.2 BEMF Detection

Estimator estimates α-axis BEMF FOC_EALP and β-axis BEMF FOC_EBET with the motor parameters, and calculates FOC_ESQU ($e\alpha^2 + e\beta^2$) to implement protection features, such as motor lock protection, phase loss protection, etc.

15.1.10.3 Motor Power

FOC module calculates motor power based on the sampling current, modulation index of SVPWM and filtered bus voltage.

15.1.11 FG Generation

FG signal is generated by FOC module and Timer4. FOC module calculates an FG result based on frequency base fbase FOC_FBASE, low-pass filtered speed FOC_EOMELPF and FG coefficient FOC_KFG in every PWM cycle. The result is updated to TIM4_ARR automatically and half of the result (TIM4_ARR/2) to TIM4_DR by hardware. It shall be noted that Timer4 must work in output mode and the clock division factor of Timer4 shall be configured properly.

FOC_KFG is computed by the following algorithm:

FOC_KFG = $24MHz/(2\text{^}T4PSC * FBASE * x)$

Where, x refers to the expected number of FG signal in one electric cycle.

If the result exceeds 65535, the clock division factor TIM4_CR0[T4PSC] shall be adjusted.

When FOC_KFG = 0, this feature is disabled, and TIM4_ARR and TIM4_DR keeps unchanged.

15.2 FOC Registers

15.2.1 FOC_CR1 (0x40A0)

Bit	7	6	5	4	3	2	1	0
Name	OVMDL	EFAE	RFAE	ANGM	CSM		RSV	SVPWMEN
Type	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W
Reset	0	0	0	0	0	0	-	0

Bit	Name	Description
[7]	OVMDL	Overmodulation Enable 0: Disable 1: Enable
[6]	EFAE	Forced Angle of Estimator Enable When this feature is enabled, angle mode is determined by the estimator and switches to estimated angle mode automatically. 0: Disable 1: Enable
[5]	RFAE	Forced Ramping Angle Enable When this feature is enabled, angle mode is determined by the ramping module. After ramping, it switches to estimated mode or forced pulling mode according to FOC_CR1[ANGM]. FOC_CR1[RFAE] is cleared to “0” by hardware as well. 0: Disable 1: Enable
[4]	ANGM	Angle Mode When FOC_CR1[RFAE] = 0, angle mode is determined by this bit. When FOC_CR1[RFAE] = 1, angle mode is determined by this bit after ramping. 0: Forced Pulling Angle Mode 1: Estimated Angle of Estimator Mode
[3:2]	CSM	Current Sampling Mode 00: Single-shunt Current Sampling 01: Dual-shunt Current Sampling 10: Reserved 11: Triple-shunt Current Sampling
[1]	RSV	Reserved
[0]	SVPWMEN	SVPWM Module Enable 0: Disable 1: Enable

15.2.2 FOC_CR2 (0x40A1)

Bit	7	6	5	4	3	2	1	0
Name	ESEL	RSV	F5SEG	DSS	CSOC		UQD	UDD
Type	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	-	0	0	0	0	0	0

Bit	Name	Description
[7]	ESEL	Angle Estimator Mode Selection 0: SMO 1: PLL (phase-locked loop). FOC_KSILDE register works as KP of PI controller, and FOC_KLPFMIN register as KI of PI controller
[6]	RSV	Reserved
[5]	F5SEG	SVPWM Mode Selection 0: Continuous SVPWM 1: Discontinuous SVPWM (cannot be selected in single-shunt current sampling mode)
[4]	DSS	Dual/Triple-shunt Current Sampling Mode 0: Sequential Sampling Mode, where two-phase currents are sampled in each carrier period 1: Alternate Sampling Mode. FOC module completes the calculation in every carrier cycle. Two-phase currents are sampled alternately in two adjacent carrier cycles.
[3:2]	CSOC	Current Sampling Offset Calibration This bit is written to select the offset of FOC_CSO. In single-shunt sampling, “00” or “11” is written to calibrate itrip offset. In dual-shunt sampling, “01” is written to calibrate ia offset and “10” to calibrate ib offset. In triple-shunt sampling, “01” is written to calibrate ia offset, “10” to calibrate ib offset and “00” or “11” to calibrate ic offset. 00,11: itrip and ic 01: ia 10: ib
[1]	UQD	q-axis PI Controller Disable When it is enabled, FOC_UQ value is no longer updated by the PI controller. 0: Disable 1: Enable
[0]	UDD	d-axis PI Controller Disable When it is enabled, FOC_UD value is no longer updated by the PI controller. 0: Disable 1: Enable

15.2.3 FOC_TSMIN (0x40A2)

Bit	7	6	5	4	3	2	1	0
Name	FOC_TSMIN							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	FOC_TSMIN	Single-shunt Current Sampling Mode: minimum window for ADC sampling Dual/triple-shunt Current Sampling Mode: deadtime compensation Range [0, 255] TSMIN = sampling window $\triangle T_{window}$ + deadtime T_{DT} Example: Assuming that $\triangle T_{window}$ = 1μs, T_{DT} = 1μs, TSMIN = 2μs and carrier period = 62.5μs, then FOC_TSMIN = (1 + 1)/62.5*4096 = 131.

15.2.4 FOC_TGLI (0x40A3)

Bit	7	6	5	4	3	2	1	0
Name	FOC_TGLI							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	FOC_TGLI	Narrow Pulse Elimination for High Side This feature is designed for high-voltage applications. The minimum pulse required by high side of the driver must be longer than a certain time. The pre-driver is not turned on if the pulse is less than the value set by this bit. Range [0,255] Example: Assuming that it is required to remove narrow pulses with less than 1μs width, deadtime DT = 1μs, and carrier period = 62.5μs, then FOC_TGLI = 2/62.5*4096 = 131.

15.2.5 FOC_TBLO (0x40A4)

Bit	7	6	5	4	3	2	1	0
Name	FOC_TBLO							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	FOC_TBLO	Sampling Masking Time in Triple-shunt Current Sampling Mode If the low side is turned on for less than FOC_TBLO, the phase current is not sampled and obtained through special process.

		Range [0, 255] Example: Assuming that the phase current is not sampled if the low side is turned on for less than 1μs, then FOC_TBLO = 1000/41.67 = 24.

15.2.6 FOC_TRGDLY (0x40A5)

Bit	7	6	5	4	3	2	1	0
Name	FOC_TRGDLY							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	FOC_TRGDLY	Single-shunt Current Sampling Mode: Trigger Delay for ADC Current Sampling Range [-128,127] Dual/Triple-shunt Current Sampling Mode: Time for Current Sampling TRGDLY[7] decides the sampling occurs in falling or rising interval of the timer: TRGDLY[7] = 0: rising interval; TRGDLY[7] = 1: falling interval Range (0, DRV_ARR[6:0]) Single-shunt Current Sampling Mode: If FOC_TRGDLY = 5, it delays by 5*T = 208ns to sample the current, and if FOC_TRGDLY = 0xFB (complement) or FOC_TRGDLY = -5, it advances by 5*T=208ns. Dual-shunt/Triple-shunt Current Sampling Mode: If FOC_TRGDLY = 0x85 (the highest bit, and the remaining 7 bits are absolute values) and Driver timer counts down, it samples the current at 5*T = 208ns before an overflow event occurs. If FOC_TRGDLY = 5 and Driver timer counts up, it samples the current at 5*T = 208ns after an overflow event occurs.

15.2.7 FOC_CSO (0x40A6, 0x40A7)

FOC_CSOH(0x40A6)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_CSO[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0
FOC_CSOL(0x40A7)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_CSO[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description

[15:0]	FOC_CSO	Current Sampling Offset FOC_CR2[CSOC] is configured to select the current, and FOC_CSO is written to calibrate current sampling offset of itrip in single-shunt current sampling mode, ia, ib in dual-shunt current sampling mode and ia, ib and ic in triple-shunt current sampling mode. Range [0,32767]; MSB is always 0 Example: Assuming that ADC voltage falls within 0V ~ 5V with a reference value of 2.5V, then FOC_CSO = 2.5V/5V*32768 = 16384 (0x4000)

15.2.8 FOC_RTHESTEP (0x40A8, 0x40A9)

FOC_RTHESTEPH(0x40A8)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_RTHESTEP[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_RTHESTEPL(0x40A9)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_RTHESTEP[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_RTHESTEP	Speed of Ramping Module The format is the same as that of FOC_THETA. FOC_RTHESTEP is an internal 32-bit register with the most significant bit (MSB) serving as the sign bit. 16 high-order bits are written by software. Range [-32768,32767] FOC_RTHESTEP (32 bits) = FOC_RTHESTEP (32 bits) + FOC_RTHEACC 16 low-order bits) THETA_OL (16 bits) = THETA_OL (16 bits) + FOC_RTHESTEP (16 high-order bits)

15.2.9 FOC_RTHEACC (0x40AA, 0x40AB)

FOC_RTHEACCH(0x40AA)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_RTHEACC[15:8]							
Type	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
FOC_RTHEACCL(0x40AB)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_RTHEACC[7:0]							
Type	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_RTHEACC	Ramping Acceleration FOC_RTHEACC is an internal 32-bit variable. MSB is sign bit. 16 low-order bits are written by software and 16 high-order bits are constantly 0. Range [-32768,32767] Note > FOC_STEP (32 bits) = FOC_RTHESTEP (32 bits) + FOC_RTHEACC (16 low-order) > THETA_OL (16 bits) = THETA_OL (16 bits) + FOC_RTHESTEP (16 high-order bits)

15.2.10 FOC_RTHECNT (0x40AC)

Bit	7	6	5	4	3	2	1	0
Name	FOC_RTHECNT							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	FOC_RTHECNT	Range [0,255] Max. ramping counts = FOC_RTHECNT*256 When ramping feature is enabled (FOC_CR1[RFAE] = 1), the ramping calculation is performed in each carrier cycle. After FOC_RTHECNT*256 times, the ramping feature is disabled.

15.2.11 FOC_THECOR (0x40AD) (Shared with BLDC Control)

Bit	7	6	5	4	3	2	1	0
Name	FOC_THECOR							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bit	Name	Description
[7:0]	FOC_THECOR	Angle Smooth Switching Correction The step value of angle smooth switching after ramping. The format is the same as FOC_THETA. Range [0,255]

15.2.12 FOC_THECOMP (0x40AE, 0x40AF)

FOC_THECOMPH(0x40AE)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_THECOMP[15:8]							
Type	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
FOC_THECOMPL(0x40AF)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_THECOMP[7:0]							
Type	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_THECOMP	Angle Compensation Value The output angle FOC_THETA is derived from the estimator estimated angle + compensation value. The format is same as that of FOC_THETA. Range [-32768,32767]

15.2.13 FOC_DMAX (0x40B0, 0x40B1)

FOC_DMAXH(0x40B0)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_DMAX[15:8]							
Type	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
FOC_DMAXL(0x40B1)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_DMAX[7:0]							
Type	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_DMAX	Max. output of d-axis PI controller Range [-32768,32767]

15.2.14 FOC_DMIN (0x40B2, 0x40B3)

FOC_DMINH(0x40B2)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_DMIN[15:8]							
Type	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
FOC_DMINL(0x40B3)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_DMIN[7:0]							
Type	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_DMIN	Min. output of d-axis PI controller Range [-32768,32767]

15.2.15 FOC_QMAX (0x40B4, 0x40B5)

FOC_QMAXH(0x40B4)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_QMAX[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_QMAXL(0x40B5)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_QMAX[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_QMAX	Max. output of q-axis PI controller Range [-32768,32767]

15.2.16 FOC_QMIN (0x40B6, 0x40B7)

FOC_QMINH(0x40B6)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_QMIN[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_QMINL(0x40B7)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_QMIN[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_QMIN	Min. output of q-axis PI controller Range [-32768,32767]

15.2.17 FOC_UD (0x40B8, 0x40B9)

FOC_UDH(0x40B8)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_UD[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_UDL(0x40B9)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_UD[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_UD	d-axis voltage calculated by d-axis PI controller Range [-32768,32767]

15.2.18 FOC_UQ (0x40BA, 0x40BB)

FOC_UQH(0x40BA)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_UQ[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_UQL(0x40BB)								
Bit	7	6	5	4	3	2	1	0

Name	FOC_UQ[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_UQ	q-axis voltage calculated by q-axis PI controller Range [-32768,32767]

15.2.19 FOC_ID (0x40BC, 0x40BD)

FOC_IDH(0x40BC)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_ID[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_IDL(0x40BD)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_ID[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_ID	d-axis current obtained after coordinate transformation of the sampled current Range [-32768,32767]

15.2.20 FOC_IQ (0x40BE, 0x40BF)

FOC_IQH(0x40BE)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_IQ[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_IQL(0x40BF)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_IQ[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_IQ	q-axis current obtained after coordinate transformation of the sampled current Range [-32768,32767]

15.2.21 FOC_IBET (0x40C0, 0x40C1)

FOC_IBETH(0x40C0)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_IBET[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_IBETL(0x40C1)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_IBET[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_IBET	β-axis current obtained after coordinate transformation of the sampled current Range [-32768,32767]

15.2.22 FOC_VBET (0x40C2, 0x40C3)

FOC_VBETH(0x40C2)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_VBET[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_VBETL(0x40C3)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_VBET[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_VBET	β-axis Voltage Outputed by FOC Module Range [-32768,32767]

15.2.23 FOC_VALP (0x40C4, 0x40C5)

FOC_VALPH(0x40C4)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_VALP[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_VALPL(0x40C5)								

Bit	7	6	5	4	3	2	1	0
Name	FOC_VALP[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_VALP	α-axis Voltage Outputed by FOC Module Range [-32768,32767]

15.2.24 FOC_IC (0x40C6, 0x40C7)

FOC_ICH(0x40C6)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_IC[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_ICL(0x40C7)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_IC[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_IC	Sampled Phase-C Current Range [-32768,32767]

15.2.25 FOC_IB (0x40C8, 0x40C9)

FOC_IBH(0x40C8)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_IB[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_IBL(0x40C9)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_IB[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_IB	Sampled Phase-B Current Range [-32768,32767]

15.2.26 FOC_IA (0x40CA, 0x40CB)

FOC_IAH(0x40CA)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_IA[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_IAL(0x40CB)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_IA[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_IA	Sampled Phase-A Current Range [-32768,32767]

15.2.27 FOC_THETA (0x40CC, 0x40CD)

FOC_THETAH(0x40CC)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_THETA[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_THETAL(0x40CD)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_THETA[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_THETA	FOC Output Angle Range [-32768,32767] The bit value -32768 ~ 32767 corresponds to angle range -180°~ 180°. Example: Assuming that THETA = 8192, the output angle is 8192/32768 *180°= 45°.

15.2.28 FOC_ETHETA (0x40CE, 0x40CF)

FOC_ETHETAH(0x40CE)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_ETHETA[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_ETHETAL(0x40CF)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_ETHETA[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_ETHETA	Read: Output Angle of Estimator (angle before FOC_THECOMP is applied); the format is same as that of FOC_THETA. Write: Initial Angle of Estimator Range [-32768,32767]

15.2.29 FOC_EALP (0x40D0, 0x40D1)

FOC_EALPH(0x40D0)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EALP[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_EALPL(0x40D1)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EALP[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EALP	α-axis BEMF by Estimator Range [-32768,32767]

15.2.30 FOC_EBET (0x40D2, 0x40D3)

FOC_EBETH(0x40D2)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EBET[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

FOC_EBETL(0x40D3)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EBET[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EBET	β-axis BEMF by Estimator Range [-32768,32767]

15.2.31 FOC_EOME (0x40D4, 0x40D5)

FOC_EOMEH(0x40D4)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EOME[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_EOMEL(0x40D5)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EOME[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EOME	Output Speed OMEGA of Estimator Range [-32768,32767]

15.2.32 FOC_ESQU (0x40D6, 0x40D7)

FOC_ESQUH(0x40D6)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_ESQU[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_ESQUL(0x40D7)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_ESQU[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_ESQU	Square of EBETA + square of EALPHA. The result is obtained from 16 high-order bits, with MSB being always 0.

		Range [0,32767]

15.2.33 FOC_POW (0x40D8, 0x40D9)

FOC_POWH(0x40D8)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_POW[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_POWL(0x40D9)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_POW[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_POW	Motor Power Range [-32768,32767]; An error occurs if this value is negative.

15.2.34 FOC_EKP (0x4074, 0x4075) (Shared with BLDC Control)

FOC_EKPH(0x4074)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EKP[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_EKPL(0x4075)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EKP[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EKP	KP of PI Controller Used by the Estimator. MSB is always 0. Q12 format. Range [0,32767].

15.2.35 FOC_EKI (0x4076, 0x4077) (Shared with BLDC Control)

FOC_EKIH(0x4076)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EKI[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_EKIL(0x4077)								

Bit	7	6	5	4	3	2	1	0
Name	FOC_EKI[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EKI	KI of PI Controller Used by the Estimator. MSB is always 0. Q15 format. Range [0,32767]

15.2.36 FOC_EBMFK (0x407C, 0x407D) (Shared with BLDC Control)

FOC_EBMFKH(0x407C)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EBMFK[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_EBMFKL(0x407D)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EBMFK[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EBMFK	Coefficient used to calculate BEMF low-pass filter coefficient EKLPF. Q15 format. Range [0,32767]. EKLPF = FOC_EBMFK * FOC_OMEGA FOC_EBMFK = 2 * π * fbase*Ts

15.2.37 FOC_KSLIDE (0x4078, 0x4079) (Shared with BLDC Control)

FOC_KSLIDEH(0x4078)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_KSLIDE/FOC_PLLKP[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_KSLIDEL(0x4079)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_KSLIDE/FOC_PLLKP[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description

[15:0]	FOC_KSLIDE/FOC_PLLKP	FOC_CR2[ESEL] = 0: KSLIDE coefficient; Q15 format FOC_CR2[ESEL] = 1: KP of PI controller on PLL; Q12 format Range [0,32767]. MSB is always 0.

15.2.38 FOC_EKLPFMIN (0x407A, 0x407B) (Shared with BLDC Control)

FOC_EKLPFMINH(0x407A)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EKLPFMIN/FOC_ PLLKI[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_EKLPFMINL(0x407B)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EKLPFMIN/FOC_PLLKI[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EKLPFMIN/ FOC_PLLKI	FOC_CR2[ESEL] = 0: The minimum value of BEMF low pass filter factor. EKLPF is forced to be this value when it is lower than this value. Q15 format. FOC_CR2[ESEL] = 1: PI controller KI coefficient on PLL. Q15 format. Range [0,32767]; MSB is always 0.

15.2.39 FOC_OMEKLPF (0x407E, 0x407F)

FOC_OMEKLPFH(0x407E)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_OMEKLPF[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_OMEKLPFL(0x407F)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_OMEKLPF[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_OMEKLPF	LPF factor of estimated speed of the estimator. MSB is always 0. Q15 format. Range [0,32767].

15.2.40 FOC_FBASE (0x4080, 0x4081)

FOC_FBASEH(0x4080)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_FBASE[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_FBASEL(0x4081)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_FBASE[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_FBASE	Coefficient of angular increment DELTA THETA that is calculated based on OMEGA FBASE = fbase * △T * 32768 Assuming that fbase = 200Hz and △T = 62.5μs, then FBASE = 409

15.2.41 FOC_EFREQACC (0x4082, 0x4083) (Shared with BLDC Control)

FOC_EFREQACCH(0x4082)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EFREQACC[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_EFREQACCL(0x4083)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EFREQACC[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EFREQACC	Speed Increment of the Forced Angle Mode. FOC_EFREQACC is an internal 24-bit variable and MSB is sign bit. 16 low-order bits are written by software Range [0,65535] Example: Assuming that fbase = 200Hz and pp (Pole_Pairs) = 4, then speed_base = 60*fbase/pp = 3000rpm. If speed increment = 3rpm, then FOC_EFREQACC = 3rpm/speed_base*32768*256 = 8388(0x20C4).

15.2.42 FOC_EFREQMIN (0x4084, 0x4085) (Shared with BLDC Control)

FOC_EFREQMINH(0x4084)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EFREQMIN[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_EFREQMINL(0x4085)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EFREQMIN[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EFREQMIN	Threshold of Switching to Estimated Speed. FOC_EFREQMIN is an internal 24-bit variable, and MSB is sign bit. 16 high-order 16 bits are written by software. With Forced Angle of Estimator Mode enabled, FOC module outputs forced angle with value range [-32768,32767] when the estimated angle is smaller than the bit value. Example: Assuming that fbase = 200Hz and pp (Pole_Pairs) = 4, then speed_base = 60*fbase/pp = 3000rpm. Assuming that the minimum switching speed to esim,ator mode = 30rpm, then FOC_EFREQMIN = 30rpm/speed_base*32768 = 327(0x147).

15.2.43 FOC_EFREQHOLD (0x4086, 0x4087) (Shared with BLDC Control)

FOC_EFREQHOLDH(0x4086)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EFREQHOLD[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_EFREQHOLDL(0x4087)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EFREQHOLD[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EFREQHOLD	Maximum Estimated Forced Speed. FOC_EFREQHOLD is an internal 24-bit variable, and MSB is sign bit. 16 high-order bits are written by the software. When Omega rises to this value, it is kept unchanged.

		Range [-32768,32767] Example: Assuming that fbase = 200Hz and pp (Pole_Pairs) = 4, then speed_base = 60*fbase/pp = 3000rpm. If hold value of forced speed = 60rpm, then FOC_EFREQHOLD = 60rpm/speed_base*32768 = 655(0x28F).

15.2.44 FOC_EK3 (0x4088, 0x4089)

FOC_EK3H(0x4088)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EK3[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_EK3L(0x4089)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EK3[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EK3	The 3rd coefficient of the current model in estimator. MSB is always 0. Q15 format. Range [0, 32767]

15.2.45 FOC_EK4 (0x408A, 0x408B)

FOC_EK4H(0x408A)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EK4[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_EK4L(0x408B)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EK4[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EK4	The 4th coefficient of the current model in estimator. Q15 format. Range [-32768, 32767]

15.2.46 FOC_EK1 (0x408C, 0x408D)

FOC_EK1H(0x408C)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EK1[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_EK1L(0x408D)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EK1[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EK1	The 1st coefficient of the current model in estimator. MSB is always 0. Q15 format. Range [0,32767].

15.2.47 FOC_EK2 (0x408E, 0x408F)

FOC_EK2H(0x408E)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EK2[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_EK2L(0x408F)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EK2[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EK2	The 2nd coefficient of the current model in estimator. MSB is always 0. Q15 format. Range [0,32767].

15.2.48 FOC_IDREF (0x4090, 0x4091) (Shared with BLDC Control)

FOC_IDREFH(0x4090)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_IDREF[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

FOC_IDREFL(0x4091)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_IDREF[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_IDREF	User-defined d-axis Current Reference Value Range [-32768,32767]

15.2.49 FOC_IQREF (0x4092, 0x4093) (Shared with BLDC Control)

FOC_IQREFH(0x4092)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_IQREF[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_IQREFL(0x4093)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_IQREF[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_IQREF	User-defined q-axis Current Reference Value Range [-32768,32767]

15.2.50 FOC_DQKP (0x4094, 0x4095) (Shared with BLDC Control)

FOC_DQKPH(0x4094)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_DQKP[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_DQKPL(0x4095)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_DQKP[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_DQKP	KP of dq-axis PI Controller. MSB is always 0. Q12 format. Range [0,32767].

15.2.51 FOC_DQKI (0x4096, 0x4097) (Shared with BLDC Control)

FOC_DQKIH(0x4096)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_DQKI[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_DQKIL(0x4097)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_DQKI[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_DQKI	KI of dq-axis PI Controller. MSB is always 0. Q15 format. Range [0,32767].

15.2.52 FOC__UDCFLT (0x4098, 0x4099)

FOC__UDCFLTH(0x4098)								
Bit	15	14	13	12	11	10	9	8
Name	FOC__UDCFLT[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC__UDCFLTL(0x4099)								
Bit	7	6	5	4	3	2	1	0
Name	FOC__UDCFLT[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC__UDCFLT	Filtered Bus voltage FOC module samples the bus voltage and filters it for FOC_UDCFLT. The default channel is ADC channel 2. Range [0,32767] Example: The bus voltage is scaled down by 1/6 before feeding into the ADC module, ADC VREF = 5V (namely, the sampling range is [0V ~ 30V]) and FOC__UDCFLT = 19661(0x4CCD), then bus voltage = 19661/32768 *5V*6 = 18V.

15.2.53 FOC_CR3 (0x40EE)

Bit	7	6	5	4	3	2	1	0
Name	ICLR	RSV	MFP_EN	FOCUSTA	FOCFEN	ESCMS	TSMINH9	TSMINH8
Type	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	-	0	0	0	0	0	0

Bit	Name	Description
[7]	ICLR	Clear FOC_IA/B/CMAX to “0” A write of “1” clears FOC_IA/B/CMAX to “0”. This bit is automatically set to “0” after FOC_IA/B/CMAX are cleared to “0”. 0: Disable 1: Enable
[6]	RSV	Reserved
[5]	MFP_EN	Adaptive Observer Enable 0: Disable 1: Enable
[4]	FOCUSTA	Single-shunt Off Sampling Enable 0: Disable 1: Enable
[3]	FOCFEN	FOC Force Enable When DRV_CR[MESEL] is set to “1”, FOC module performs calculation even if DRV_CR[OCS] = 0. 0: Disable 1: Enable
[2]	ESCMS	ATAN Estimation Enable 0: Disable 1: Enable
[1:0]	TSMINH[9:8]	Scale up by two bits of FOC_TSMIN

15.2.54 FOC_DKP (0x409C, 0x409D)

FOC_DKPH(0x409C)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_DKP[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_DKPL(0x409D)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_DKP[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_DKP	KP of d-axis PI Controller. MSB is always 0. Q12 format Range [0,32767]. It is valid when FOC_DKP! = 0. Otherwise, the original FOC_DQKP/I is applied.

15.2.55 FOC_DKI (0x409E, 0x409F)

FOC_DKIH(0x409E)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_DKI[15:8]							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_DKIL(0x409F)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_DKI[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_DKI	KI of d-axis PI Controller. MSB is always 0. Q15 format. Range [0,32767].

15.2.56 FOC__IAMAX (0x40DA, 0x40DB)

FOC__IAMAXH(0x40DA)								
Bit	15	14	13	12	11	10	9	8
Name	FOC__IAMAX[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC__IAMAXL(0x40DB)								
Bit	7	6	5	4	3	2	1	0
Name	FOC__IAMAX[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC__IAMAX	Max. Phase-A Current This value may be unreliable unless the motor rotates in a full electrical period. It is also incorrect if the phase current is collected improperly. This maximum value will not be cleared to “0” automatically unless FOC_CR3[ICLR] is set to “1”. Range [0,32767]

15.2.57 FOC_IBMAX (0x40DC, 0x40DD)

FOC_IBMAXH(0x40DC)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_IBMAX[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_IBMAXL(0x40DD)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_IBMAX[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_IBMAX	Max. Phase-B Current This value may be unreliable unless the motor rotates in a full electrical period. It is also incorrect if the phase current is collected improperly. This maximum value will not be cleared to “0” automatically unless FOC_CR3[ICLR] is set to “1”. Range [0,32767]

15.2.58 FOC_ICMAX (0x40DE, 0x40DF)

FOC_ICMAXH(0x40DE)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_ICMAX[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_ICMAXL(0x40DF)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_ICMAX[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_ICMAX	Max. Phase-C Current This value may be unreliable unless the motor rotates in a full electrical period. It is also incorrect if the phase current is collected improperly. This maximum value will not be cleared to “0” automatically unless FOC_CR3[ICLR] is set to “1”. Range [0,32767]

15.2.59 FOC_EMF (0x40E0, 0x40E1)

FOC_EMFH(0x40E0)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_EMF[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_EMFL(0x40E1)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_EMF[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_EMF	Estimated BEMF of Estimator This value is the root of sum of square of FOC_EALP and square of FOC_EBET Range [0,32767]

15.2.60 FOC_UDCPS (0x40E2,0x40E3)

FOC_UDCPSH(0x40E2)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_UDCPS[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_UDCPSL(0x40E3)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_UDCPS[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_UDCPS	d-axis Voltage Compensation Value The result of d-axis PI controller (FOC_UD) added to FOC_UDCPS is transferred to the next module. Range [-32768,32767]

15.2.61 FOC_UQCPS (0x40E4, 0x40E5)

FOC_UQCPSH(0x40E4)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_UQCPS[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

FOC_UQCPSL(0x40E5)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_UQCPS[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_UQCPS	q-axis Voltage Compensation Value The result of q-axis PI controller (FOC_UQ) added to FOC_UQCPS is transferred to the next module. Range [-32768,32767]

15.2.62 FOC_UQEX (0x40E6, 0x40E7)

FOC_UQEXH(0x40E6)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_UQEX[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
FOC_UQEXL(0x40E7)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_UQEX[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_UQEX	q-axis Overflow Value for Flux-weakening Control Equation: FOC_UQ - FOC_QMAX FOC_UQEX is positive when FOC_UQ > FOC_QMAX; FOC_UQEX is negative when FOC_UQ < FOC_QMAX; FOC_UQEX can be used to realize flux-weakening control Range [-32768,32767]

15.2.63 FOC_ID_LPFK (0x40E8)

Bit	7	6	5	4	3	2	1	0
Name	FOC_ID_LPFK							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	Name	Description
[7:0]	FOC_ID_LPFK	LPF coefficient of FOC_ID Range [0,255]

15.2.64 FOC_IQ_LPFK (0x40E9)

Bit	7	6	5	4	3	2	1	0
Name	FOC_IQ_LPFK							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	Name	Description
[7:0]	FOC_IQ_LPFK	LPF coefficient of FOC_IQ Range [0,255]

15.2.65 FOC_KFG (0x40EA, 0x40EB)

FOC_KFGH(0x40EA)								
Bit	15	14	13	12	11	10	9	8
Name	FOC_KFG[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
FOC_KFGL(0x40EB)								
Bit	7	6	5	4	3	2	1	0
Name	FOC_KFG[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	FOC_KFG	Coefficient of FG Calculation FOC module performs the calculation based on FOC_EOMELPF and FOC_KFG in each PWM cycle. The result is updated to TIM4_ARR and half of the result (TIM4_ARR/2) to TIM4_DR by hardware. Range [0,65535]. Note When FOC_KFG = 0, this feature is disabled. The clock division factor TIM4_CR0[T4PSC] of Timer4 shall be adjusted if FOC_KFG overflows.

16 Timer1

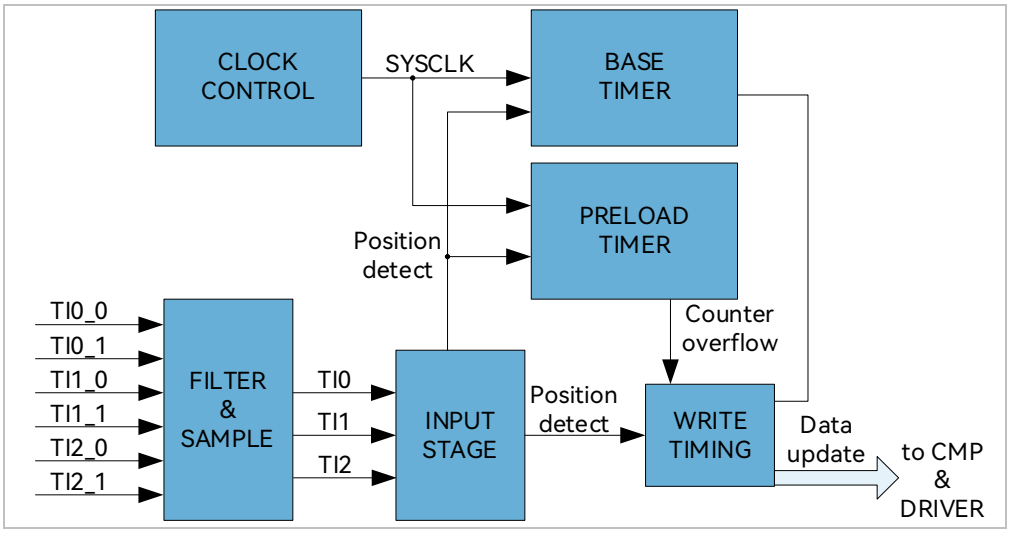
16.1 Timer1 Operations

Timer1 consists of an internal 16-bit up-counting Basic Timer and an internal 16-bit up-counting Reload Timer. Timer1 can be used in the applications of square-wave controlled BLDC motor drive or Hall signals processing. Timer1 features as follows.

- The 16-bit up-counting Basic Timer is used to record the time between two position detection events or writing timings, that is, two phase commutations (60 degree time);
- The 16-bit up-counting Reload Timer is used to control the time between position detection and reload timer overflow, that is, masking time for diode freewheeling as well as the time from ZCP to phase commutation.
- The 3-bit programmable frequency prescaler divides the system clock. The divided clock is used as the clock source of the two timers.
- Input filtering and sampling
- Position detection module generates the position signal required according to the input signal
- The output status register is updated by the writing timing module
- 7 groups of state registers control comparators and outputs
- 6 interrupt sources
  - Basic timer overflow interrupt
  - Reload timer overflow interrupt
  - Write timing interrupt
  - Position detection interrupt
  - Shield freewheeling end interrupt
  - ADC detection interrupt

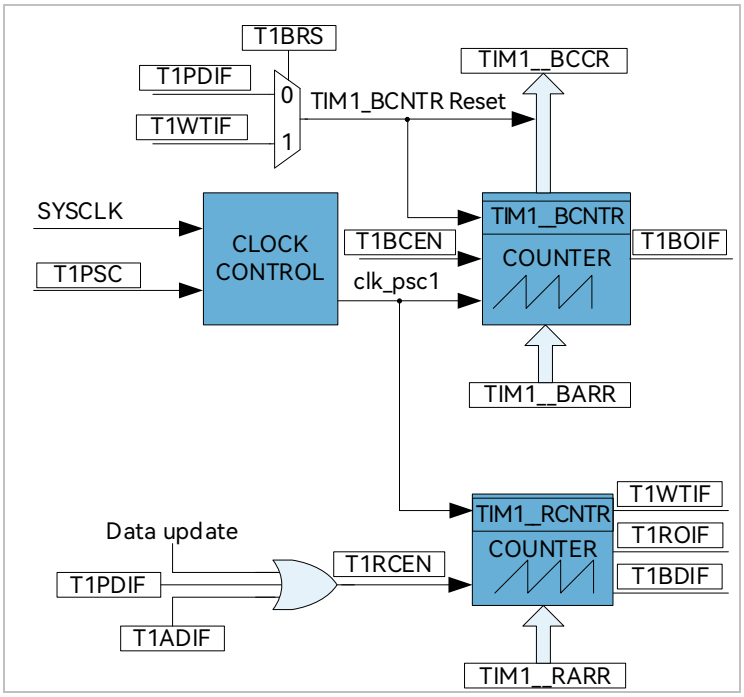
The internal structure of Timer1 is shown in Figure 16-1.

Figure 16-1 Internal Structure of Timer1



16.1.1 Timer1 Counter Module

Figure 16-2 Timebase Unit



Timer1 consists of a frequency prescaler, an 16-bit up-counting Basic Timer and an 16-bit up-counting Reload Timer.

16.1.1.1 Prescaler

Prescaler divides the system clock frequency and generates the counter clock source for Basic Timer and Reload Timer. It offers 8 division coefficients and can be selected through TIM1_CR3[T1PSC]. Since this register has no buffer, the clock rate is immediately updated after the division coefficient is written. Therefore, the division coefficient shall be configured when both the Basic Timer and Reload Timer are not working. The clock rate clk_psc1 = SYSCLK/(2^TIM1_CR3[T1PSC]). The clock rate corresponding to TIM1_CR3[T1PSC] is shown in Table 16-1.

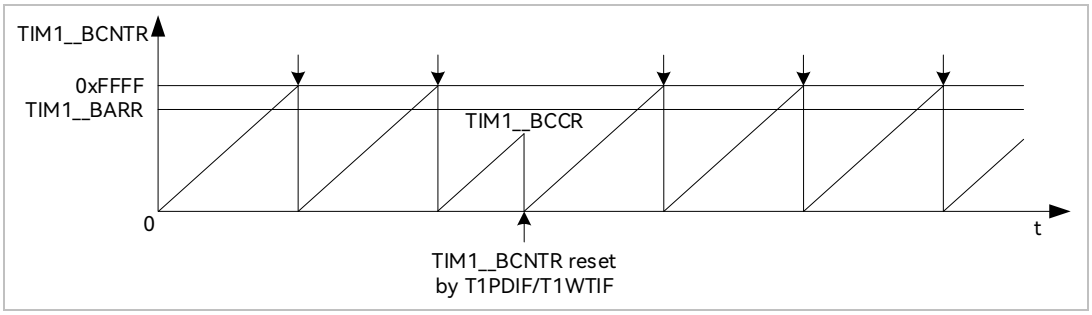
Table 16-1 Mapping between Clock Rate and TIM1_CR3[T1PSC]

TIM1_CR3[T1PSC]	Division Factor	clk_psc1(Hz)	TIM1_CR3[T1PSC]	Division Factor	clk_psc1(Hz)
000	0x1	24M	100	0x10	1.5M
001	0x2	12M	101	0x20	750k
010	0x4	6M	110	0x40	375k
011	0x8	3M	111	0x80	187.5k

16.1.1.2 Basic Timer

The Basic Timer is a 16-bit up timer with its count value held in TIM1_BCNTR. When count value of TIM1_BCNTR increases to TIM1_BARR, overflow interrupt flag TIM1_SR[T1BOIF] of the Basic Timer is set to “1” and TIM1_BCNTR continues (instead of being cleared to “0” to restart the counter cycle). TIM1_BCNTR value is loaded into TIM1_BCCR upon a Position Detection Interrupt or a Write Timing Interrupt (selected by TIM1_CR2[T1BRS]). Meanwhile, TIM1_BCNTR is cleared to “0” and restarts the counter cycle.

Figure 16-3 Waveform of Basic Timer



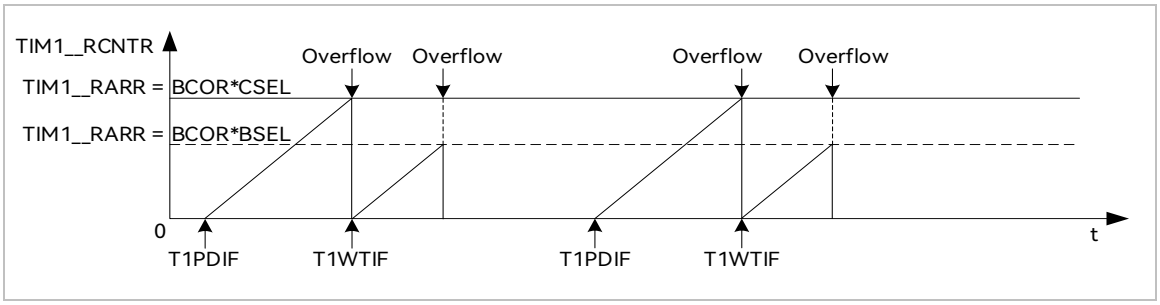
TIM1_BARR register shall be updated when the basic timer stops working, so that its value is immediately applied to the timer. The overflow event occurs only when TIM1_BCNTR is equal to the value held by

TIM1__BARR. When TIM1__BCNTR is larger than the value held by TIM1__BARR, TIM1__BCNTR restarts from 0 after it reaches 0xFFFF. In this case, TIM1__BCNTR cannot be greater than TIM1__BARR after the register is initialized.

16.1.1.3 Reload Timer

The Reload Timer is a 16-bit up timer with its count value held in TIM1__RCNTR. The timer overflows when TIM1__RCNTR increases to TIM1__RARR. In this case, TIM1_SR[T1ROIF] (overflow interrupt flag of the reload counter) is set to "1", and TIM1__RCNTR and TIM1_CR0[T1RCEN] are cleared to "0". The timer restarts after TIM1_CR0[T1RCEN] is set to "1".

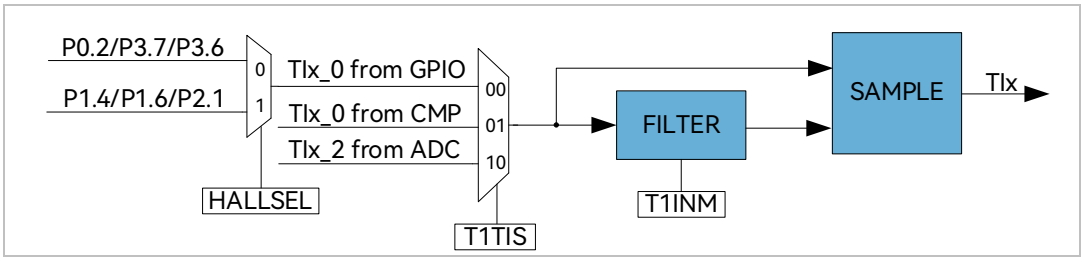
Figure 16-4 Waveform of Reload Timer



TIM1_CR0[T1RCEN] is set to "1" upon a position detection interrupt or write timing interrupt. After the Reload Timer overflows, TIM1_CR0[T1RCEN] is cleared to "0" by hardware and the timer stops counting. The Reload Timer is mainly used to realize diode freewheeling masking and delay commutation after ZCP for square-wave control over BLDC motors. It does not work in other situations.

16.1.2 Position Detection

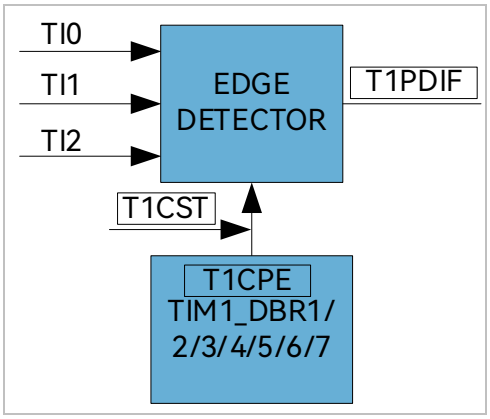
Figure 16-5 Functional Block Diagram of Input Signal Filtering and Sampling



TIM1_CR3[T1TIS] selects the sources from comparator or GPIO. CMP_CR1[HALLSEL] is used to configure GPIO sourced by P1.4/P1.6/P2.1 or P0.2/P3.7/P3.6. TIM1_CR3[T1INM] decides whether the signal is filtered and CMP_CR3[SAMSEL] determines sampling delay feature is enabled or disabled.

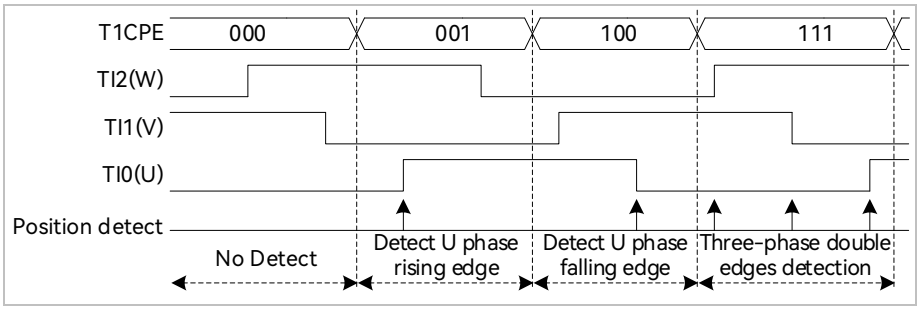
16.1.2.1 Position Detection Events

Figure 16-6 Functional Block Diagram of Position Detection



The register bank TIM1_DBR1/2/3/4/5/6/7[T1CPE] is configured to select the active edge of position detection signal. An position detection event is generated after an input active edge (TI2/TI1/TI0) is detected. TIM1_CR4[T1CST] selects TIM1_DBR1/2/3/4/5/6/7[T1CPE] timing.

Figure 16-7 Functional Block Diagram of Position Detection



The relation between active edge and TIM1_DBR1/2/3/4/5/6/7[T1CPE] is shown in Table 16-2.

Table 16-2 Mapping between Active Edge and TIM1_DBR1/2/3/4/5/6/7[T1CPE]

T1CPE	Description	T1CPE	Description
000	0	100	Phase-U corresponding comparator is enabled when falling edge of phase-U is detected.
001	Phase-U corresponding comparator is enabled when rising edge of phase-U is detected.	101	phase-W corresponding comparator is enabled when rising edge of phase-W is detected.
010	phase-W corresponding comparator is enabled when falling edge of phase-W is detected.	110	Phase-V corresponding comparator is enabled when falling edge of phase-V is detected.
011	Phase-V corresponding comparator is enabled when rising edge of phase-V is detected.	111	Phase-U+W+V corresponding comparator is enabled when rising or falling edge of phase-U+W+V is detected.

16.1.2.2 Sampling

Figure 16-8 PWM ON Sampling Mode

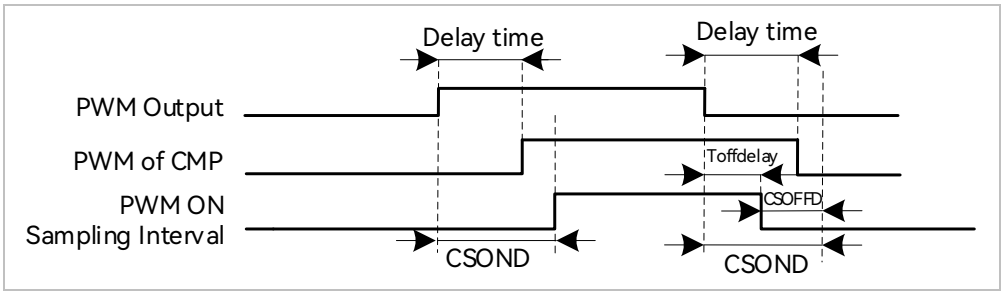
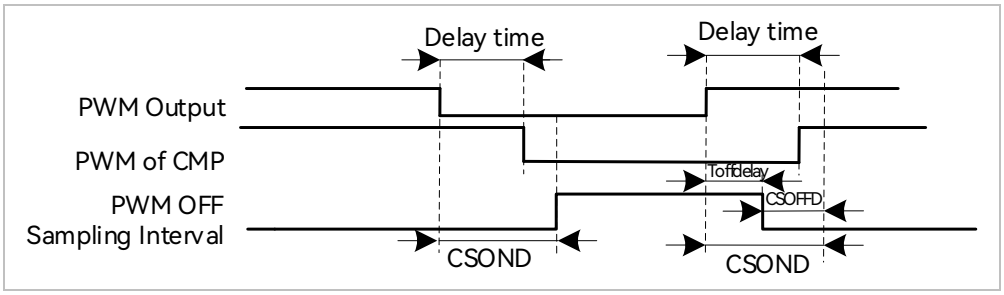


Figure 16-9 PWM OFF Sampling Mode



In the square wave control mode, the input of TI2/TI1/TI0 comes from the comparator. Due to MOS on-off from driving circuit, PWM signals create electromagnetic interference. Therefore, CMP_CR3[SAMSEL], CMP_SAMR[CSOFFD] and CMP_SAMR[CSOND] shall be set reasonably to adjust the sampling interval and obtain the valid position detection signal.

There is a delay from PWM output to the output of the comparator, which is mainly affected by the following factors: resistance value of drive resistor, MOS switch speed, and input delay and hysteresis settings of the comparator. In this case, CMP_SAMR[CSOFFD] is set to delay comparator sampling by offdelay, in order to avoid the interference from comparators, where offdelay = CSOND-CSOFFD and means the sampling delay for CMP0, CMP1 and CMP2.

For example, the delay from PWM output to the output of the comparator is 2μs and the interference width is 1μs, then

CSOFFD >1μs = 1000ns/41.67ns/8 = 3

CSOND > (2 + 1) μs = 3000ns/41.67ns/8 = 9

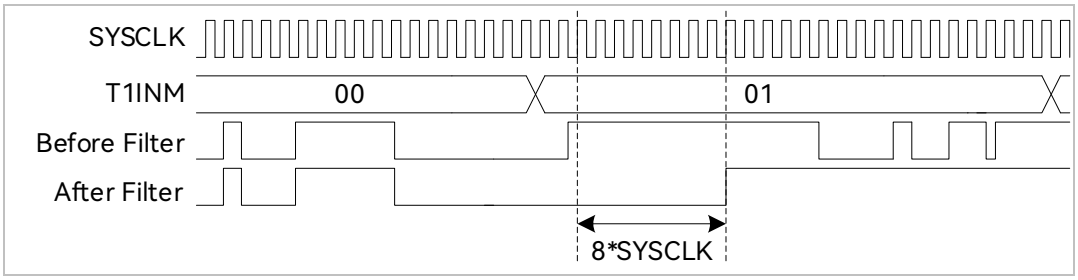
Method for measuring the delay of PWM output to comparator: Set CMP_CR3[SAMSEL] = 00 to disable the

comparator sampling delay feature. Enable PWM output and comparator, manually rotate the motor to change the comparator value, and measure the delay between the PWM output and the comparator output.

Method for measuring interference width: The operations are the same as above.

16.1.2.2.1 Filtering

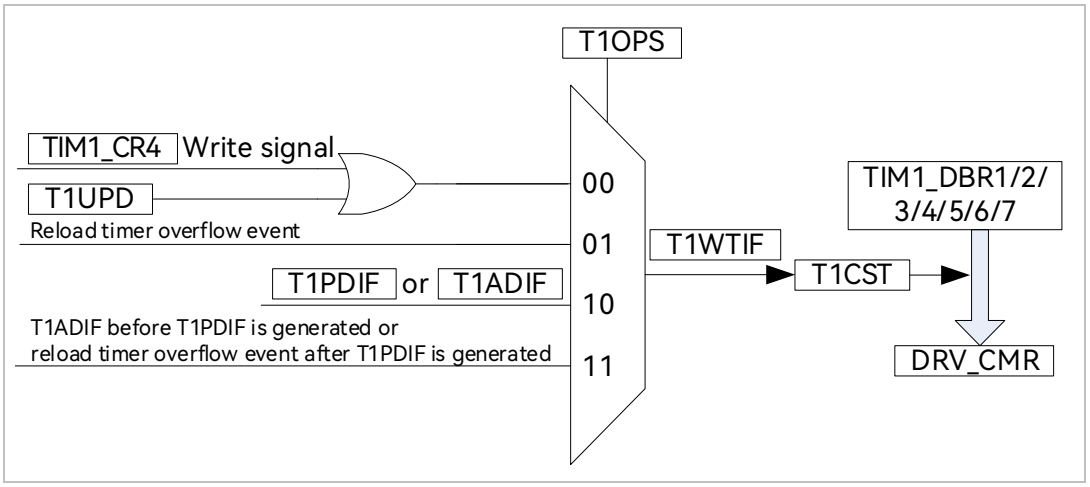
Figure 16-10 Timing Diagram of Filtering Module



According to TIM1_CR3[T1INM], the filtered pulse width of input noise can be selected as 8/32/64 system clocks. After this feature is enabled, the signal is delayed by about 8~ 9/32 ~ 33/64 ~ 65 system clocks.

16.1.3 Write Timing Interrupt

Figure 16-11 Writing Timing Block Diagram



The triggered source of write timing interrupt is selected by TIM1_CR0[T1OPS]. After a write timing interrupt is generated, write timing interrupt flag TIM1_SR[T1WTIF] is set to “1”. If TIM1_CR4[T1CST] ranges in 001 ~ 110, TIM1_CR4[T1CST] adds 1 automatically and the value held by TIM1_DBR1/2/3/4/5/6/7 is updated to DRV_CMR.

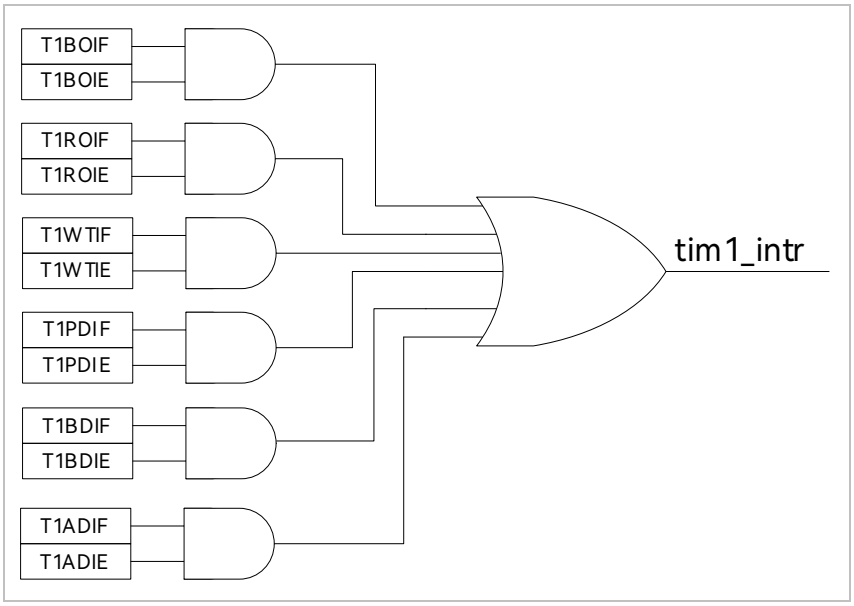
16.1.4 Timer1 Interrupts

Timer1 supports 6 interrupt sources:

- Basic timer overflow interrupt
- Reload timer overflow interrupt
- Write timing interrupt
- Position detection interrupt
- Diode freewheeling end interrupt
- ADC position detection interrupt

Configuring enable bit of TIM1_IER enables or disables the corresponding interrupt request.

Figure 16-12 Timer1 Interrupt Sources



16.2 Square-wave Control for BLDC Motors

For BLDC motor square-wave control applications, Timer1 works with CMP0/1/2 and Driver module to achieve the following features:

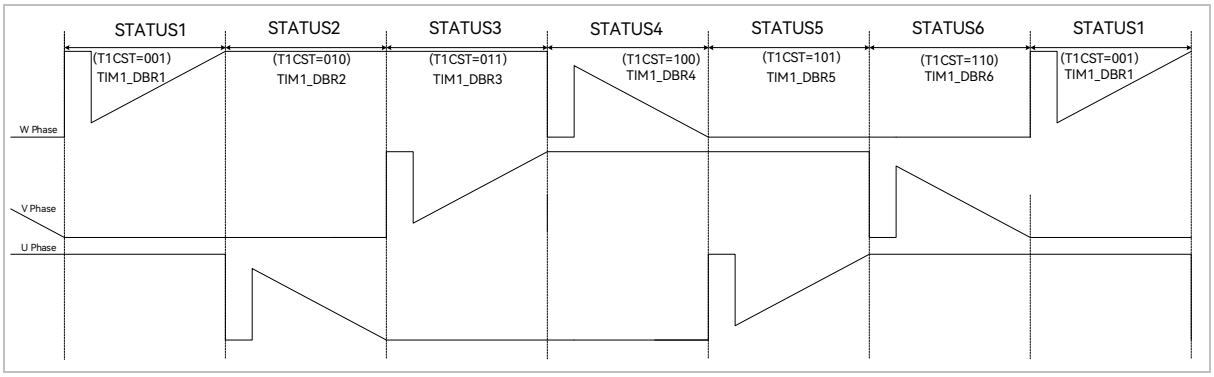
- Automatic record of 60 degree time, filtered as 60 degree reference time
- Automatic forced phase commutation when no position signal is detected
- Automatic diode freewheeling masking, i.e., stopping comparator sampling during diode freewheeling
- Automatic control of the time from position detection to phase commutation to achieve automatic

commutation

- Take over CMP_CR2[CMP0SEL] to control CMP0/1/2 automatically
- Comparator signals can be configured to avoid switching ringing of the power devices, and the signals can be filtered as well
- Take over DRV_CMR register to control 6-channel PWM outputs automatically

16.2.1 Six-Step Phase Commutation of Square Wave Control

Figure 16-13 Diagram of Six-step Phase Commutation of Square Wave Control

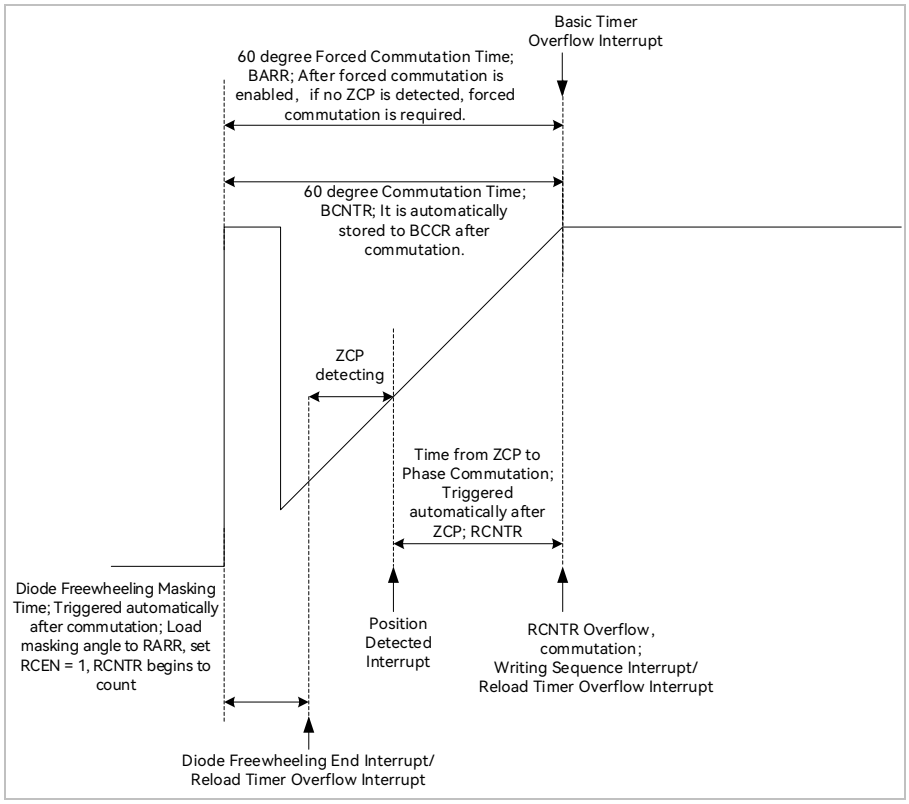


TIM1_CR4[T1CST] is the commutation state machine. Among them, state 0 is used to output off state, and state 7 is customizable for braking, pre-charging, pre-positioning, startup, etc. States 1 ~ 6 are used for six-step automatic commutation, and the state machine TIM1_CR4[T1CST] automatically adds 1 after phase commutation.

The states 1 ~ 7 maps to the TIM1_DBR1 ~ 7. When write timing interrupt is generated, TIM1_DBRx corresponding to the current state is automatically transferred to DRV_CMR and CMP_CR2[CMP0SEL] for phase commutation and position detection.

16.2.2 Working Principle of Square-wave Control

Figure 16-14 Working Principle of Square-wave Control



16.2.2.1 60° Commutation Base Time

TIM1_BCCR captures the time of previous 60 degree. TIM1_CR2[T1BRS] is set to “0” to capture the time between two phase commutations (i.e., 60 degree base time) and TIM1_CR2[T1BRS] to “1” to capture the time between two zero-crossing points (i.e., 60 degree base time).

TIM1_BCOR is the filtered 60 degree time, i.e., 60 degree base time. TIM1_CR0[T1CFLT] can select the previous 1/2/4/8 TIM1_BCCR averaged to obtain TIM1_BCOR.

In square-wave control mode, the diode freewheeling masking time, the time from position detection to phase commutation, and the time to forced commutation are determined by the 60 degree base time TIM1_BCOR.

16.2.2.2 Phase Commutation

TIM1_CR0[T1OPS] decides phase commutation mode. Configuring TIM1_CR0[T1OPS] = 00 enables

sensorless control, TIM1_CR0[T1OPS]= 01 enables sensorless automatic commutation, or TIM1_CR0[T1OPS] = 10 enables sensored commutation.

After phase commutation, Timer1 automatically performs the following operations:

1. Store the data held by TIM1_BCNTR to TIM1_BCCR for filtering, and then sends it to TIM1_BCOR as the 60 degree base time;
2. TIM1_BCNTR starts counting from “0”;
3. Start freewheeling mask, write the mask angle into TIM1_RARR and set TIM1_CR0[T1RCEN] to “1”. TIM1_RCNTR begins to count;
4. If TIM1_CR4[TICST] is in the state 1 to 6, it automatically switches to the next state;
5. Write timing interrupt TIM1_SR[T1WTIF] and reload timer overflow interrupt TIM1_SR[T1ROIF] are generated.

16.2.2.3 Forced Commutation at 60°

When the motor rotates smoothly, ZCP is generally detected after 30 degrees of rotation after phase commutation. If no ZCP is detected in 60 degree after phase commutation, a forced phase commutation is required. In this case, TIM1_CR0[T1FORC] is set to “1” to enable the forced commutation feature. If no ZCP is detected in 60 degree after commutation, TIM1_SR[T1BOIF] (overflow interrupt flag of the Basic Timer) is set to “1” for forced phase commutation.

Note

If an ZCP is detected within 60 degrees after phase commutation (TIM1_CR0[T1FORC] = 1), even when TIM1_BCNTR > TIM1_BARR, the forced commutation will not be triggered and TIM1_SR[T1BOIF] will not be set to “1”.

When forced commutation feature is disabled (TIM1_CR0[T1FORC] = 0) and TIM1_BCNTR > TIM1_BARR, the interrupt flag TIM1_SR[T1BOIF] is set to “1” and TIM1_BCNTR continues. Phase commutation can be performed manually (via software) by Basic Timer overflow interrupt flag TIM1_SR[T1BOIF] and the position detection interrupt flag TIM1_SR[T1PDIF].

16.2.2.4 Diode Freewheeling Masking

After the commutation, inductance energy of the phase is released to the power supply or ground through

the diode since the original active phase becomes a floating phase. By masking comparator signal during freewheeling time, wrong commutation caused by wrong signal generated by the freewheeling is avoided. After freewheeling masking, the freewheeling masking end interrupt flag TIM1_SR[T1BDIF] is generated.

Timer1 holds the last latched level value of the comparator during freewheeling masking, and samples the level value after freewheeling masking. If the time for freewheeling masking is shorter than that for freewheeling, a false zero-crossing trigger point is generated. Therefore, it is necessary to adjust freewheeling masking time according to motor characteristics and ensure it is longer than freewheeling time.

Freewheeling masking time is set by TIM1_CR1[BSEL] with the formula: Masking angle = TIM1_CR1[BSEL]/128*60°.

16.2.2.5 Angle of ZCP to Phase Commutation (Delayed Commutation)

A zero-crossing detection is performed after diode freewheeling masking. If no ZCP is detected, the detection continues until phase commutation. It is triggered by a position detection interrupt, and only the first position detection interrupt is the effective trigger source. If a ZCP is detected, zero-crossing detection is completed and other subsequent trigger sources become invalid. Therefore, parameters related to filtering and sampling must be properly configured to ensure the first trigger source is a correct zero-crossing point.

After commutation, a ZCP is detected (generating a position detection interrupt) and the hardware starts TIM1_RCNTR for counting according to the software-set time between ZCP and the commutation. After the counting ends, the hardware automatically implements phase commutation and generates the write timing interrupt flag TIM1_SR[T1WTIF].

The time between ZCP and phase commutation is set by TIM1_CR2[CSEL] with the formula: Commutation angle = TIM1_CR2[CSEL]/128*60°.

16.2.2.6 Cycle-by-cycle Current Limiting

See section 31.1.1.2.

16.2.3 BLDC Control Debugging

The chip supports the following debugging methods.

- Display comparator signals in real time via P0.7
- Set EXT0[TIM4_CT] = 1 to display the status of Timer1 in real time via P0.1
- Display Timer1 related registers on the oscilloscope via SPI debugger

16.2.3.1 Comparator Debugging

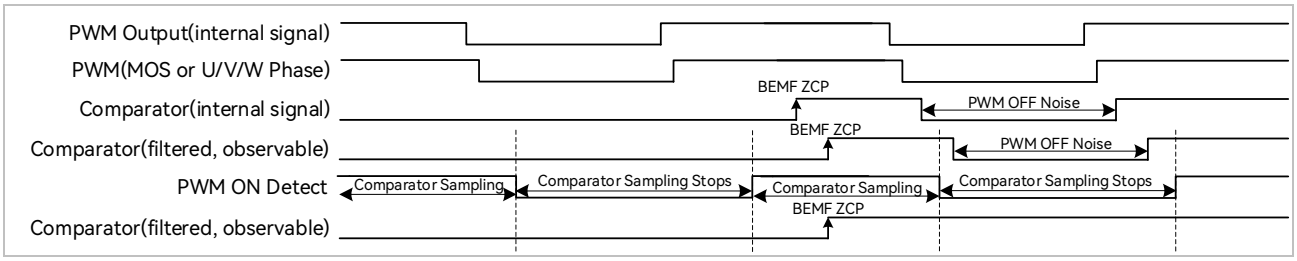
Configure CMP_CR3[DBGSEL] = 11 to output comparator signals via P0.1. See section 16.1.2.2 for waveforms. Select sampling delay by CMP_CR3[SAMSEL], as shown in the below table.

Table 16-3 Relation between CMP_CR3[SAMSEL] and P0.1 Output

SAMSEL	Sampling Delay	P0.1 Output
00	Sampling at both PWM ON and OFF modes without time delay	Constant high level
01	Sampling at PWM OFF, with time delay according to CMP_SAMR	Sampling at PWM OFF
10	Sampling at PWM ON, with time delay according to CMP_SAMR	Sampling at PWM ON
11	Sampling at both PWM ON and OFF, with time delay according to CMP_SAMR	Sampling at both PWM ON and OFF

Display comparator sampling, one of the signals of CMP0/1/2OUT and the corresponding phase signal of phase-U/V/W output on the oscilloscope, adjust CMP_SAMR register to fall the comparator sampling waveform within the PWM waveform and then observe whether CMP0/1/2OUT meets the requirements.

Figure 16-15 Comparator Debugging

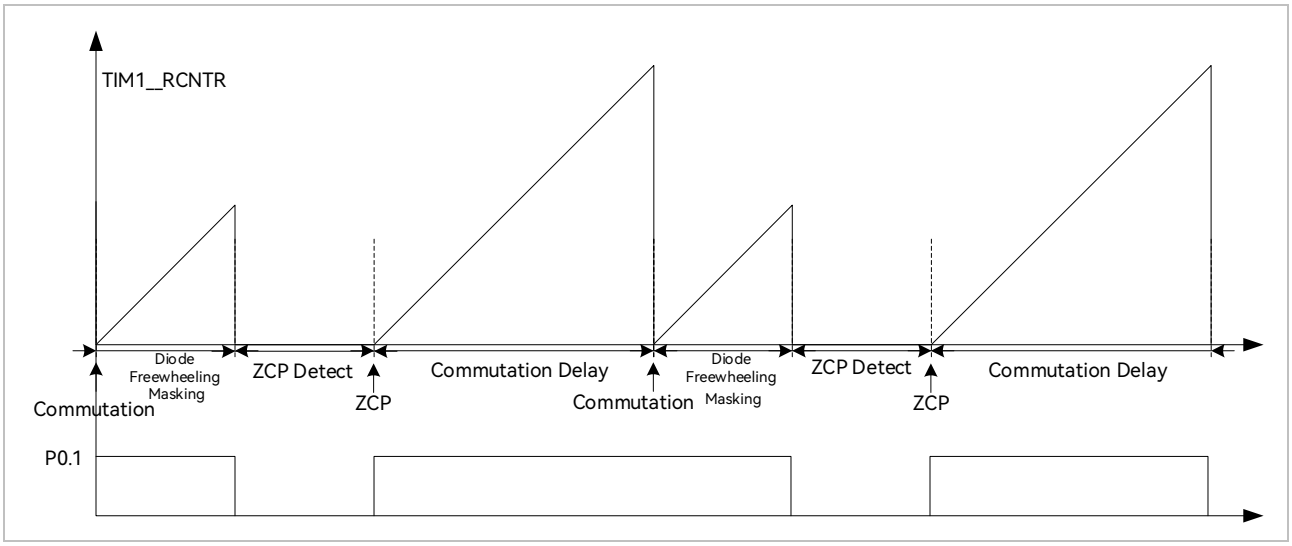


16.2.3.2 Debugging on Diode Freewheeling Masking and Phase Commutation

The reload timer TIM1_RCNTR is used for freewheeling masking and delayed commutation, so SPI debugger can be used to display its waveform on the oscilloscope.

After the real-time status of Timer1 is displayed via P0.1, waveforms of the freewheeling masking, ZCP and delayed commutation are obtained through phase-U/V/W commutation points.

Figure 16-16 RCNTR/P0.6 Waveform at 15° Freewheeling Masking and 30° Delayed Commutation



16.3 Phase Commutation Signals by ADC

Formula K*A-B, where K refers to coefficient, A to sampled voltage of active phase and B to sampled voltage of floating phase. When the symbol of the formula changes, phase commutation signal is generated.

Table 16-4 Relation between TIM1_DBR1/2/3/4/5/6/7[T1CPE] and K/A/B

T1CPE	Description
000	No sampling
001	A = W, B = U, K = TIM1_KR

T1CPE	Description
010	A = U, B = W, K = TIM1_KF
011	A = U, B = V, K = TIM1_KR
100	A = V, B = U, K = TIM1_KF
101	A = V, B = W, K = TIM1_KR
110	A = W, B = V, K = TIM1_KF
111	Reserved

Similar to the comparator, ADC can also samples the volage at PWM ON/OFF. To reduce interference, filtering counts for ADC sampled voltage can be set as 2 or 4 by TIM1_CR3[T1AFL].

ADC has basically the same configurations for phase commutation as the comparator. But ADC has more flexible calculation formula, including different coefficients K, symbol flip with different position points, etc. For example, K = TIM1_KR = TIM1_KF = 0.5, the symbol flip point is ZCP.

16.4 Timer1 Registers

16.4.1 TIM1_CR0 (0x4068)

Bit	7	6	5	4	3	2	1	0
Name	T1RWEN	T1CFLT		T1FORC	T1OPS		T1BCEN	T1RCEN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	T1RWEN	When TIM1_CR0 is updated, TIM1_CR0[T1RWEN] must be set to “1” to enable TIM1_CR0[T1RCEN]. This bit can be read to “0” only.
[6:5]	T1CFLT	60 Degree Base Time Filtering Selection The average of previous x times 60 degree is used as the base time 00: 1 times 60 degree 01: 2 times 60 degree 10: 4 times 60 degree 11: 8 times 60 degree
[4]	T1FORC	Forced Phase Commutation at 60° Enable If no ZCP is detected after phase commutation, the hardware implements forced phase commutation. But if a ZCP is detected, forced phase commutation will not be implemented even if TIM1__BCNTR exceeds TIM1__BARR. 0: Disable 1: Enable

		Note If TIM1_CR0[T1FORC] = 0, TIM1__BCNTR continues (does not restart from “0”) and forced phase commutation will not be implemented even if TIM1__BCNTR exceeds TIM1__BARR.
[3:2]	T1OPS	Data Transfer Mode Selection This bit selects the trigger signal for TIM1_DBRx to transfer data to DRV_CMR, i.e., writing timing even or phase commutation. 00: The transfer is triggered upon a write of “1” to TIM1_IER[T1UPD] in software or on a write to TIM1_CR4[T1CST] (sensorless square-wave control) 01: The transfer is triggered upon an overflow interrupt of 16-bit reload timer during phase commutation (sensorless square-wave control) 10: The transfer is triggered upon a Position Detection Interrupt (sensored square-wave control) or ADC calculation result 11: The transfer is triggered upon an overflow interrupt of 16-bit reload timer during phase commutation or ADC calculation result
[1]	T1BCEN	Basic Timer Enable 0: Disable 1: Enable
[0]	T1RCEN	Reload Timer Enable When TIM1_CR0 is updated, TIM1_CR0[T1RWEN] must be set to “1” to enable TIM1_CR0[T1RCEN]. TIM1_CR0[T1RCEN] is automatically enabled upon a Position Detection Interrupt and a Write Timing Interrupt. TIM1_CR0[T1RCEN] is cleared to “0” by hardware upon a Reload Timer Overflow Interrupt. 0: Disable 1: Enable

16.4.2 TIM1_CR1 (0x4069)

Bit	7	6	5	4	3	2	1	0
Name	T1BAPE	BSEL						
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	T1BAPE	TIM1__BARR Register Auto-load Enable With this bit enabled, TIM1__BCOR is written to TIM1__BARR when Basic Timer is reset due to a Position Detection Interrupt or a Write Timing Interrupt. It is used for forced phase commutation at 60°when no ZCP is detected. Manual mode has no effect on TIM1__BARR Register auto-load feature. 0: Disable

		1: Enable
[6:0]	BSEL	Diode Freewheeling Masking Angle Selection This bit is used to configure the angle (time) of diode freewheeling masking after phase commutation. Position is not detected during diode freewheeling masking. Equation: Diode freewheeling masking angle = TIM1_CR1[BSEL]/128*60° Note This bit is invalid in Manual mode.

16.4.3 TIM1_CR2 (0x406A)

Bit	7	6	5	4	3	2	1	0
Name	T1BRS	CSEL						
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	T1BRS	Basic Timer Reset Source Selection This bit is invalid in Manual mode (TIM1_IER[T1MAME] = 1). TIM1__BCNTR can only be cleared by a BCNTR Overflow Interrupt. 0: Writing Timing Reset 1: Position Detection Interrupt Reset
[6:0]	CSEL	Phase Commutation Angle Selection After a position detection event, phase commutation is implemented after the degree configured by TIM1_CR2[CSEL]. Equation: Commutation angle = TIM1_CR2[CSEL]/128*60 Note This bit shall be set as “1” if the phase commutation angle is required at 0.

16.4.4 TIM1_CR3 (0x406B)

Bit	7	6	5	4	3	2	1	0
Name	T1AFL	T1PSC			T1TIS		T1INM	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	0

Bit	Name	Description
[7]	T1AFL	ADC Sampled Voltage Calculation Filtering Counts 0: 4 1: 2
[6:4]	T1PSC	Timer Clock Source Frequency Selection

		These bits are configured to divide the system clock as the clock source for Basic Timer and Reload Timer. Assuming that MCU clock runs at 24MHz(41.67ns): 000: 0x1 (24MHz) 001: 0x2 (12MHz) 010: 0x4 (6MHz) 011: 0x8 (3MHz) 100: 0x10 (1.5MHz) 101: 0x20 (750kHz) 110: 0x40 (375kHz) 111: 0x80 (187.5kHz)
[3:2]	T1TIS	Position Detection Signal Selection Timer1 filters, samples and generates a position detection on the selected input source. This bit affects CMP0/1/2OUT and CMP0/1/2IF results of the comparator module CMP_SR. 00: GPIO as the input (P1.4/P1.6/P2.1 according to CMP_CR1[HALLSEL]). The results of CMP_SR is generated through the GPIO. 01: CMP0/1/2 as the input. The results of CMP_SR is generated through the comparator. 10: Output signal of ADC 11: Reserved
[1:0]	T1INM	Noise Pulse Width Selection for TI0/TI1/TI2 When pulse width of the noise is less than the set value, it is filtered as noise. Assuming that MCU clock runs at 24MHz(41.67ns): 00: Disable 01: 8 system clock cycles, 8 x 41.67ns 10: 32 system clock cycles, 32 x 41.67ns 11: 64 system clock cycles, 64 x 41.67ns

16.4.5 TIM1_CR4 (0x406C)

Bit	7	6	5	4	3	2	1	0
Name	RSV					T1CST		
Type	-	-	-	-	-	R/W	R/W	R/W
Reset	-	-	-	-	-	0	0	0

Bit	Name	Description
[7:3]	RSV	Reserved
[2:0]	T1CST	Commutation State Machine The state machine corresponds to different TIM1_DBRx at different states. When TIM1_CR4[T1CST] reads 001~111, Timer1 automatically enables or disables CMP0/1/2 according to the TIM1_DBRx[T1CPE]. When TIM1_CR4[T1CST] reads 001~110, Timer1 automatically adds by “1” each cycle upon a Write Timing Interrupt.

Table 16-5 Mapping between TIM1_CR4[T1CST] and TIM1_DBRx

TIM1_CR4[T1CST]	TIM1_DBRx	TIM1_CR4[T1CST]	TIM1_DBRx
000	0	100	TIM1_DBR4
001	TIM1_DBR1	101	TIM1_DBR5
010	TIM1_DBR2	110	TIM1_DBR6

		011	TIM1_DBR3	111	TIM1_DBR7	

16.4.6 TIM1_IER (0x406D)

Bit	7	6	5	4	3	2	1	0
Name	T1UPD	T1MAME	T1ADIE	T1BOIE	T1ROIE	T1WTIE	T1PDIE	T1BDIE
Type	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	T1UPD	When TIM1_CR0[T1OPS] = 00, a write of “1” to this bit enables data transfer. This bit is Write only, and automatically cleared to “0” by hardware after “1” is written.
[6]	T1MAME	Manual Mode Enable With this bit enabled, Basic Timer and Reload Timer acts as separate counters. Details: TIM1_BCNTR of the Basic Timer is cleared by a Basic Timer Overflow Interrupt instead of TIM1_CR2[T1BRS] TIM1_CR0[T1RCEN] of the Reload Timer cannot be cleared to “0” or set to “1” automatically, and is controlled by software only. TIM1_RCNTR of the Reload Timer can be cleared to “0” upon a Reload Timer Overflow Interrupt only. TIM1_RARR of the Reload Timer cannot be updated automatically, and is controlled by software only. 0: Disable 1: Enable
[5]	T1ADIE	ADC Position Detection Interrupt Enable 0: Disable 1: Enable
[4]	T1BOIE	Basic Timer Overflow Interrupt Enable 0: Disable 1: Enable
[3]	T1ROIE	Reload Timer Overflow Interrupt Enable 0: Disable 1: Enable
[2]	T1WTIE	Write Timing Interrupt Enable 0: Disable 1: Enable
[1]	T1PDIE	Position Detection Interrupt Enable 0: Disable 1: Enable
[0]	T1BDIE	Diode Freewheeling Masking Interrupt Enable 0: Disable 1: Enable

16.4.7 TIM1_SR (0x406E)

Bit	7	6	5	4	3	2	1	0
Name	RSV		T1ADIF	T1BOIF	T1ROIF	T1WTIF	T1PDIF	T1BDIF
Type	-	-	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0
Reset	-	-	0	0	0	0	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5]	T1ADIF	ADC Position Detection Interrupt Flag Position Detection Interrupt is generated when ADC position detection signal is the same as TIM_DBRx[T1CPE]. Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[4]	T1BOIF	Basic Timer Overflow Interrupt Flag An overflow event occurs when Basic Timer counts up and TIM1__BCNTR matches with TIM1__BARR. If TIM1_CR0[T1FORC] = 1, TIM1__BCNTR is cleared to “0”, otherwise, TIM1__BCNTR continues.  Note If TIM1__BCNTR is to be cleared during an interrupt, T1UPD or TIM1_CR4 is written when TIM1_CR2[T1BRS] = 0. Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[3]	T1ROIF	Reload Timer Overflow Interrupt Flag An overflow event occurs and TIM1__RCNTR is cleared to “0” when TIM1__RCNTR matches TIM1__RARR. Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[2]	T1WTIF	Write Timing Interrupt Flag

		Write Timing Interrupt is generated when TIM1_DBRx is transferred to DRV_CMR. Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[1]	T1PDIF	Position Detection Interrupt Flag A position detection interrupt is generated when Position Detection matches TIM1_DBRx[T1CPE]. Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[0]	T1BDIF	Diode Freewheeling Masking End Interrupt Flag Diode freewheeling masking starts after phase commutation and the interrupt is generated when masking finished Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect

16.4.8 TIM1_BCOR (0x4070, 0x4071)

TIM1_BCORH(0x4070)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_BCOR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM1_BCORL(0x4071)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_BCOR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM1_BCOR	This bit is configured to capture filtered count values held in the Basic Timer. TIM1_BCCR hods the filtered count value, i.e.60 Degree Base Time.

		Note TIM1_BCCR and TIM1_BCOR shall be initialized when the 60 Degree Base Time is initialized. For TIM1_BCCR, the 60 Degree Base Time can be directly written. For TIM1_BCOR, please note the followings: › TIM1_CR0[T1CFLT] = 00, 60 Degree Base Time; › TIM1_CR0[T1CFLT] = 01, 60 Degree Base Time /2; › TIM1_CR0[T1CFLT] = 10, 60 Degree Base Time /4; › TIM1_CR0[T1CFLT] = 11, 60 Degree Base Time /8.

16.4.9 TIM1_DBRx (x = 1~7)(0x4074+2*x, 0x4075+2*x)

TIM1_DBRx(x = 1 ~ 7) corresponds to the data when T1CST=1/2/3/4/5/6, respectively. TIM1_DBR1 is taken as an example to introduce TIM1_DBRx registers.

TIM1_DBR1H(0x4074)								
Bit	15	14	13	12	11	10	9	8
Name	RSV	T1CPE			T1WHP	T1WLP	T1VHP	T1VLP
Type	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	0	0	0	0	0	0	0
TIM1_DBR1L(0x4075)								
Bit	7	6	5	4	3	2	1	0
Name	T1UHP	T1ULP	T1WHE	T1WLE	T1VHE	T1VLE	T1UHE	T1ULE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15]	RSV	Reserved
[14:12]	T1CPE	TI0/TI1/TI2 Input Edge Polarity and Comparator Enable Selection These bits are used to define the edge of Position Detection Input and enable or disable the associated comparators. The detected edge in input signal, corresponding to the configuration, generates a position detection interrupt. See Position Detection Events and Table 16-2
[11]	T1WHP	High-side Output Polarity of Phase-W 0: Active High 1: Active Low
[10]	T1WLP	Low-side Output Polarity of phase-W 0: Active High 1: Active Low
[9]	T1VHP	High-side Output Polarity of Phase-V

		0: Active High 1: Active Low
[8]	T1VLP	Low-side Output Polarity of Phase-V 0: Active High 1: Active Low
[7]	T1UHP	High-side Output Polarity of Phase-U 0: Active High 1: Active Low
[6]	T1ULP	Low-side Output Polarity of Phase-U 0: Active High 1: Active Low
[5]	T1WHE	High-side Output Enable of Phase-W 0: Disable 1: Enable
[4]	T1WLE	Low-side Output Enable of Phase-W 0: Disable 1: Enable
[3]	T1VHE	High-side Output Enable of Phase-V 0: Disable 1: Enable
[2]	T1VLE	Low-side Output Enable of Phase-U 0: Disable 1: Enable
[1]	T1UHE	High-side Output Enable of Phase-U 0: Disable 1: Enable
[0]	T1ULE	Low-side Output Enable of Phase-U 0: Disable 1: Enable  Note The high-side and low-side outputs of phase-U are complementary and deadtime is automatically added when ULE and UHE are set to “1”.

 Note

The high-side and low-side outputs of three-phase are complementary and deadtime is automatically added when WLE and WHE, VLE and VHE, VLE and ULE, or ULE and UHE are set to “1”

16.4.10 TIM1_BCNTR (0x4082, 0x4083)

TIM1_BCNTRH(0x4082)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_BCNTR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM1_BCNTRL(0x4083)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_BCNTR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM1_BCNTR	This bit holds count values of the Basic Timer and is used for clocking commutation at 60°. Note TIM1_BCNTR selects the reset source according to TIM1_CR2[T1BRS], and TIM1_BCNTR does not restart when TIM1_BCNTR overflow interrupt is generated

16.4.11 TIM1_BCCR (0x4084, 0x4085)

TIM1_BCCRH(0x4084)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_BCCR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM1_BCCRL(0x4085)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_BCCR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM1_BCCR	This bit is configured to capture count values held in Basic Timer. When the Basic Timer is reset on a Position Detection Interrupt or a Write Timing Interrupt, the count values before the reset are stored into TIM1_BCCR.

16.4.12 TIM1_BARR (0x4086, 0x4087)

TIM1_BARRH(0x4086)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_BARR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM1_BARRL(0x4087)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_BARR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM1_BARR	Auto-Reload Value in Basic Timer When the count value of the Basic Timer equals to TIM1_BARR value, an overflow interrupt is generated and the timer is cleared to “0”.

16.4.13 TIM1_RARR (0x4088, 0x4089)

TIM1_RARRH(0x4088)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_RARR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM1_RARRL(0x4089)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_RARR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM1_RARR	Auto-Reload Value in Reload Timer When count of the Reload Timer is equal to TIM1_RARR, an overflow interrupt is generated and the value of timer is cleared to “0”.

16.4.14 TIM1_RCNTR (0x408A, 0x408B)

TIM1_RCNTRH(0x408A)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_RCNTR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

TIM1_RCNTRL(0x408B)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_RCNTR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM1_RCNTR	Count value of the Reload Timer for diode freewheeling masking and ZCP to phase commutation.

16.4.15 TIM1_ITRIP (0x4098, 0x4099)

TIM1_ITRIPH(0x4098)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_ITRIP[15:8]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
TIM1_ITRIPL(0x4099)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_ITRIP[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM1_ITRIP	Filtered Bus Current The hardware automatically samples the bus current and filters it for software application. The default channel is ADC channel 4. Range [0,32767]

16.4.16 TIM1_UCOP (0x408C, 0x408D)

TIM1_UCOPH(0x408C)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_UCOP[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM1_UCOPL(0x408D)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_UCOP[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description

[15:0]	TIM1_UCOP	Active Phase Voltage

16.4.17 TIM1_UFLP (0x408E, 0x408F)

TIM1_UFLPH(0x408E)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_UFLP[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM1_UFLPL(0x408F)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_UFLP[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM1_UFLP	Floating Phase Voltage

16.4.18 TIM1_URES (0x4090, 0x4091)

TIM1_URESH(0x4090)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_URES[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM1_URESL(0x4091)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_URES[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM1_URES	Voltage Calculation Result

16.4.19 TIM1_UIGN (0x4092, 0x4093)

TIM1_UIGNH(0x4092)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_UIGN[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM1_UIGNL(0x4093)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_UIGN[7:0]							

Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM1__UIGN	Ignored Voltage of Active Phase When the voltage of active phase is lower than TIM1__UIGN, the voltage is ignored.

16.4.20 TIM1_KF (0x4094, 0x4095)

TIM1_KFH(0x4094)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_KF[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM1_KFL(0x4095)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_KF[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM1_KF	Coefficient of the falling edge

16.4.21 TIM1_KR (0x4096, 0x4097)

TIM1_KRH(0x4096)								
Bit	15	14	13	12	11	10	9	8
Name	TIM1_KR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM1_KRL(0x4097)								
Bit	7	6	5	4	3	2	1	0
Name	TIM1_KR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM1_KR	Coefficient of the rising edge

16.4.22 EXT0 (0x40F0)

Bit	7	6	5	4	3	2	1	0
Name	RSV		FAEN	MOEMD2	T1COM_MD	RSV	TIM4_CT	EXT0_P11

Type	-	-	R/W	R/W	R/W	-	R/W	R/W
Reset	-	-	0	0	0	-	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5]	FAEN	After this feature is enabled, CMP_SAMR is scaled up by 4 times. 0: Disable 1: Enable
[4]	MOEMD2	10μs of MOE Cycle-by-cycle Current Limiting Enable (MOEMD must be configured as 1X) 0: Disable 1: Enable
[3]	T1COM_MD	Freewheeling Masking by ADC in Square-wave Control Mode 0: Disable. Freewheeling masking is not implemented by ADC. 1: Enable. Freewheeling masking is implemented by ADC (TIM1_CR1[BSEL] ≥ 1).
[2]	RSV	Reserved
[1]	TIM4_CT	DBG Function Switching 0: Reserved 1: P0.1
[0]	EXT0_P11	P1.1 INT0 Enable 0: Disable 1: Enable

17 Timer2

17.1 Timer2 Instructions

Timer2 has the following five working modes:

- Output mode: PWM generation
- Input capture mode: Detect the duration of high and low level of input PWM
- Input counter mode: Detect input time of the set PWM wave numbers
- QEP&RSD mode: Quadrature Encoder Pulse & Rotating State Detection (tailwind/headwind detection)
- Step Mode: Detect rotation direction, position and speed of step motor.

Timer2 features:

- 3-bit programmable prescaler divides the system clock
- 16-bit up-counting Basic Timer; Counting clock source serves as the output of prescaler
- 16-bit up/down-counting special timer for Input Counter Mode, QEP&RSD Mode, with external input signal selected as clock source
- Input filter module
- Edge detection module
- PWM generation module
- Interrupt event

17.1.1 Prescaler

Prescaler divides the system clock frequency and generates clock source for Basic Timer. 8 frequency division coefficients of prescaler are available and can be selected by TIM2_CR0[T2PSC]. Since this register has no buffer, the clock source frequency is updated immediately after TIM2_CR0[T2PSC] is written. Therefore, the frequency division coefficients shall be configured when Basic Timer is not working.

Clock source frequency formula:

$f_{CK\_CNT} = f_{CK\_PSC}$/TIM2_CR0[T2PSC]

When MCU clock rate is at 24MHz(41.67ns)

Table 17-1 Mapping between Clock Rate and TIM2_CR0[T2PSC]

TIM2_CR0[T2PSC]	Divider Factor	clk_psc2((Hz)	TIM2_CR0[T2PSC]	Divider Factor	clk_psc2(Hz)
000	0x01	24M	100	0x10	1.5M
001	0x02	12M	101	0x20	750k
010	0x04	6M	110	0x40	375k
011	0x08	3M	111	0x80	187.5k

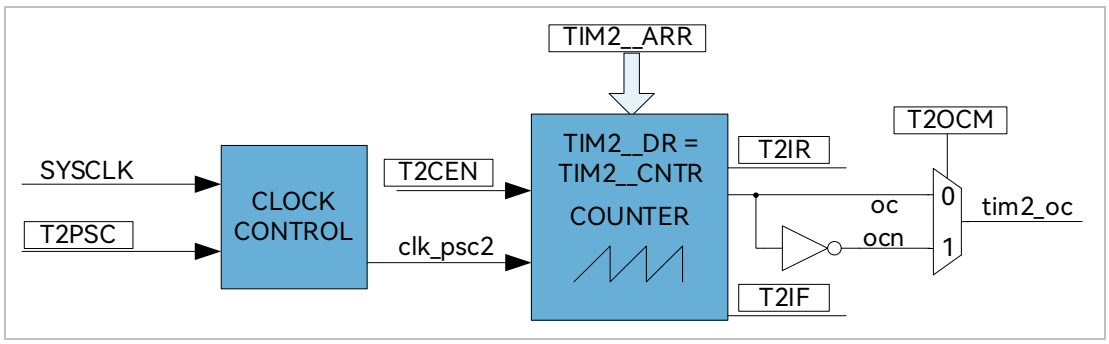
17.1.2 Reading, Writing and Counting of TIM2__CNTR

When TIM2_CR1[T2CEN] = 1, TIM2__CNTR starts to count. The write operation to TIM2__CNTR directly changes the value of the register, so Basic Timer shall be disabled before the write operation. When reading TIM2__CNTR, software reads the high-order bits first, and the hardware synchronously caches the low-order bits. When reading the low-order bits, the software reads the cached data.

17.1.3 Output Mode

When TIM2_CR0[T2MOD] = 01, Timer2 works in output mode.

Figure 17-1 Output Mode Block Diagram



The output mode generates output signals according to TIM2_CR0[T2OCM] and the comparison results from the comparator. Meanwhile, corresponding interrupts events are generated.

17.1.3.1 Reading and Writing of TIM2__ARR/TIM2__DR

In output mode, TIM2__ARR/TIM2__DR contains preload registers and shadow registers. When the software writes TIM2__ARR/TIM2__DR register, the data is saved in the preload register. When the overflow event TIM2_CR1[T2IF] is generated or the Basic Timer stops working (TIM2_CR1[T2CEN] = 0), the set value is

transferred to the shadow register.

TIM2_ARR/TIM2_DR is a 16-bit register, which requires to write the high byte first and then the low byte. The hardware ensures that the data in the preload register is not transferred to the shadow register after the high byte is written and before the low byte is written.

17.1.3.2 High-/Low-level Output Mode

When TIM2_CR0[T2OCM] = 0 and TIM2_DR = TIM2_ARR, the output signal (TIM2_OC) is always low. When TIM2_CR0[T2OCM] = 1 and TIM2_DR = TIM2_ARR, the output signal (TIM2_OC) is always high.

The output signal is always high/low only when TIM2_DR = TIM2_ARR. Configuring TIM2_DR = 0 generates a pulse of one clock cycle.

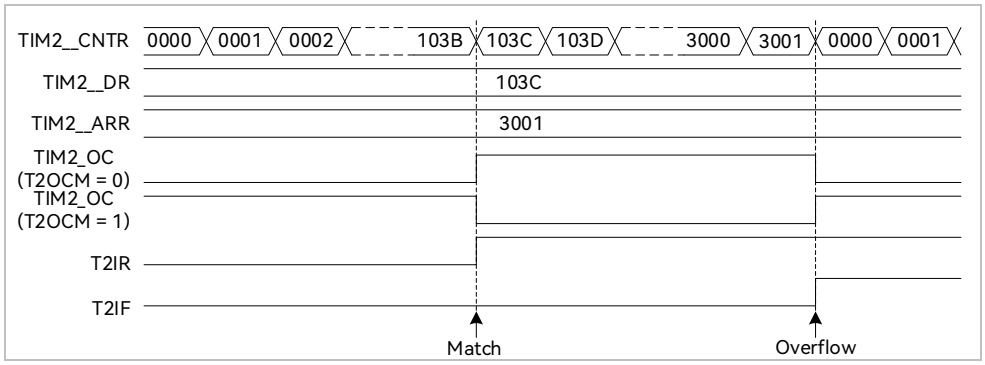
17.1.3.3 PWM Generation

In PWM generation mode, TIM2_ARR determines PWM cycle, TIM2_DR determines duty cycle, and duty cycle = TIM2_DR/TIM2_ARR*100%. If TIM2_CR0[T2OCM] = 0, the low level is output when TIM2_CNTR ≤ TIM2_DR, and the high level is output when TIM2_CNTR > TIM2_DR. If TIM2_CR0[T2OCM] = 1, the high level is output when TIM2_CNTR ≤ TIM2_DR, and the low level is output when TIM2_CNTR > TIM2_DR.

17.1.3.4 Interrupt Event

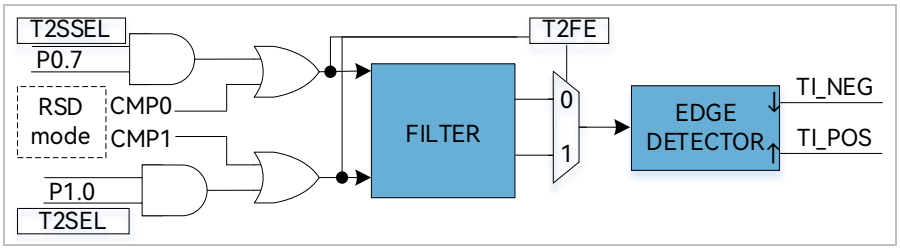
- When TIM2_CNTR = TIM2_DR, a compare match event is generated and the interrupt flag bit TIM2_CR1[T2IR] is set to “1”. The timer continues.
- When TIM2_CNTR = TIM2_ARR, an overflow event is generated, and the interrupt flag bit TIM2_CR1[T2IF] is set to “1”. The timer is cleared to “0” and then restarts.

Figure 17-2 Output Mode Waveform



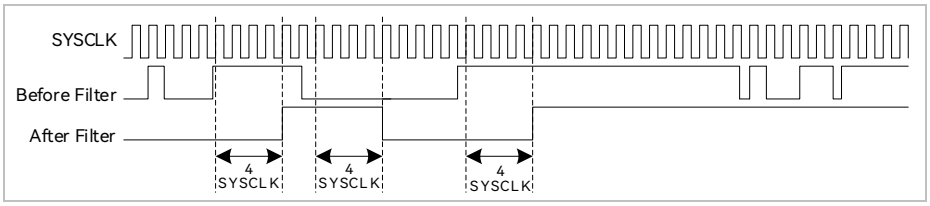
17.1.4 Input Signal Filtering and Edge Detection

Figure 17-3 Block Diagram of Input Signal Filtering and Edge Detection



The input signal of Timer2 comes from P0.7 or P1.0, set by PH_SEL[T2SSEL] or PH_SEL[T2SEL]. The filter of input signal is optional. The edge detection module detects filtered input signals and records rising edge and falling edge for use by the next module.

Figure 17-4 Timing Diagram of Filter Module

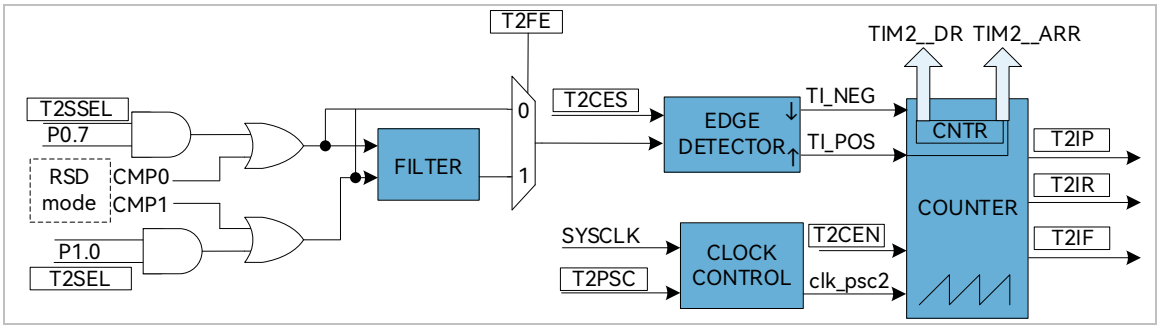


The filtering circuit removes the input noise with a pulse width of 4 clock cycles. The filtering feature is enabled when TIM2_CR1[T2FE] is set to “1”. The filtered signal is delayed by about 4~5 clock cycles.

17.1.5 Input Capture Mode

When TIM2_CR0[T2MOD] = 00, Timer2 works in input capture mode.

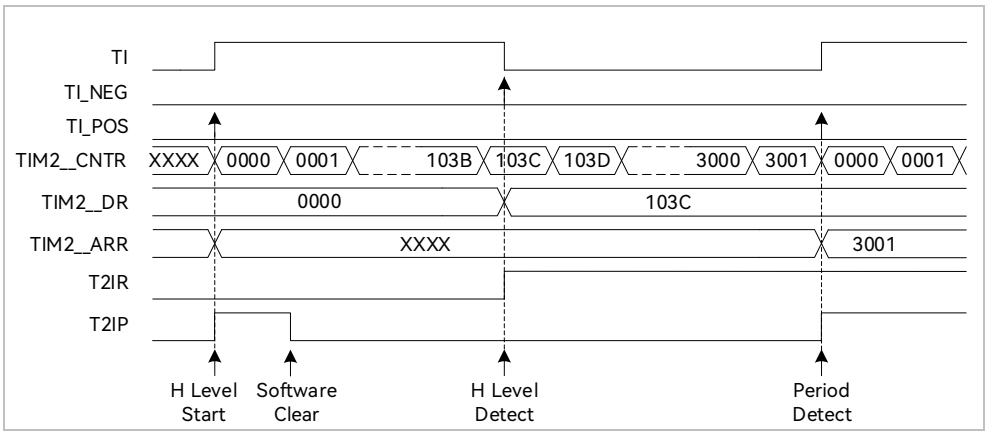
Figure 17-5 Schematic Diagram of Input Capture Mode



The input capture mode detects duty cycle and period of the PWM signal. When TIM2_CR0[T2CES] = 0, the time between two adjacent rising edges forms one cycle, and the time from rising edge to falling edge

forms the pulse width (HIGH). When TIM2_CR0[T2CES] = 1, the time between two adjacent falling edges forms one cycle, and the time from falling edge to rising edge forms the pulse width (LOW). When the predefined edge arrives, the count value TIM2__CNTR is stored in TIM2__DR and TIM2__ARR respectively. The filter of input signal is optional.

Figure 17-6 Timing Diagram of Input Capture Mode (TIM2_CR0[T2CES] = 0)



For example, when TIM2_CR0[T2CES] = 0, TIM2_CR1[T2CEN] is set to “1” to enable the Basic Timer. When the first rising edge of the input (falling edge is invalid) is detected, TIM2__CNTR is cleared and restarts.

When falling edge of the input is detected, the value of TIM2__CNTR is stored in TIM2__DR, and the interrupt flag TIM2_CR1[T2IR] is set to “1”, and TIM2__CNTR continues to count.

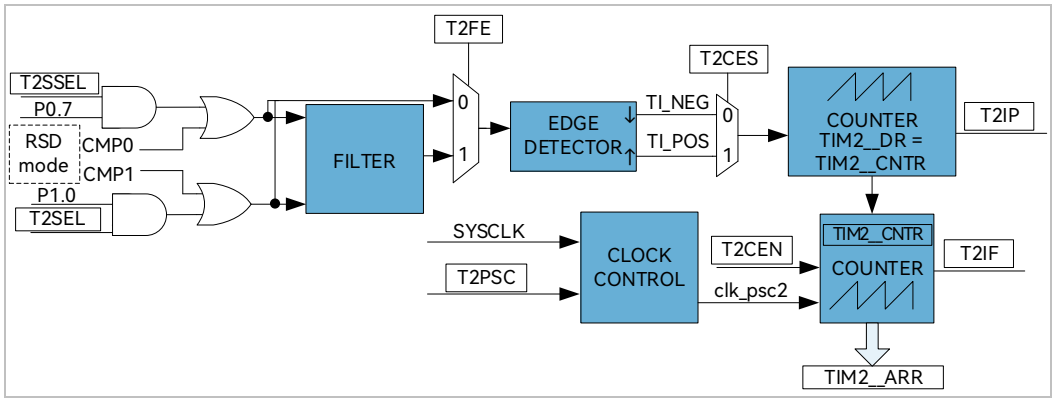
When the second rising edge of input is detected, the value of TIM2__CNTR is stored in TIM2__ARR. Meanwhile, the interrupt flag TIM2_CR1[T2IP] is set to “1”, and TIM2__CNTR is cleared to “0” and restarts.

An overflow event occurs if Timer2 does not detect the second rising edge of the input and TIM2__CNTR reaches 0xFFFF. In this case, the interrupt flag TIM2_CR1[T2IF] is set to “1”, and TIM2__CNTR is cleared to “0” and restarts.

17.1.6 Input Counter Mode

When TIM2_CR0[T2MOD] = 10, Timer2 works in input counter mode.

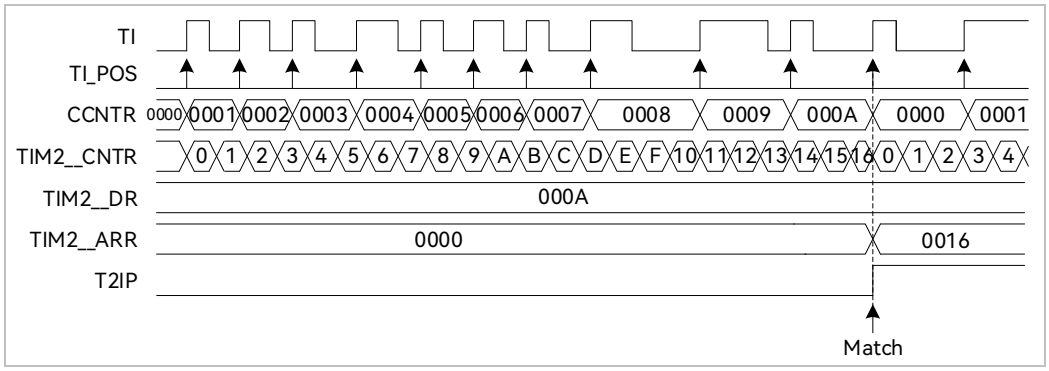
Figure 17-7 Schematic Diagram of Input Counter Mode



In input counter mode, TIM2__DR includes preload register and shadow register. When the software writes TIM2__DR register, the data is saved in the preload register first, and then sent to the shadow register in case of compare match event (TIM2_CR1[T2IP] = 1), overflow event (TIM2_CR1[T2IF] = 1) or timer disable (TIM2_CR1[T2CEN] = 0). TIM2__DR is a 16-bit register, which requires the software writes the high byte first and then the low byte. The hardware ensures that the data in the preload register is not updated to the shadow register after the high byte is written and before the low byte is written.

The input counter mode is used to detect the time to input the set PWM wave. In this mode, TIM2__CNTR of the Basic Timer is stored in TIM2__ARR. The filter of input signal is optional. When TIM2_CR0[T2CES] is set to “1”, the rising edge of the input PWM signal serves as the active counting edge of the special timer; when TIM2_CR0[T2CES] is set to “0”, the falling edge of the input signal as the active edge.

Figure 17-8 Timing Diagram of Input Counter Mode



The Basic Timer is enabled when TIM2_CR1[T2CEN] is set to “1”. If the first active edge of the input signal is detected, TIM2__CNTR is cleared to “0” and restarts.

Whenever active edge of the input signal arrives, one is added to the count value of the special timer CCNTR.

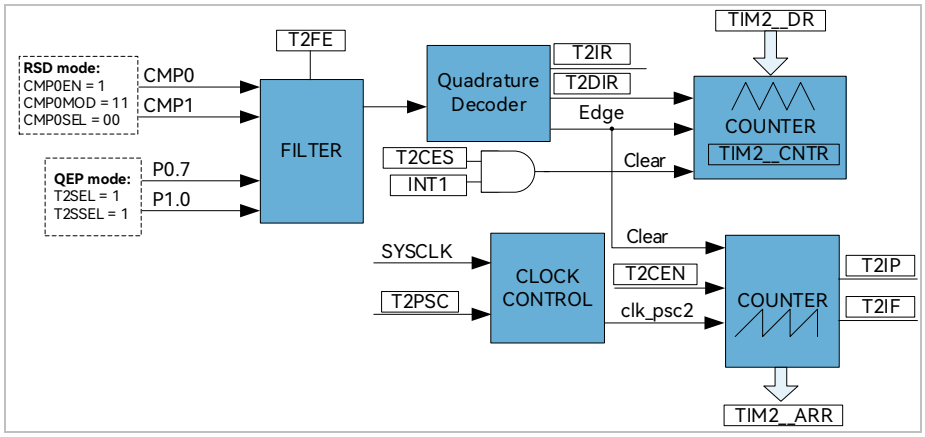
When the count value reaches TIM2__DR, TIM2__CNTR is stored in TIM2__ARR. When TIM2_CR1[T2IP] is set to “1”, TIM2__CNTR and CCNTR are cleared to “0” and restart.

When the number of input PWM does not reach the set value and TIM2__CNTR reaches 0xFFFF, an overflow event occurs, and the interrupt flag TIM2_CR1[T2IF] is set to “1”. TIM2__CNTR is cleared to “0” with CCNTR uncleared. TIM2__CNTR starts counting from 0, and CCNTR continues counting with the previous value.

17.1.7 QEP&RSD Mode

When TIM2_CR0[T2MOD] = 11, Timer2 works in QEP&RSD mode.

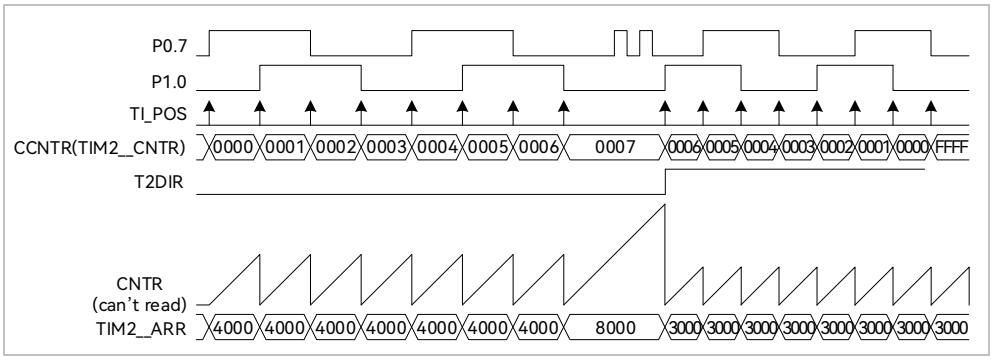
Figure 17-9 Schematic Diagram of QEP&RSD Mode



QEP&RSD mode obtains relative position, direction and speed of the motor by detecting orthogonal signals on two channels. P0.7 and P1.0 (QEP mode. Two inputs generally differ in phase by 90 degrees) or CMP0 and CMP1 (RSD mode. Two inputs generally differ in phase by 60 degrees) are the input signal sources, which are sent to the quadrature decoding module from the filtering module to obtain active edge and direction (TIM2_CR1[T2DIR]). TIM2_CR1[T2IF] interrupt flag is generated when the direction changes.

Figure 17-10 Timing Diagram of QEP&RSD Mode

(Phases of Orthogonal Signals in RSD Mode Different from those in QEP Mode)



The special timer is an up/down-counting timer, and the signal source is the active edge from orthogonal decoding module. If TIM2_CR1[T2DIR] = 0, the direction is positive, and special timer counts up. When the active edge arrives, the timer increases by one. If TIM2_CR1[T2DIR] = 1, the direction is reverse and special timer counts down. When the active edge arrives, the timer decreases by one.

The special timer can be cleared by external interrupt INT1. After mechanical zero of the encoder is connected with any port of INT1, INT1 interrupt is enabled, TIM2_CR0[T2CES] = 1 and INT1 is detected,

- When TIM234_CTRL[TIM2_DR_SEL] = 1, the special timer is cleared to “0”. If the timer reaches TIM2__DR from 0, it is automatically cleared to “0”. If the timer decreases from TIM2__DR to 0, it is automatically set to TIM2__DR. TIM2__CNTR is read to obtain the value of special timer.
- When TIM234_CTRL[TIM2_DR_SEL] = 0, the special timer is cleared to “0”, and the value held by the timer is stored into TIM2__DR. If the timer reaches 65535 from 0, it is automatically cleared to “0”. If the timer decreases from 65535 to 0, it is automatically set to 65535. TIM2__CNTR is read to obtain the value of special timer.

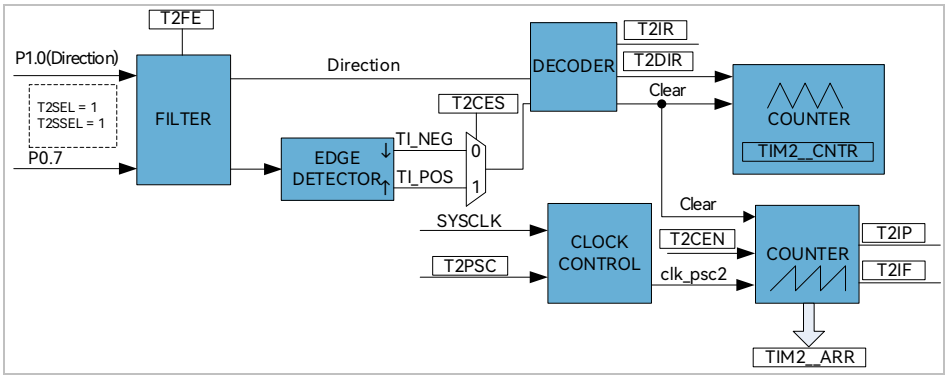
The Basic Timer is an up-counting timer, which uses the output of prescaler as the clock source to record the time between two active counting edges. When active counting edge arrives, the value of Basic Timer is stored in TIM2__ARR and then cleared to “0”, and TIM2_CR1[T2IP] interrupt flag bit is set to “1”. When Basic Timer counts to 0xFFFF, the count overflows and (TIM2_CR1[T2IF]) interrupt flag is generated.

17.1.7.1 RSD Comparator Sampling

See section 31.1.4.

17.1.8 Step Mode

Figure 17-11 Step Mode Schematic Diagram

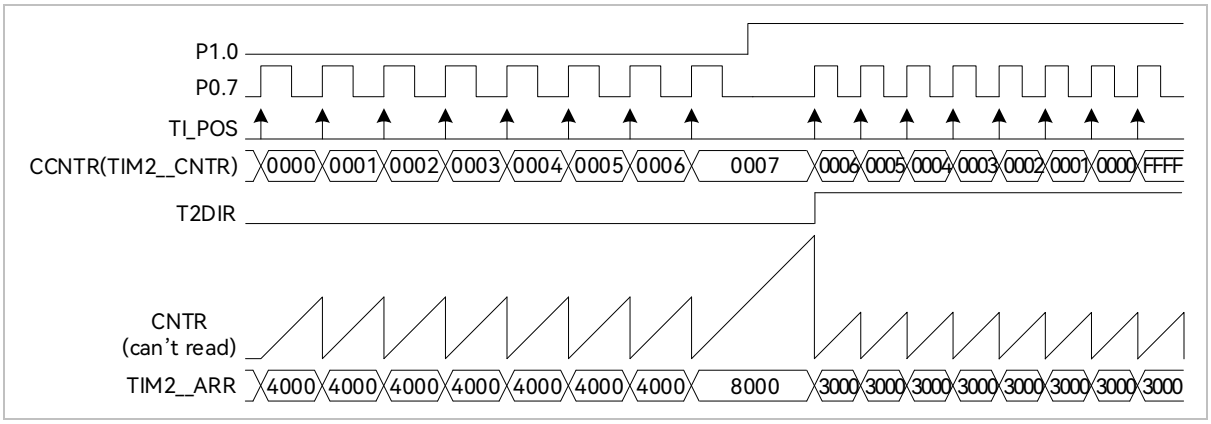


In step mode, relative position, direction and speed of the step motor are obtained by detecting inputs of two channels. P1.0 is direction input, and P0.7 is pulse input. Setting TIM2_CR0[T2CES] to select the rising edge or falling edge as the active edge. The input signals are sent to decoding module from the filtering module to obtain the active edge and direction TIM2_CR1[T2DIR]. TIM2_CR1[T2IF] interrupt flag is generated when the direction changes.

Note

TIM2_CR1[T2IR] and TIM2_CR1[T2DIR] will not change unless transition occurs at P1.0 and active edge is detected at P0.7. To generate an interrupt immediately after P1.0 changes, use INT1

Figure 17-12 Timing Diagram of Step Mode



The special timer is an up/down-counter, and the signal source is active edge of the encoding module. When P1.0 = 0 and TIM2_CR1[T2DIR] = 0, the direction is forward. If active edge of P0.7 arrives, the special timer increases by 1. When P1.0 = 1 and TIM2_CR1[T2DIR] = 1, the direction is reverse. If active edge of P0.7 arrives, the special timer decreases by 1. If count value of the special timer reaches 65535 from 0, it is automatically cleared to "0". If it decreases from 65535 to 0, it is automatically set to 65535. TIM2__CNTR is read to obtain the value of special timer.

The Basic Timer is an up counter, which uses the output of prescaler as the clock source to record the time between two active counting edges. When active counting edge arrives, the value of Basic Timer is stored in TIM2__ARR and then cleared to "0", and TIM2_CR1[T2IP] interrupt flag bit is set to "1". When Basic Timer counts to 0xFFFF, the count overflows and (TIM2_CR1[T2IF]) interrupt flag is generated.

17.2 Timer2 Registers

17.2.1 TIM2_CR0 (0xA1)

Bit	7	6	5	4	3	2	1	0
Name	T2PSC			T2OCM	T2IRE	T2CES	T2MOD	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:5]	T2PSC	Basic Timer Clock Prescaler Selection It is configured to divide the system clock frequency and generate the clock source for Basic Timer. When MCU clock runs at 24MHz(41.67ns), the prescaled clock rates are configured as follows: 000: 0x1 (24MHz) 001: 0x2 (12MHz) 010: 0x4 (6MHz) 011: 0x8 (3MHz) 100: 0x10 (1.5MHz) 101: 0x20 (750kHz) 110: 0x40 (375kHz) 111: 0x80 (187.5kHz)
[4]	T2OCM	Output Mode: Compare Mode Selection 0: “0” is output when TIM2_CNTR ≤ TIM2_DR; “1” is output when TIM2_CNTR > TIM2_DR. 1: “1” is output when TIM2_CNTR ≤ TIM2_DR; “0” is output when TIM2_CNTR > TIM2_DR. Input Counter Mode: No effect Input Capture Mode: No effect QEP&RSD Mode or Step Mode Selection 0: QEP&RSD Mode 1: Step Mode
[3]	T2IRE	Output Mode: Compare Match Interrupt Enable Input Capture Mode: Pulse Width Detection Interrupt Enable Input Counter Mode: No effect QEP &RSD Mode or Step Mode: Direction Change Interrupt Enable 0: Disable 1: Enable
[2]	T2CES	Output: No effect Input Capture Mode: Counting Edge Selection 0: The time between two adjacent raising edges forms one cycle, and the time from rising edge to falling edge forms the pulse width (HIGH). 1: The time between two adjacent falling edges forms one cycle, and the time from falling edge to raising edge forms the pulse width (LOW). Input Counter Mode: Active Edge Selection

		0: Falling Edge Count 1: Rising Edge Count QEP&RSD Mode: Pulse Counter Cleared Enable upon INT1 (Zero Point) 0: Disable 1: Enable
[1:0]	T2MOD	Mode Selection 00: Input Capture Mode 01: Output Mode 10: Input Counter Mode 11: QEP&RSD Mode or Step Mode

17.2.2 TIM2_CR1 (0xA9)

Bit	7	6	5	4	3	2	1	0
Name	T2IR	T2IP	T2IF	T2IPE	T2IFE	T2FE	T2DIR	T2CEN
Type	R/W0	R/W0	R/W0	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	T2IR	Output Mode: Compare Match Interrupt Flag This bit is set to “1” by the hardware when TIM2__CNTR matches TIM2__DR. Input Capture Mode: Pulse Width Detection Interrupt Flag This bit is set to “1” when an input pulse width is detected (Setting TIM2_CR0[T2CES] to select the rising edge or falling edge as the active edge). Input Counter Mode: No effect QEP&RSD Mode or Step Mode: Direction Change Flag Bit Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[6]	T2IP	Output Mode: No effect Input Capture Mode: PWM Cycle Detection Interrupt Flag This bit is set to “1” when an input PWM cycle is detected (Setting TIM2_CR0[T2CES] to select the rising edge or falling edge as the active edge). Input Counter Mode: PWM Input Counter Match Interrupt Flag This bit is set to “1” by hardware when the number of input PWM reaches TIM2__DR. QEP&RSD Mode or Step Mode: Active Edge Detection Interrupt Flag This bit is set to “1” by hardware when the input edge is detected as an active edge. Read:

		0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[5]	T2IF	Output Mode: Timer Overflow Interrupt Flag. This bit is set to “1” by hardware when TIM2_CNTR matches TIM2_ARR. Input Capture Mode: Timer Overflow Interrupt Flag Set TIM2_CR0[T2CES] to select the rising edge or falling edge as the active edge. This bit is set to “1” and TIM2_CNTR is cleared to “0” when the Timer has not detected an input PWM cycle but the timer TIM2_CNTR reaches 0xFFFF (overflow occurs). Input Counter Mode: Basic Timer Overflow Interrupt Flag This bit is set to “1” by hardware when the input PWM cycle has not reached the preset TIM2_DR value but Basic Timer TIM2_CNTR value reaches 0xFFFF (overflow occurs). QEP&RSD Mode or Step Mode: Basic Timer Overflow Interrupt Flag This bit is set to “1” by hardware when Basic Timer reaches to 0xFFFF (overflow occurs). Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[4]	T2IPE	Output Mode: No effect Input Capture Mode: PWM Cycle Detection Interrupt Enable Input Counter Mode: PWM Input Counter Match Interrupt Enable QEP&RSD Mode or Step Mode: Active Edge Detection Interrupt Enable 0: Disable 1: Enable
[3]	T2IFE	Output Mode: Timer Overflow Interrupt Enable Input Capture Mode: Timer Overflow Interrupt Enable Input Counter Mode: Basic Timer Overflow Interrupt Enable QEP&RSD Mode and Step Mode: Basic Timer Overflow Interrupt Enable 0: Disable 1: Enable
[2]	T2FE	Input Signal Filter Selection 0: Disable 1: Enable
[1]	T2DIR	QEP&RSD Mode: Indicator of Motor Rotation Direction Indicates the motor rotation direction based on the phase relationship of the two input signals.

		Step mode: Motor rotation direction Indiicates motor rotation direction according to direction signal (P1.0) 0: Forward 1: Backward
[0]	T2CEN	Timer Enable 0: Disable 1: Enable

17.2.3 PI_LPF_CR (0Xf9)

Bit	7	6	5	4	3	2	1	0
Name	T2SS	RSV				PIRANGE	PISTA	LPFSTA
Type	R/W	-	R/W	R/W	R/W	R/W	R	R/W
Reset	0	-	0	0	0	0	0	0

Bit	Name	Description
[7]	T2SS	Timer2 Step Motor Input Mode 0: P1.0 as direction and P0.7 as pulse count 1: P1.0 as reverse pulse count, P0.7 as forward pulse count.
[6]	RSV	Reserved
[5]	T2IF	Output Mode: Timer Overflow Interrupt Flag. This bit is set to “1” by hardware when TIM2_CNTR matches TIM2_ARR. Input Capture Mode: Timer Overflow Interrupt Flag Set TIM2_CR0[T2CES] to select the rising edge or falling edge as the active edge. This bit is set to “1” and TIM2_CNTR is cleared to “0” when the Timer has not detected an input PWM cycle but the timer TIM2_CNTR reaches 0xFFFF (overflow occurs). Input Counter Mode: Basic Timer Overflow Interrupt Flag This bit is set to “1” by hardware when the input PWM cycle has not reached the preset TIM2_DR value but Basic Timer TIM2_CNTR value reaches 0xFFFF (overflow occurs). QEP&RSD Mode or Step Mode: Basic Timer Overflow Interrupt Flag This bit is set to “1” by hardware when Basic Timer reaches to 0xFFFF (overflow occurs). Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[2:0]		See 12.3.1

17.2.4 TIM2_CNTR (0xAA, 0xAB)

TIM2_CNTRH(0xAB)								
Bit	15	14	13	12	11	10	9	8
Name	TIM2_CNTR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM2_CNTRL(0xAA)								
Bit	7	6	5	4	3	2	1	0
Name	TIM2_CNTR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM2_CNTR	Output Mode/Input Capture Mode/Input Counter Mode: Count values held in the Basic Timer QEP&RSD Mode or Step Mode: Count values held in the special timer When TIM2_CNTR is 0xFFFF, this bit is automatically cleared to “0”.

17.2.5 TIM2_DR (0xAC, 0xAD)

TIM2_DRH(0xAD)								
Bit	15	14	13	12	11	10	9	8
Name	TIM2_DR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM2_DRL(0xAC)								
Bit	7	6	5	4	3	2	1	0
Name	TIM2_DR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM2_DR	Output Mode: Compare and match value (written by software) Input Capture Mode: Count value of the detected input pulse width based on TIM2_CR0[T2CES] (written by hardware) Input Counter Mode: PWM cycles to be counted (written by software) QEP&RSD Mode: Value of the special timer when TIM2_CR0[T2CES] = 1 and INT1 (zero point) is detected (written by hardware) Step Mode: No effect

17.2.6 TIM2_ARR (0xAE, 0xAF)

TIM2_ARRH(0xAF)								
Bit	15	14	13	12	11	10	9	8
Name	TIM2_ARR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIM2_ARRL(0xAE)								
Bit	7	6	5	4	3	2	1	0
Name	TIM2_ARR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIM2_ARR	Output Mode: Overload value (written by software) Input Capture Mode: Count value of a PWM cycle (written by hardware) Input Counter Mode: Count value held in Basic Timer when the input PWM count matches (written by hardware) QEP&RSD Mode or Step Mode: Count value held in Basic Timer when the input signal is detected as an active edge (written by hardware)

18 Timer3/Timer4

18.1 Timer3/Timer4 Instructions

Timer3/Timer4 supports output and input modes:

- Output mode: Generate PWM waveform (single mode)
- Input capture mode: Detect the duration of high and low level of input PWM, which can be used to calculate PWM duty cycle

Timer3/Timer4 includes:

- 3-bit programmable prescaler divides system clock as the clock source for Basic Timer
- 16-bit up-counting Basic Timer; The output of the prescaler serves as the counting clock source
- Input filtering module
- Edge detection Module
- Output module generates PWM signal and outputs single compare results
- Interrupt event

18.1.1 Prescaler

Prescaler divides the system clock frequency and generates counter clock source for Basic Timer. 8 frequency division coefficients of prescaler are available and can be selected by TIMx_CR0[TxPSC]. Since this register has no buffer, the clock source frequency is updated immediately after TIMx_CR0[TxPSC] is written. Therefore, the frequency division coefficients shall be configured when Basic Timer is not working.

The clock source frequency formula:

$f_{CK\_CNT}=f_{CK\_PSC}$/TIMx_CR0[TxPSC]

When system clock runs at 24MHz(41.67ns):

Table 18-1 Relationship between Clock Source Frequency and TIMx_CR0[TxPSC] after Division

TIMx_CR0[TxPSC]	Divider Factor	clk_pscx(Hz)	TIMx_CR0[TxPSC]	Divider Factor	clk_pscx(Hz)
000	0x01	24M	100	0x10	1.5M
001	0x02	12M	101	0x20	750k

TIMx_CR0[TxPSC]	Divider Factor	clk_pscx(Hz)	TIMx_CR0[TxPSC]	Divider Factor	clk_pscx(Hz)
010	0x04	6M	110	0x40	375k
011	0x8	3M	111	0x80	187.5k

Note

In Input Capture Mode of Timer3, the clock rate is 48MHz when TIM234_CTRL[0] is set to “1”

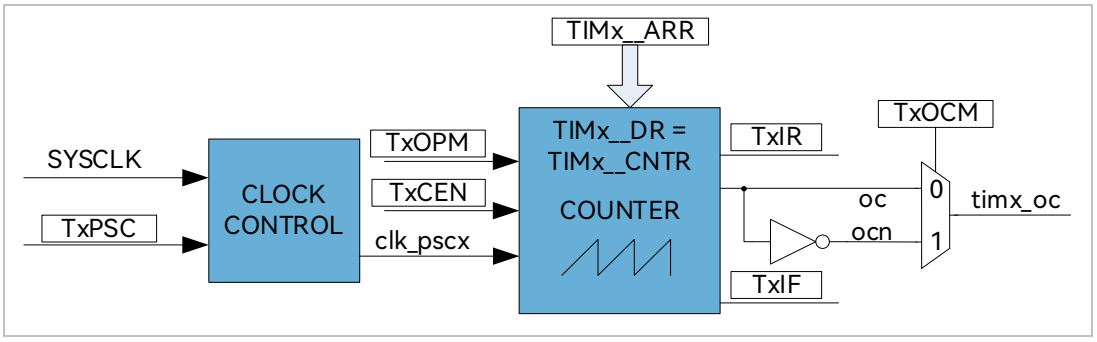
18.1.2 Reading, Writing and Counting of TIMx_CNTR

TIMx_CNTR starts when TIMx_CR1[TxEN] = 1. The write operation to TIMx_CNTR directly changes the value of the register, so it is required to disable the timer before the write operation. When reading TIMx_CNTR, the software reads high-order bits first and then low-order bits, and the hardware caches the low-order bits simultaneously. When reading the low-order bits, the software reads the cached data.

18.1.3 Output Mode

When TIMx_CR0[TxMOD] = 1, Timer3/4 works in output mode.

Figure 18-1 Output Mode Block Diagram



The output mode generates output signals according to TIMx_CR0[TxOCM] and the comparison results from the comparator. Meanwhile, corresponding interrupts is generated.

18.1.3.1 High-/Low-level Output Mode

When TIMx_CR0[TxOCM] = 0 and TIMx_DR = TIMx_ARR, the output signals (TIMx_OC) are always low. When TIMx_CR0[TxOCM] = 1 and TIMx_DR = TIMx_ARR, the output signals (TIMx_OC) are always high.

The output signal is always high/low only when TIMx_DR = TIMx_ARR. Configuring TIMx_DR = 0 generates a pulse of one clock cycle.

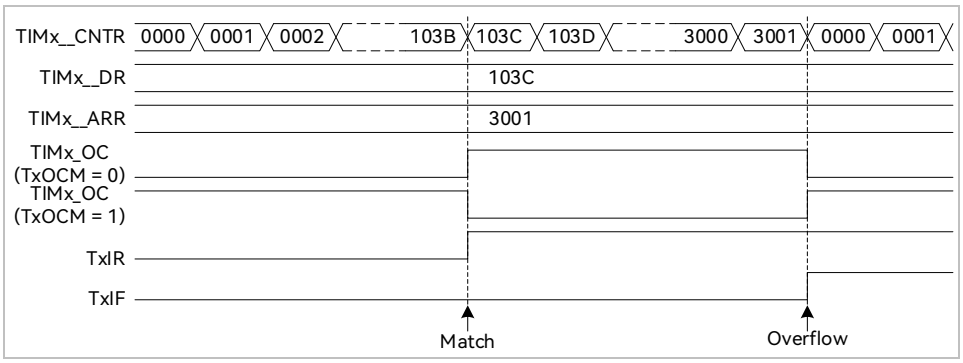
18.1.3.2 PWM Generation

In PWM generation mode, TIMx_ARR determines PWM cycle, and TIMx_DR determines the duty cycle, and duty cycle = TIMx_DR/TIMx_ARR*100%. If TIMx_CR0[TxOCM] = 0, the low level is output when TIMx_CNTR ≤ TIMx_DR, and the high level is output when TIMx_CNTR > TIMx_DR. If TIMx_CR0[TxOCM] = 1, the high level is output when TIMx_CNTR ≤ TIMx_DR, and low level is output when TIMx_CNTR > TIMx_DR.

18.1.3.3 Interrupt Event

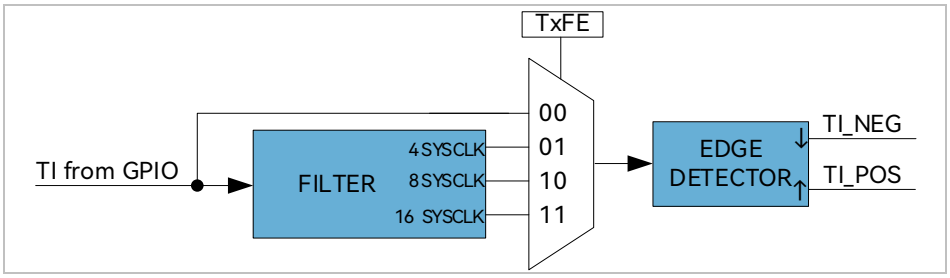
- When TIMx_CNTR = TIMx_DR, a compare match interrupt is generated. The interrupt flag TIMx_CR1[TxIR] is set to “1”, and the timer continues.
- When TIMx_CNTR = TIMx_ARR, an overflow event is generated. The interrupt flag TIMx_CR1[TxIF] is set to “1”, and the timer is cleared to “0”. TIMx_CR0[TxOPM] determines whether the timer recounts. The timer stops when TIMx_CR0[TxOPM]= 1, and restarts when TIMx_CR0[TxOPM]= 0.

Figure 18-2 Output Waveform of Output Mode



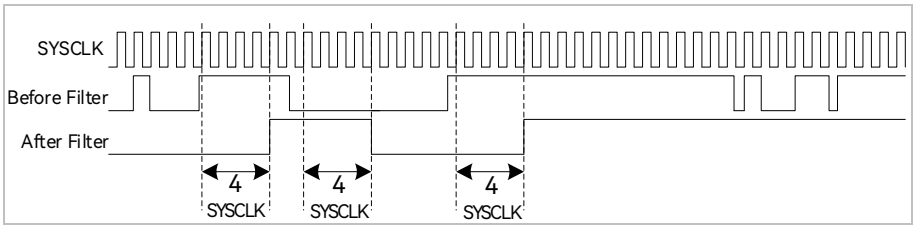
18.1.4 Input Signal Filtering and Edge Detection

Figure 18-3 Block Diagram of Input Signal Filtering and Edge Detection



The input signal TI of Timer3/Timer4 comes from P1.1/P0.1. The filter of input signal is optional. The edge detection module detects filtered input signals and records rising edge and falling edge for the next module.

Figure 18-4 4clk Timing Diagram of Filter Module

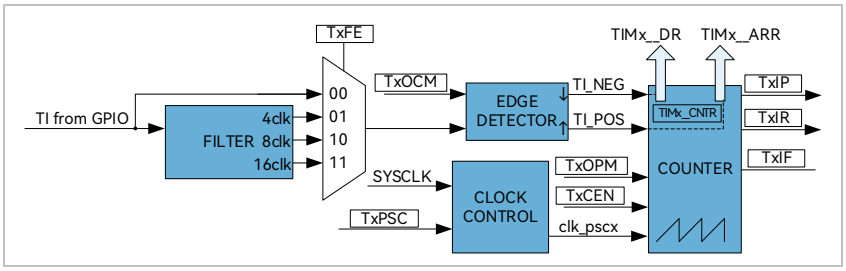


The filtering circuit removes the input noise with a pulse width of 4/8/16 clock cycles. The filtering feature is enabled when TIMx_CR1[TxFE] = 01/10/11. The filtered signal is delayed by about 4 ~ 5/8 ~ 9/16 ~ 17 clock cycles.

18.1.5 Input Capture Mode

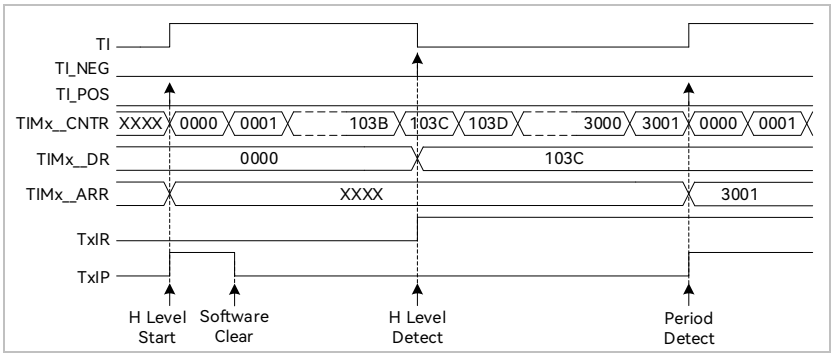
When TIMx_CR0[TxMOD] = 0, Timer3 works in input capture mode.

Figure 18-5 Schematic Diagram of Input Capture Mode



The Input Capture Mode detects pulse width and waveform period of the input PWM signals. When TIMx_CR0[TxOCM] = 0, the time between two adjacent rising edges forms one cycle, and the time from rising edge to falling edge forms the pulse width (HIGH). When TIMx_CR0[TxOCM] = 1, the time between two adjacent falling edges forms one cycle, and the time from falling edge to rising edge forms the pulse width (LOW). The pulse width and the period obtained by TIMx__CNTR are stored in TIMx__DR and TIMx__ARR respectively. The filter of input signal is optional.

Figure 18-6 Timing Diagram of Input Capture Mode (TIMx_CR0[TxOCM] = 0)



For example, when TIMx_CR0[TxOCM]= 0, TIMx_CR1[TxEN] is set to “1” to enable the timer.

When the falling edge is detected, the value of TIMx__CNTR is stored into TIMx__DR. Meanwhile, the interrupt flag TIMx_CR1[TxIR] is set to “1”, and TIMx__CNTR continues to count.

When the second rising edge is detected, the value of TIMx__CNTR is saved into TIMx__ARR. The interrupt flag TIMx_CR1[TxIP] is set to “1” and TIMx__CNTR is cleared to “0”. TIMx_CR0[TxOPM] determines whether the timer restarts. If TxOPM = 1, the timer stops; and if TxOPM = 0, it restarts.

An overflow event occurs if Timer3/Timer4 does not detect the second rising edge of the input and TIMx__CNTR reaches 0xFFFF. In this case, the interrupt flag bit TIMx_CR1[TxIF] is set to “1”, and TIMx__CNTR is cleared to “0”. TIMx_CR0[TxOPM] determines whether the timer restarts. If TxOCM= 1, the timer stops counting, and if TxOPM = 0, it restarts.

18.1.6 FG Generation (Timer4)

See section FG Generation.

18.2 Timer3/Timer4 Registers

18.2.1 TIMx_CR0 (0x9C/0x9E) (x = 3/4)

Bit	7	6	5	4	3	2	1	0
Name	TxPSC			TxOCM	TxIRE	RSV	TxOPM	TxMOD
Type	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W
Reset	0	0	0	0	0	-	0	0

Bit	Name	Description
[7:5]	TxPSC	Basic Timer Clock Prescaler Selection It is configured to divide the system clock frequency and generate the clock source for Basic Timer. When MCU clock runs at 24MHz(41.67ns), the prescaled clock rates are configured as follows: 000: 0x1 (24MHz) 001: 0x2 (12MHz) 010: 0x4 (6MHz) 011: 0x8 (3MHz) 100: 0x10 (1.5MHz) 101: 0x20 (750kHz) 110: 0x40 (375kHz) 111: 0x80 (187.5kHz)
[4]	TxOCM	Output Mode: Compare Mode Selection 0: “0” is output when TIMx__CNTR ≤ TIMx__DR; “1” is output when TIMx__CNTR > TIMx__DR. 1: “1” is output when TIMx__CNTR ≤ TIMx__DR; “0” is output when TIMx__CNTR >

		TIMx_DR. Input Capture Mode: Active Edge Selection 0: The time between two adjacent raising edges forms one cycle, and the time from rising edge to falling edge forms the pulse width (HIGH). 1: The time between two adjacent falling edges forms one cycle, and the time from falling edge to raising edge forms the pulse width (LOW).
[3]	TxIRE	Output Mode: Compare Match Interrupt Enable Input Capture Mode: Pulse Width Detection Interrupt Enable Input Counter Mode: No effect 0: Disable 1: Enable
[2]	RSV	Reserved
[1]	TxOPM	Single Mode The timer stops in any of the following events: Output Mode: Timer overflow event Input Capture Mode: PWM Cycle Detection or Timer Overflow Event 0: The Timer does not stop 1: The Timer stops (TIMx_CR1[TxEN] is reset to “0”)
[0]	TxMOD	Working Mode Selection 0: Input Capture Mode 1: Output Mode

18.2.2 TIMx_CR1 (0x9D/0x9F) (x = 3/4)

Bit	7	6	5	4	3	2	1	0
Name	TxIR	TxIP	TxIF	TxIPE	TxIFE	TxFE		TxEN
Type	R/W0	R/W0	R/W0	R/W0	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	TxIR	Output Mode: Compare Match Interrupt Flag This bit is set to “1” by the hardware when TIMx_CNTR matches TIMx_DR. It is cleared to “0” by software. Input Capture Mode: Pulse Width Detection Interrupt Flag This bit is set to “1” when an input pulse width is detected (Setting TIMx_CR0[TxOCM] to select the rising edge or falling edge as the active edge). This bit is cleared to “0” by software. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect

[6]	TxIP	Output Mode: No effect Input Capture Mode: PWM Cycle Detection Interrupt Flag This bit is set to “1” when an input PWM cycle is detected (Setting TIMx_CR0[TxOCM] to select the rising edge or falling edge as the active edge). It is cleared to “0” by software. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[5]	TxIF	Output Mode: Timer Overflow Interrupt Flag. This bit is set to “1” and TIMx_CNTR is cleared to “0” when TIMx_CNTR matches TIMx_ARR. It is cleared to “0” by software. Input Capture Mode: Timer Overflow Interrupt Flag This bit is set to “1” and TIMx_CNTR is cleared to “0” when the timer does has not detected an input PWM cycle but the timer TIMx_CNTR reaches 0xFFFF (overflow occurs). It is cleared to “0” by software. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[4]	TxIPE	Output Mode: No effect Input Capture Mode: PWM Cycle Detection Interrupt Enable 0: No interrupt pending 1: Interrupt pending
[3]	TxIFE	Output Mode: Timer Overflow Interrupt Input Capture Mode: Timer Overflow Interrupt Enable 0: No interrupt pending 1: Interrupt pending
[2:1]	TxFE	Input Signal Filtering Pulse Width Selection Input signals are filtered as noise if pulse width is less than the defined value. Assuming that MCU clock runs at 24MHz(41.67ns): 00: Disable 01: 4 system clock cycles, 4 x 41.67ns 10: 8 system clock cycles, 8 x 41.67ns 11: 16 system clock cycles, 16 x 41.67ns
[0]	TxEN	Basic Timer Enable 0: Disable 1: Enable

18.2.3 TIMx_CNTR (0xA2, 0xA3/0x92, 0x93) (x = 3/4)

TIMx_CNTRH(0xA3/0x93)								
Bit	15	14	13	12	11	10	9	8
Name	TIMx_CNTR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIMx_CNTRL(0xA2/0x92)								
Bit	7	6	5	4	3	2	1	0
Name	TIMx_CNTR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIMx_CNTR	Count Values Held in Basic Timer When TIMx_CNTR reaches 0xFFFF, this bit is automatically cleared to “0”.

18.2.4 TIMx_DR (0xA4, 0xA5/0x94, 0x95) (x = 3/4)

TIMx_DRH(0xA5/0x95)								
Bit	15	14	13	12	11	10	9	8
Name	TIMx_DR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIMx_DRL(0xA4/0x94)								
Bit	7	6	5	4	3	2	1	0
Name	TIMx_DR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIMx_DR	Output Mode: Compare match values (written by software) Input Capture Mode: Count value of the detected input pulse width based on TIMx_CR0[TxOCM] (written by hardware)

18.2.5 TIMx_ARR (0xA6, 0xA7/0x96, 0x97) (x = 3/4)

TIMx_ARRH(0xA7/0x97)								
Bit	15	14	13	12	11	10	9	8
Name	TIMx_ARR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
TIMx_ARRL(0xA6/0x96)								

Bit	7	6	5	4	3	2	1	0
Name	TIMx_ARR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	TIMx_ARR	Output Mode: Overload value (written by software) Input Capture Mode: Count value of a PWM cycle based on TIMx_CR0[TxOCM] (written by hardware)

19 Systick

19.1 Systick Instructions

The chip can generate Systick interrupts at a fixed interval, and the interrupt cycle is controlled by SYST_ARR. Systick interrupt is enabled when DRV_SR[SYSTIE] is set to “1” for the descriptions on the register DRV_SR), and the interrupt entry is accessed by 10 (multiplexed with Timer4 interrupt input).

19.2 Systick Registers

19.2.1 DRV_SR (0x4061)

SYST_ARRH(0x4064)								
Bit	15	14	13	12	11	10	9	8
Name	SYSTIF	SYSTIE	FGIF	DCIF	FGIE	DCIP	DCIM	
Type	R/W0	R/W	R/W0	R/W0	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bit	Name	Description
[7]	SYSTIF	Systick Interrupt Flag Bit Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[6]	SYSTIE	Systick Interrupt Enable 0: Disable 1: Enable
[5:0]		See 0.

19.2.2 SYST_ARR (0x4064, 0x4065)

SYST_ARRH(0x4064)								
Bit	15	14	13	12	11	10	9	8
Name	SYST_ARR[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	1	1	0	1

SYST_ARRL(0x4065)								
Bit	7	6	5	4	3	2	1	0
Name	SYST_ARR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	1	1	1	1	1	1

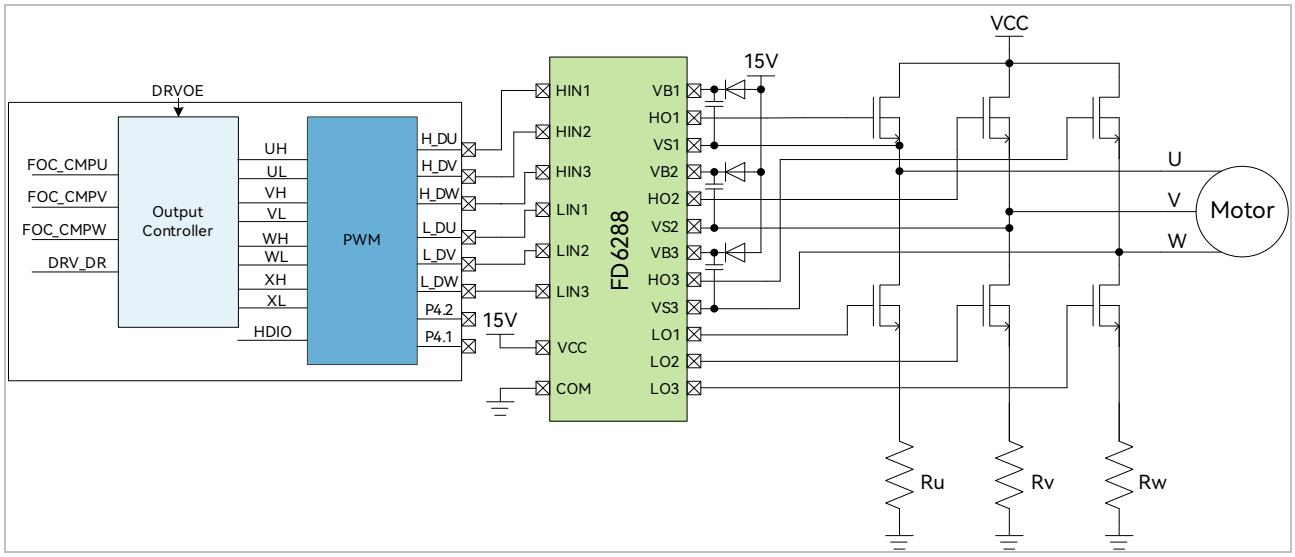
Bit	Name	Description
[15:0]	SYST_ARR	Systick Cycle This bit determines the cycle at which Systick interrupts are generated, which defaults to 1ms. Calculation formula is as follows: Systick rate = SYSCLK/(SYST_ARR[15:0] + 1) Range [0,65535]

20 Driver

20.1 Driver Instructions

20.1.1 FU6812 Driver

Figure 20-1 Functionl Block Diagram of FU6812 Driver Module



The FU6812 outputs PWM signals, and its functional block diagram is shown in Figure 20-1. In this mode, DRVOE serves as the enable signal for the PWM output. The PWM output is connected to the HVIC, which drives the MOSFET gates through the HVIC.

20.1.2 FU6861 / FU6862 / FU6872 Driver Introduction

Figure 20-2 Functionl Block Diagram of FU6861 Driver Module

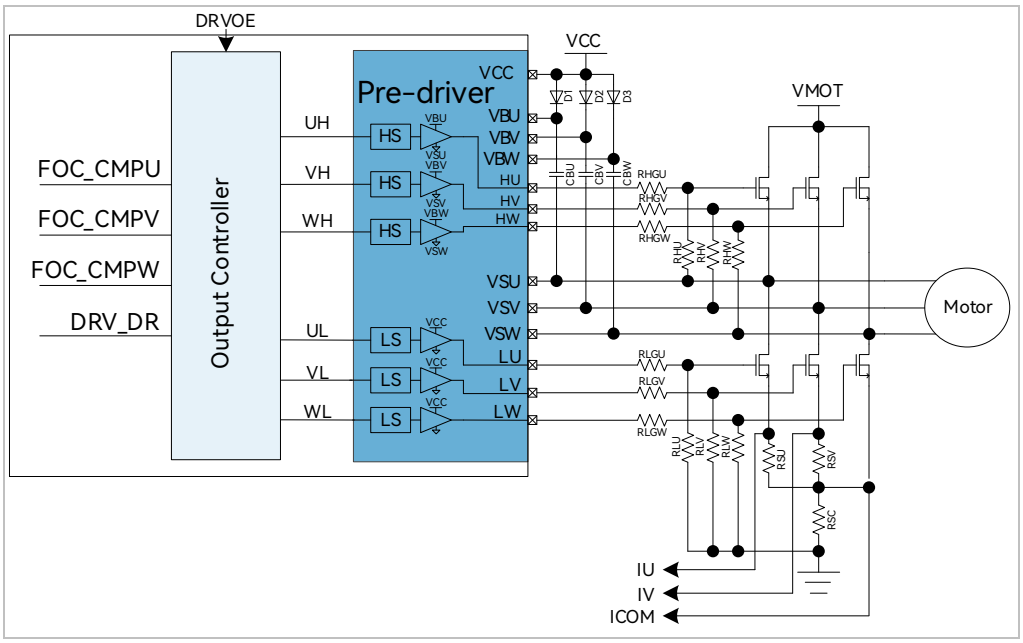


Figure 20-3 Functionl Block Diagram of FU6862 Driver Module

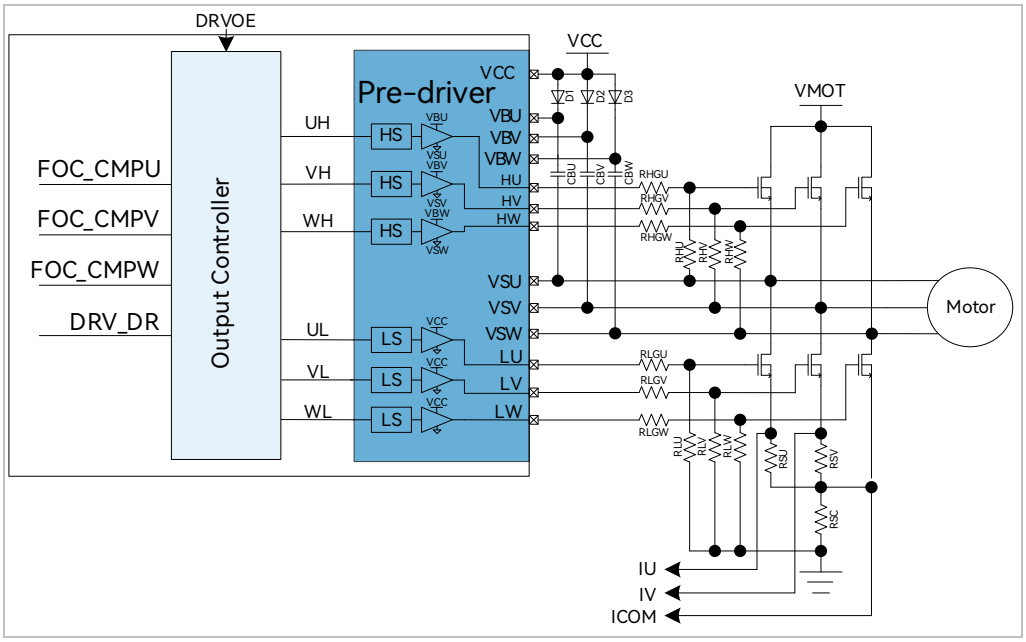
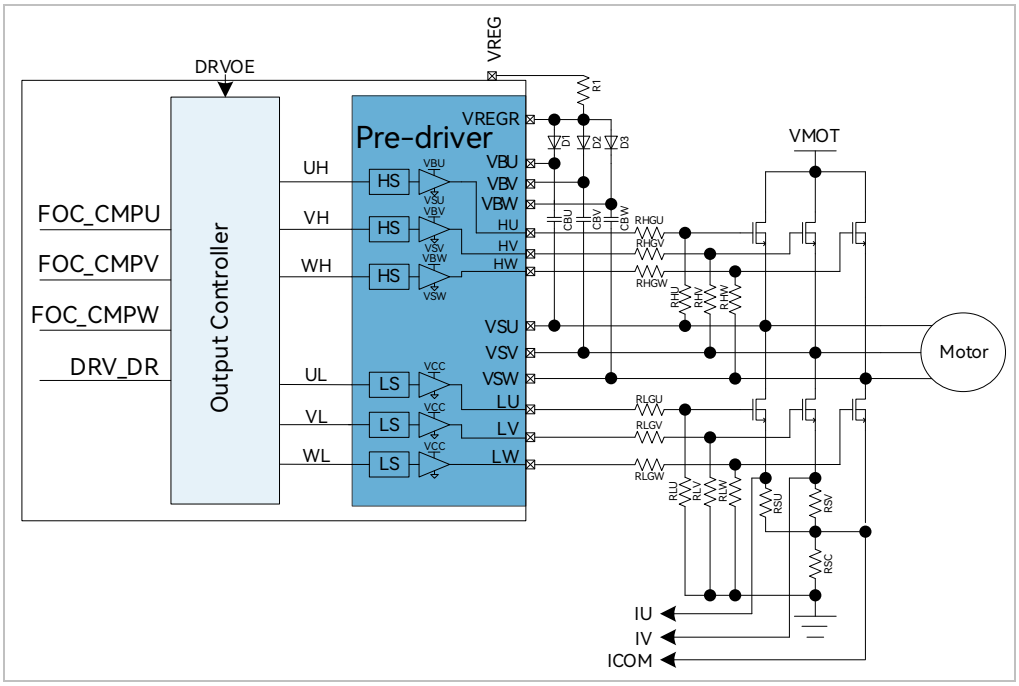


Figure 20-4 Functionl Block Diagram of FU6872 Driver Module



FOC_CMPU/V/W is the three-way comparison value output by FOC module, and DRV_DR is the comparison value set by the software. The above comparison value outputs three sets of level signals U/V/W to the Pre-driver (FU6812) or Pre-driver (FU6861 / FU6862 / FU6872) after passing through the output control module. The U/V/W three-way outputs are applied to DC brushless motor control, and the U/V/W/X four-way outputs to step motor control.

Table 20-1 Output Truth Values of Built-in Pre-driver (FU6861Q2 / FU6861L2 / FU6861N2 / FU6861NF2)

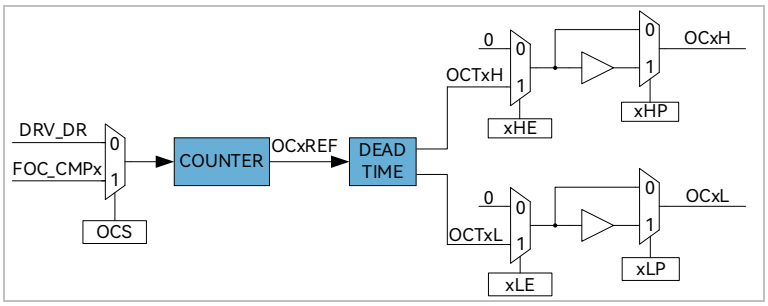
Input		Output	
UH/VH/WH	UL/VL/WL	HU/HV/HW	LU/LV/LW
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

Table 20-2 Output Truth Values of Built-in Pre-driver (FU6862L / FU6862Q / FU6872P)

Input		Output	
UH/VH/WH	UL/VL/WL	HU/HV/HW	LU/LV/LW
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

20.1.3 Output Control Module

Figure 20-5 Block Diagram of Output Control Module



Before Driver module works, DRV_CR[MESEL] is set to “1” to select FOC/SVPWM/SPWM mode or to “0” to select square-wave control mode.

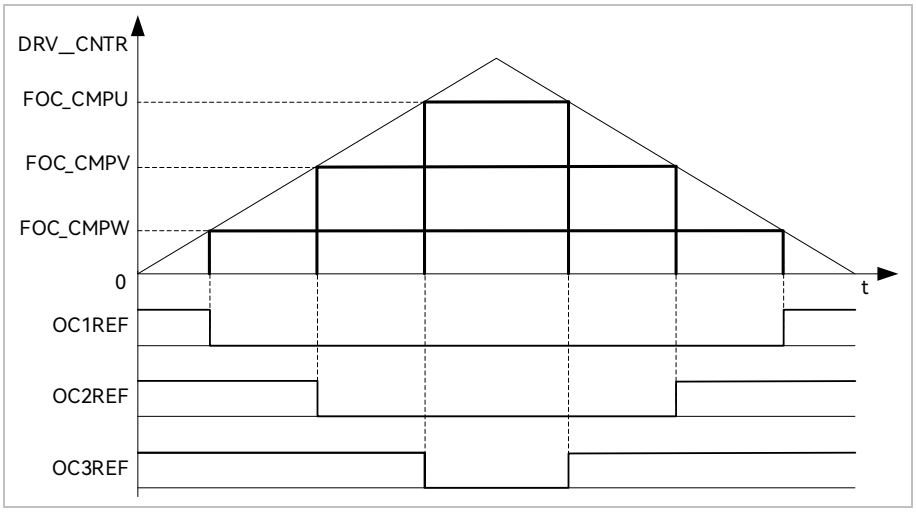
When DRV_CR[OCS] = 0, comparison value of PWM comes from DRV_DR, and OCTxH serves as the reference for output PWM signal. If OCxH and OCxL are output at the same time, OCTxL is output in reverse phase. When DRV_CR[OCS] = 1, comparison value of PWM comes from FOC module, and OCTxL serves as the reference for output PWM signal. If OCxH and OCxL are output at the same time, OCTxH is output in reverse phase.

20.1.3.1 Count and Compare Module

DRV_CR[OCS] is configured to select the comparison value of PWM from FOC_CMPU/V/W of FOC module or DRV_DR set by software. The comparison value is sent to the counter for comparison to obtain a 4-way PWM signal OCxREF, and DRV_DR is used for motor pre-charging, braking and BLDC control. If DRV_CNTR(built-in register) is smaller than the comparison value, OCxREF outputs high-level signal, and if DRV_CNTR is larger than the comparison value, OCxREF outputs low-level signal.

When DRV_CR[OCS] = 1, FOC_CMPU/V/W is compared with the count value to generate the duty cycle OC1REF/OC2REF/OC3REF.

Figure 20-6 PWM Generation



When DRV_CR[OCS] = 0, DRV_DR set by software is compared with the count value to generate OC1REF/OC2REF/OC3REF with the same duty cycle. Duty cycle = DRV_DR/DRV_ARR*100% (For example, if DRV_ARR=750 and DRV_DR = 375, then duty cycle = 50%).

20.1.3.2 Enable and Polarity of Output Signals

DRV_CMR[xHE] and DRV_CMR[xLE] are configured by software to enable high and low sides of the driver, and DRV_CMR[xHP] and DRV_CMR[xLP] to select the polarity of output. With DRV_DR and DRV_ARR registers, DRV_CMR[xHE] and DRV_CMR[xLE] can be configured to implement pre-charging, brake, etc.

Figure 20-7 Pre-charge Waveform

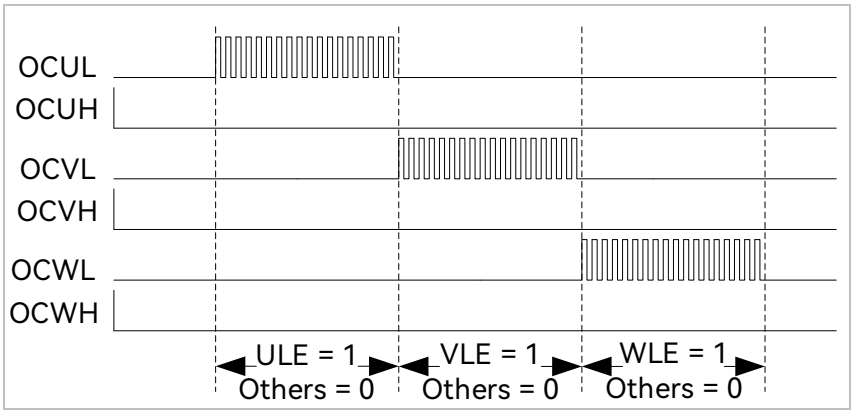
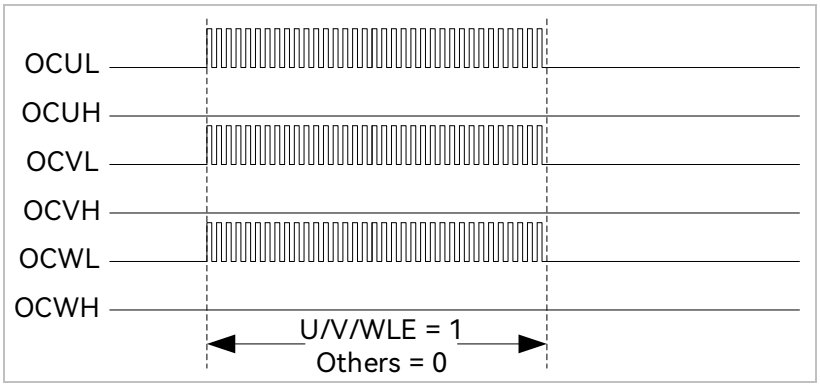


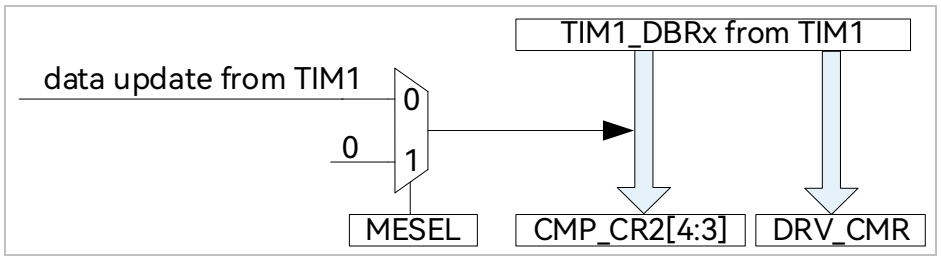
Figure 20-8 Brake Waveform



For square-wave control, Timer1 automatically controls DRV_CMR to implement phase commutation.

Configuring DRV_CR[MESEL] = 0 enables the Square Wave Drive Mode. After Timer1 generates timing, the data stored in the corresponding TIM1_DBRx are transferred to DRV_CMR.

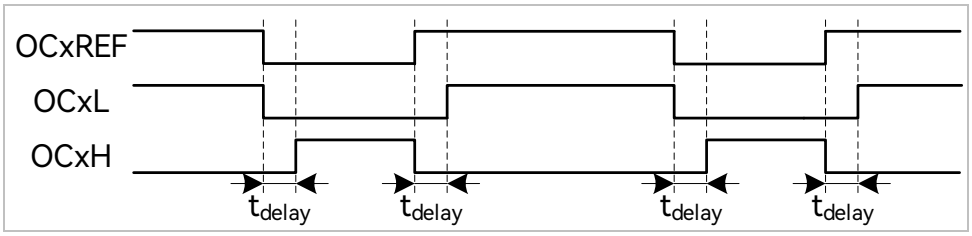
Figure 20-9 Timer1 Automatic Control of DRV_CMR and CMP_CR2[4:3]



20.1.3.3 Deadtime Module

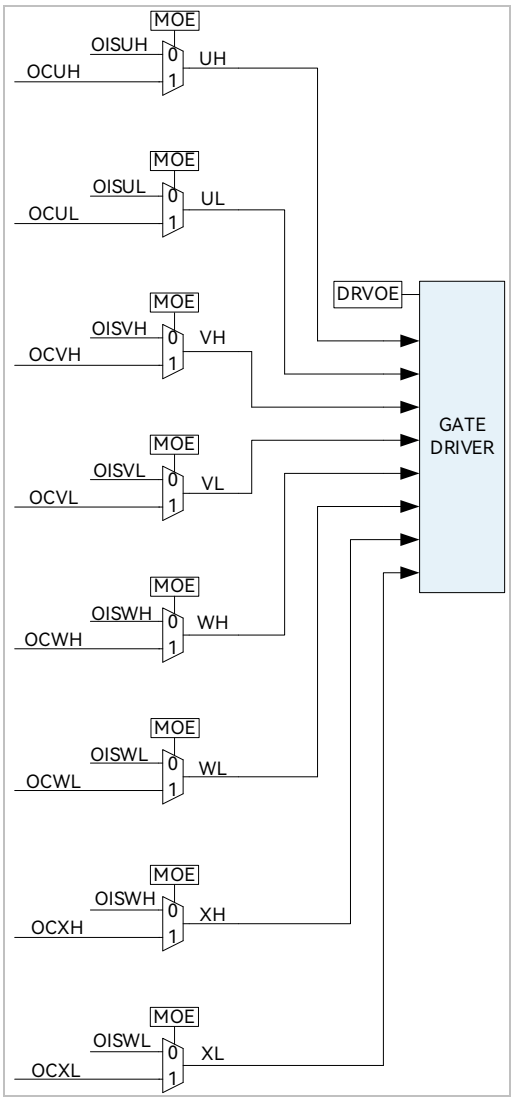
OCxREF supports deadtime insertion. For complementary outputs, the deadtime insertion is enabled when DRV_DTR is not “0”. Each channel has an 8-bit deadtime generator, and four channels have the same deadtime, which is set by DRV_DTR. When OCxREF rising edge signals are detected, output high level of OCxL is delayed for a period of time set in DRV_DTR. When OCxREF falling edge signals are detected, output high level of OcxH is delayed for a period of time set in DRV_DTR.

Figure 20-10 Complementary Outputs with Deadtime Insertion



20.1.3.4 Main Output Enable (MOE)

Figure 20-11 Block Diagram of Output Control Module



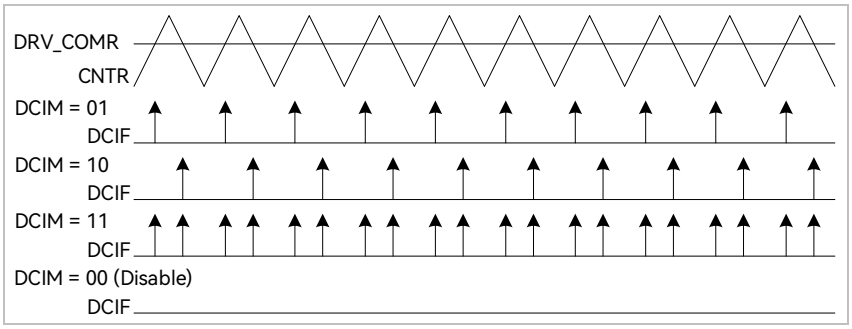
When DRV_OUT[MOE] is enabled, MOE module uses comparison value of the counter for motor control. When DRV_OUT[MOE] id disabled, the module outputs idle level set by the software to keep the motor at shutdown state.

20.1.3.5 Interrupts

20.1.3.5.1 Compare Match Interrupt

The generation conditions and time for compare match interrupt are configured by DRV_SR[DCIM] and DRV_COMR respectively. When the timer reaches the value set in DRV_COMR and the conditions set by DRV_SR[DCIM] are met, a compare match interrupt is generated and the interrupt flag DRV_SR[DCIF] is set to “1” by hardware.

Figure 20-12 Driver Compare Match Interrupt



20.1.3.5.2 FG Interrupt

FG interrupt is enabled when DRV_SR[FGIE] is set to “1”. The motor generates an interrupt for every electrical cycle.

20.2 Driver Registers

20.2.1 DRV_CR (0x4062)

Bit	7	6	5	4	3	2	1	0
Name	DRVEN	DDIR	FOCEN	DRPE	OCS	MESEL	RSV	DRVOE
Type	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W
Reset	0	0	0	0	0	0	-	0

Bit	Name	Description
[7]	DRVEN	Counter Enable 0: Disable 1: Enable
[6]	DDIR	Output Direction (Forward/Reverse) This bit sets motor rotation directions. It is valid in both square-wave drive and FOC drive modes. In sensorless FOC mode, setting this bit changes motor rotation. In sensored FOC mode, it is also required to modify the angle by the software. In square-wave control mode, parameters related to Timer1 shall be configured. 0: Forward 1: Reverse
[5]	FOCEN	FOC Module Enable 0: Disable 1: Enable
[4]	DRPE	DRV_DR Pre-load Enable When preload is enabled, the data written to DRV_DR is updated after a timer underflow event occurs. When preload is disabled, the data written to DRV_DR is updated immediately. 0: Disable 1: Enable
[3]	OCS	Comparison Source Selection 0: DRV_DR 1: FOC Module
[2]	MESEL	ME Operating Mode Selection 0: Square Wave Drive 1: FOC Drive
[1]	RSV	Reserved
[0]	DRVOE	Driver Enable 0: Disable 1: Enable

20.2.2 DRV_SR (0x4061)

Bit	7	6	5	4	3	2	1	0
Name	SYSTIF	SYSTIE	FGIF	DCIF	FGIE	DCIP	DCIM	
Type	R/W0	R/W	R/W0	R/W0	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	SYSTIF	Systick Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[6]	SYSTIE	Systick Interrupt Enable 0: Disable 1: Enable
[5]	FGIF	FG Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[4]	DCIF	Driver Compare Match Interrupt Flag When the Driver count value is equal to DRV_COMR, the system decides whether to generate an interrupt according to DRV_SR[DCIM]. Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[3]	FGIE	FG Interrupt Enable After the interrupt feature is enabled, an FG Interrupt is generated in each electrical cycle under FOC/square-wave control mode. 0: Disable 1: Enable
[2]	DCIP	Number of driver compare match cycles to generate an interrupt 0: 1 PWM cycle 1: 2 PWM cycles

[1:0]	DCIM	Driver Compare Match Interrupt Mode Selection When the Driver count value is equal to DRV_COMR, the system decides whether to generate an interrupt according to DRV_SR[DCIM]. 00: No interrupt is generated. 01: An interrupt is generated when the timer counts up. 10: An interrupt is generated when the timer counts down. 11: An interrupt is generated when the timer counts up/down.

20.2.3 DRV_OUT (0xF8)

Bit	7	6	5	4	3	2	1	0
Name	MOE	RSV	OISWXL	OISWXH	OISVL	OISVH	OISUL	OISUH
Type	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	-	0	0	0	0	0	0

Bit	Name	Description
[7]	MOE	Main Output Enable This bit selects the sources for high and low sides of the driver of phase-U/V/W/X output signals. It can be set to “1” and “0” by software. When bus current protection occurs, it is automatically cleared to “0” to turn off the output (see section 31.1.1.1). 0: Disable, with output sourced from the idle levels set by DRV_OUT[OISUH]/DRV_OUT[OISVH]/DRV_OUT[OISWH] and DRV_OUT[OISUL]/DRV_OUT[OISVL]/DRV_OUT[OISWL]. 1: Enable, with output sourced from the comparison value of the timer.
[6]	RSV	Reserved
[5]	OISWXL	Output idle level of WL/XL See descriptions on OISUH bit
[4]	OISWXH	Output idle level of WH/XH See descriptions on OISUH bit
[3]	OISVL	Output idle level of VL See descriptions on OISUH bit
[2]	OISVH	Output idle level of VH See descriptions on OISUH bit
[1]	OISUL	Output idle level of UL See descriptions on OISUH bit
[0]	OISUH	Output idle level of UH This bit sets the UH output in idle state. When DRV_OUT[MOE] = 0, it outputs idle level to disable MOS. 0: Low 1: High

20.2.4 DRV_CMR (0x405C, 0x405D)

DRV_CMRH(0x405C)								
Bit	15	14	13	12	11	10	9	8
Name	XHP	XLP	XHE	XLE	WHP	WLP	VHP	VLP
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DRV_CMRL(0x405D)								
Bit	7	6	5	4	3	2	1	0
Name	UHP	ULP	WHE	WLE	VHE	VLE	UHE	ULE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15]	XHP	High-side Polarity Control of Phase-X 0: Active High 1: Active Low
[14]	XLP	Low-side Polarity Control of Phase-X 0: Active High 1: Active Low
[13]	XHE	High-side Output of phase-X Enable 0: Disable 1: Enable
[12]	XLE	Low-side Output of Phase-X Enable 0: Disable 1: Enable
[11]	WHP	High-side Output Polarity of Phase-W 0: Active High 1: Active Low
[10]	WLP	Low-side Output Polarity of Phase-W 0: Active High 1: Active Low
[9]	VHP	High-side Output Polarity of Phase-V 0: Active High 1: Active Low
[8]	VLP	Low-side Output Polarity of Phase-V 0: Active High 1: Active Low
[7]	UHP	High-side Output Polarity of Phase-U 0: Active High 1: Active Low

[6]	ULP	Low-side Output Polarity of Phase-U 0: Active High 1: Active Low
[5]	WHE	High-side Output Enable of Phase-W 0: Disable 1: Enable
[4]	WLE	Low-side Output Enable of Phase-W 0: Disable 1: Enable
[3]	VHE	High-side Output Enable of Phase-V 0: Disable 1: Enable
[2]	VLE	Low-side Output Enable of Phase-U 0: Disable 1: Enable
[1]	UHE	High-side Output Enable of Phase-U 0: Disable 1: Enable
[0]	ULE	Low-side Output Enable of Phase-U 0: Disable 1: Enable

Note

- High-side and low-side outputs of phase-W/V/U/X are complementary and deadtime is automatically added when DRV_CMR[W/V/U/XLE] and DRV_CMR[W/V/U/XHE] are set to “1”
- Timer1 controls DRV_CMR register automatically when the square-wave drives

20.2.5 DRV_ARR (0x405E, 0x405F)

DRV_ARRH(0x405E)								
Bit	15	14	13	12	11	10	9	8
Name	DRV_ARR[15:8]							
Type	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DRV_ARRL(0x405F)								
Bit	7	6	5	4	3	2	1	0
Name	DRV_ARR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	DRV_ARR	Timer reload value, which determines PWM frequency (center-aligned)

		Driver timer up-counts from 0 to DRV_ARR and an overflow event occurs. Then it down-counts to 0. Calculation formula: $f_{Carrier} = f_{mcu}/2/(DRV\_ARR)$ Range [0,4095]

20.2.6 DRV_COMR (0x405A, 0x405B)

DRV_COMRH(0x405A)								
Bit	15	14	13	12	11	10	9	8
Name	DRV_COMR[15:8]							
Type	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DRV_COMRL(0x405B)								
Bit	7	6	5	4	3	2	1	0
Name	DRV_COMR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	DRV_COMR	Timer Compare Match Value The compare match interrupt is generated when the count value is equal to DRV_COMR and the conditions set in DRV_SR[DCIM] are met. Range [0,4095]

20.2.7 DRV_DR (0x4058, 0x4059)

DRV_DRH(0x4058)								
Bit	15	14	13	12	11	10	9	8
Name	DRV_DR[15:8]							
Type	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DRV_DRL(0x4059)								
Bit	7	6	5	4	3	2	1	0
Name	DRV_DR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:0]	DRV_DR	PWM Duty Cycle Setting in Software When DRV_CR[OCS] = 0, DRV_CNTR is compared with DRV_DR to output PWM. “1” is output when DRV_CNTR is smaller than DRV_DR, and “0” is output when DRV_CNTR is larger than DRV_DR. Range [0,4095]

		Note > When this register is used as a comparison source, PWM is referenced to high side of the driver and a deadtime is inserted in the complementary output of low side of the driver > Range [0, 4095]

20.2.8 DRV_DTR (0x4060)

Bit	7	6	5	4	3	2	1	0
Name	DRV_DTR							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	DRV_DTR	Deadtime Setting Deadtime = (DRV_DTR + 1) * T For example, if DRV_DTR = 11, deadtime = 12*41.67ns = 500ns Note When DRV_DTR = 0, deadtime insertion is disabled

21 System clock

21.1 Clock Intropduction

The clock system comprises two modules: the internal high-speed clock and the internal low-speed clock. The system clock operates on the internal high-speed clock, while the internal low-speed clock serves as the watchdog timer clock, with configurable overflow time.

21.2 Clock Caliberation Introduction

Clock calibration is a feature that uses internal slow clock to calibrate the internal fast clock. Register ISOSCSEL controls the slow clock source, internal slow clock or external clock input. Working principles: A 13-bit timer is used to count the length of 8 slow clock cycles with the fast clock as the clock source.

Caliberation operations:

1. Set CAL_CR0[CAL_STA] = 1 in software to start the calibration;
2. Read CAL_CR [CAL_BUSY] flag bit to check if the calibration process is completed;
3. When the calibration is completed (CAL_CR0[CAL_BUSY] = 0), the readout of CAL_CR0[CAL_ARR] is the value of the length of counting 8 slow clock cycles.

21.3 Register

21.3.1 CAL_CR (0x4040, 0X4041)

CAL_CRH(0x4040)								
Bit	15	14	13	12	11	10	9	8
Name	CAL_STA/ CAL_BUSY	RSV		CAL_ARR[12:8]				
Type	R/W	-	-	R	R/W	R/W	R/W	R/W
Reset	1	-	-	0	0	0	0	0
CAL_CRL(0x4041)								
Bit	7	6	5	4	3	2	1	0
Name	CAL_ARR[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15]	CAL_STA/ CAL_BUSY	Clock Calibration Enable Read: 0: Calibration is completed. 1: Calibration is in progress. Write: 0: No effect 1: Clock Calibration starts.
[14:13]	RSV	Reserved
[12:0]	CAL_ARR	Calibration Counts The count values of the fast clock to continuously count eight slow clock cycles. When this value is 0, it indicates that no corresponding slow clock input exists, and when this value is 0x1FFF, it indicates that the count overflows (slow clock is too slow or fast clock is too fast).

22 WDT

The watchdog timer (WDT) is a timer that works on the internal slow clock to monitor the master program operation and prevent the MCU running out. Watchdog works as follows: After watchdog operates, WDT starts counting. When WDT overflows, watchdog sends a signal to reset the MCU and the program restarts running from address 0. During the operation of master program, WDT has to be initialized at regular intervals to prevent WDT overflowing.

After being enabled, WDT starts counting from 0. When it reaches 0xFFFC, watchdog outputs a signal that is 4 internal slow clock cycles wide to reset MCU, and the program starts running from address 0. WDT has to be initialized according to WDT_REL at regular intervals during operation, and cannot reset the MCU.

22.1 WDT Notes

- When MCU enters standby or sleep mode, WDT stops counting, but the count values are retained.
- WDT is automatically disabled during emulation.
- RST_SR[RSTWDT] is set to “1” when MCU is reset by WDT overflow.

22.2 WDT Operations

1. Set CCFG1[WDT_EN] = 1 to start WDT, which then starts counting from 0;
2. Set WDT_REL (this operation can also be performed before starting WDT);
3. Set WDT_CR[WDTRF] = 1 in the running of program to initialize WDT.

22.3 WDT Registers

22.3.1 WDT_CR (0x4026)

Bit	7	6	5	4	3	2	1	0
Name	RSV							WDTRF
Type	-	-	-	-	-	-	-	R/W
Reset	-	-	-	-	-	-	-	0

Bit	Name	Description
[7:1]	RSV	Reserved
[0]	WDTRF	0: No effect 1: WDT is initialized.

22.3.2 WDT_REL (0x4027)

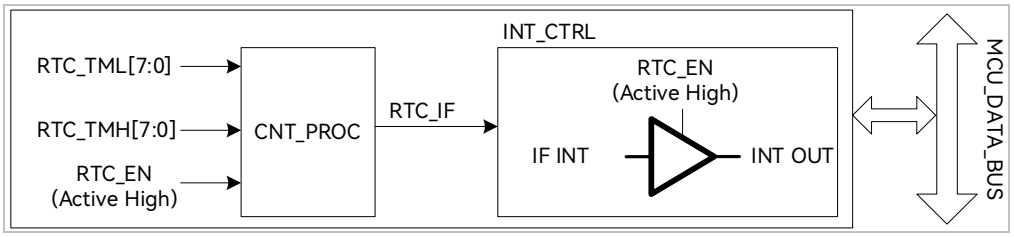
Bit	7	6	5	4	3	2	1	0
Name	WDT_REL							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	WDT_REL	This bit sets 8 high-order bits of WDT after initialization.

23 RTC

23.1 RTC Functional Block Diagram

Figure 23-1 RTC Functional Block Diagram



23.2 RTC Operations

A write to RTC_TM sets RTC reload value. RTC is enabled when RTC_STA[RTC_EN] is set to “1”.

23.3 RTC Registers

23.3.1 RTC_TM (0x402C, 0x402D)

RTC_TMH(0x402C)								
Bit	15	14	13	12	11	10	9	8
Name	RTC_TM[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
RTC_TML(0x402D)								
Bit	7	6	5	4	3	2	1	0
Name	RTC_TM[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	Name	Description
[15:0]	RTC_TM	RTC Count Register Write: RTC timer up-counts at a rate of 32768Hz from 0 to RTC_TM[15:0] and becomes overflowed. Meanwhile, an interrupt request is generated, causing the timer to be cleared and restart counting. Read: Instantaneous value of the timer

23.3.2 RTC_STA (0x402E)

Bit	7	6	5	4	3	2	1	0
Name	RTC_EN	RTC_IF	ISOSCSEL	ISOSCEN	RSV			
Type	R/W	R/W0	R/W	R/W	-	-	-	-
Reset	0	0	0	0	-	-	-	-

Bit	Name	Description
[7]	RTC_EN	RTC Enable 0: Disable 1: Enable
[6]	RTC_IF	RTC Interrupt Flag When IE[RTC_IF] is “1”, counter value is equal to RTC_TM. Read: 0: No interrupt pending 1: Iinterrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[5]	ISOSCSEL	External Source for Clock Calibration 0: Internal Slow Clock 1: P1.1 Input
[4]	ISOSCEN	Internal Slow Clock Enable 0: Disable 1: Enable
[3:0]	RSV	Reserved

24 IO

24.1 IO Introduction

FU6812L2 has up to 34 GPIO pins, including P0.0 ~ P0.7, P1.0 ~ P1.7, P20 ~ P2.7, P3.0 ~ P3.7, P4.1 ~ P4.2, and IOVCC.

FU6812N2 has up to 20 GPIO pins, including P0.0 ~ P0.1, P0.4 ~ P0.7, P1.1 ~ P1.6, P2.1, P2.4, P2.6 ~ P2.7, P3.0 ~ P3.2, P3.5, and IOVCC.

FU6812S2 has up to 12 GPIO pins, including P0.5 ~ P0.7, P1.2 ~ P1.3, P1.6, P2.1, P2.4, P2.7, P3.0 ~ P3.2, and IOVCC.

FU6812V has up to 13 GPIO pins, including P0.5 ~ P0.6, P1.1 ~ P1.2, P1.4, P1.6, P2.1, P2.4 ~ P2.6, P3.0 ~ P3.1, and P3.4.

FU6812Q2 has up to 32 GPIO pins, including P0.0 ~ P0.7, P1.0 ~ P1.7, P2.0 ~ P2.7, P3.0 ~ P3.7, and IOVCC.

FU6812L2 has up to 27 GPIO pins, including P0.0 ~ P0.1, P0.4 ~ P0.7, P1.0 ~ P1.7, P2.0 ~ P2.4, P2.6 ~ P2.7, P3.0 ~ P3.5, and IOVCC.

FU6812N2 has up to 19 GPIO pins, including P0.0 ~ P0.1, P0.4 ~ P0.7, P1.1 ~ P1.4, P1.6, P2.0 ~ P2.1, P2.3 ~ P2.4, P2.6 ~ P2.7, P3.0 ~ P3.2, P3.5, and IOVCC. Among them, P0.7 and P1.1 work on the same pin, and P1.3 and P1.4 work on the same pin.

FU6861NF2 has up to 19 GPIO pins, including P0.0 ~ P0.1, P0.4 ~ P0.7, P1.1 ~ P1.4, P1.6, P2.0 ~ P2.1, P2.3 ~ P2.4, P2.6 ~ P2.7, P3.0 ~ P3.2, P3.5, and IOVCC. Among them, P0.7 and P1.1 work on the same pin, and P1.3 and P1.4 work on the same pin.

FU6862L has up to 20 GPIO pins, including P0.1, P0.5 ~ P0.7, P1.2 ~ P1.7, P2.1 ~ P2.2, P2.4, P2.6 ~ P2.7, P3.0 ~ P3.1, and P3.3 ~ P3.5.

FU6862Q has up to 20 GPIO pins, including P0.1, P0.5 ~ P0.7, P1.2 ~ P1.7, P2.1 ~ P2.2, P2.4, P2.6 ~ P2.7, P3.0 ~ P3.1, and P3.3 ~ P3.5.

FU6872P has up to 18 GPIO pins, including P0.0 ~ P0.1, P0.5 ~ P0.7, P1.1 ~ P1.4, P1.6, P2.1, P2.4, P2.6 ~ P2.7, P3.0 ~ P3.1, and P3.3 ~ P3.4.

24.2 IO Operations

Each GPIO port pin has relevant registers to meet different application requirements. For example, P0.0 is mapped to register P0, and P1.0 to register P1. P0_OE and P1_OE registers are configured for digital input and output.

- The enable bits of pull-up resistors and pull-down resistors are configured to “1”. See 24.3.9 P0_PU (0x4053) ~ 24.3.13 P4_PU (0x4057) for port pins and registers.
- See 5.3 GPIO Electrical Characteristics for the values of pull-up resistors and pull-down resistors.
- The relevant bits of P1_AN, P2_AN and P3_AN registers are configured to “1” to activate analog signal mode. See 24.3.5 P4_OE (0xE9)

Bit	7	6	5	4	3	2	1	0
Name	RSV					P4_OE		
Type	-	-	-	-	-	R/W	R/W	R/W
Reset	-	-	-	-	-	0	0	0

Bit	Name	Description
[7:3	RSV	Reserved
[2:0]	P4_OE	P4.0 ~ P4.2 Digital I/O Selection 0: Input 1: Output

- P1_AN (0x4050) ~ 24.3.8 P3_AN (0x4052) for port pins and registers. After the port pins are configured to analog mode, all their digital features are disabled and the port state is 0 by reading relevant bits in P1, P2 and P3 registers.
- Pull-up resistors of P0.0 ~ P0.2, P1.3 ~ P1.6. P2.1, and P3.6 ~ P3.7 are automatically disabled when the port pins are configured as analog mode.
- IO Priority:
  - GPIO has the lowest priority
  - P0.1: I^2C > Timer4 > GPIO
  - P0.5: SPI > UART > GPIO
  - P0.6: Timer4 > SPI > UART > GPIO
  - P0.7: Timer2 > CMP > SPI >GPIO

24.3 IO Registers

24.3.1 P0_OE (0xFC)

Bit	7	6	5	4	3	2	1	0
Name	P0_OE							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	P0_OE	P0.0 ~ P0.7 Digital I/O Selection 0: Input 1: Output

24.3.2 P1_OE (0xFD)

Bit	7	6	5	4	3	2	1	0
Name	P1_OE							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	P1_OE	P1.0 ~ P1.7 Digital I/O Selection 0: Input 1: Output

24.3.3 P2_OE (0xFE)

Bit	7	6	5	4	3	2	1	0
Name	P2_OE							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	P2_OE	P2.0 ~ P2.7 Digital I/O Selection 0: Input 1: Output

24.3.4 P3_OE (0xFF)

Bit	7	6	5	4	3	2	1	0
Name	P3_OE							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	P3_OE	P3.0 ~ P3.7 Digital I/O Selection 0: Input 1: Output

24.3.5 P4_OE (0xE9)

Bit	7	6	5	4	3	2	1	0
Name	RSV					P4_OE		
Type	-	-	-	-	-	R/W	R/W	R/W
Reset	-	-	-	-	-	0	0	0

Bit	Name	Description
[7:3	RSV	Reserved
[2:0]	P4_OE	P4.0 ~ P4.2 Digital I/O Selection 0: Input 1: Output

24.3.6 P1_AN (0x4050)

Bit	7	6	5	4	3	2	1	0
Name	RSV				HBMOD	HDIO	ODE1	ODE0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>[7:4]</td><td>P1_AN</td><td>P1.4 ~ P1.7 Analog Mode Enable
0: Disable
1: Enable</td></tr>
<tr><td>[3]</td><td>HBMOD</td><td>P1.3 mode configuration, which determines the functional mode of P1.3 in combination with P1_OE[3], as shown in Table 24-1.
Table 24-1 P1.3 Mode Settings
<table>
<tr><th>HBMOD</th><th>P1_OE[3]</th><th>P1.3 Pin Mode</th></tr>
<tr><td>0</td><td>0</td><td>Digital Input (DI)</td></tr>
<tr><td>0</td><td>1</td><td>Digital Output (DO)</td></tr>
<tr><td>1</td><td>0</td><td>Analog Input (AI)</td></tr>
<tr><td>1</td><td>1</td><td>Enhanced digital drive output mode. The high level output provides enhanced drive capability. The low level output provides the same drive capability as that in digital output (DO) mode “01”.</td></tr>
</table></td></tr>
<tr><td>[2]</td><td>HDIO</td><td>PWM IO Output Driver Power Selection (Only valid to L_DU, L_DV, L_DW, H_DU, H_DV, and H_DW)</td></tr>
</table>

		0: Normal 1: High
[1]	ODE1	P0.1 Open-drain Output 0: Disable 1: Enable
[0]	ODE0	P0.0 Open-drain Output 0: Disable 1: Enable

24.3.7 P2_AN (0x4051)

Bit	7	6	5	4	3	2	1	0
Name	P2_AN							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	P2_AN	P2.0 ~ P2.7 Analog Mode Enable 0: Disable 1: Enable

24.3.8 P3_AN (0x4052)

Bit	7	6	5	4	3	2	1	0
Name	RSV		P3_AN					
Type	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	-	0	0	0	0	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5:0]	P3_AN	P3.0 ~ P3.5 Analog Mode Enable 0: Disable 1: Enable

24.3.9 P0_PU (0x4053)

Bit	7	6	5	4	3	2	1	0
Name	P0_PU							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	P0_PU	P0.0 ~ P0.7 Pull-up Resistor Enable 0: Disable

		1: Enable
[4:0]	RSV	Reserved

24.3.10 P1_PU (0x4054)

Bit	7	6	5	4	3	2	1	0
Name	P1_PU							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Reset	0	0	0	0	0	0	0	-

Bit	Name	Description
[7:0]	P1_PU	P1.0 ~ P1.7 Pull-up Resistor Enable 0: Disable 1: Enable

24.3.11 P2_PU (0x4055)

Bit	7	6	5	4	3	2	1	0
Name	P2_PU							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	P2_PU	P2.0 ~ P2.7 Pull-up Resistor Enable 0: Disable 1: Enable

24.3.12 P3_PU (0x4056)

Bit	7	6	5	4	3	2	1	0
Name	P3_PU							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	P3_PU	P3.0 ~ P3.7 Pull-up Resistor Enable 0: Disable 1: Enable

24.3.13 P4_PU (0x4057)

Bit	7	6	5	4	3	2	1	0
Name	RSV					P4_PU		
Type	-	-	-	-	-	R/W	R/W	R/W
Reset	-	-	-	-	-	0	0	0

Bit	Name	Description
[7:3]	RSV	Reserved
[2:0]	P4_PU	P4.0 ~ P4.2 Pull-up Resistor Enable 0: Disable 1: Enable

24.3.14 PH_SEL (0x404C)

Bit	7	6	5	4	3	2	1	0
Name	SPITMOD	UARTEN	UARTCH	T4SEL	T3SEL	T2SEL	T2SSEL	XOE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	SPITMOD	MISO pin status after SPI slave device completes transmission 0: Output State 1: High-impedance State
[6]	UARTEN	UART Enable 0: Disable 1: Enable
[5]	UARTCH	UART Function Switching 0: Disable, with P0.6 serving as RXD and P0.5 as TXD 1: Enable, with P3.3 serving as RXD and P3.4 as TXD
[4]	T4SEL	Port Pins Multiplexed as Timer4 0: Disable, with P0.1 serving as general-purposed GPIO 1: Enable, with P0.1 multiplexed as Timer4 I/O pins. Note I²Chas the higher priority than Timer4. When I²C is enabled, P0.1 is the SCL interface of I²C
[3]	T3SEL	Port Pins Multiplexed as Timer3 0: Disable, with P1.1 serving as general-purposed GPIO 1: Enable, with P1.1 multiplexed as Timer3 I/O pins.
[2]	T2SEL	Port Pins for Timer2 Enable 0: Disable, with P1.0 serving as general-purposed GPIO 1: Enable, with P1.0 multiplexed as Timer2 I/O pins

[1]	T2SSEL	Port Pins Multiplexed as Timer2S 0: Disable, with P0.7 serving as general-purposed GPIO 1: Enable, with P0.7 multiplexed as Timer2 I/O pins  Note Timer2 has the highest priority, followed by comparator output and then MISO
[0]	XOE	XH/L Interface Enable 0: P4.2/P4.1 serving as general-purposed GPIO 1: P4.2/P4.1 serve as the outputs for XH/XL. Depending on the value of DRVOE[MOE], P4.2/P4.1 either output the active signal or the idle level defined by OISWH/OISWL.

24.3.15 P0(0x80)/P1(0x90)/P2(0xA0)/P3(0xB0)/P4(0xE8)

Port output register P0/1/2/3/4 supports read and write access. RMW commands are used to access the register value (see Table 24-3 for RMW commands), and other commands are used to access PORT pin.

Table 24-2 P0/P1/P2/P3/P4

Bit	7	6	5	4	3	2	1	0
Name	GPx[7]	GPx[6]	GPx[5]	GPx[4]	GPx[3]	GPx[2]	GPx[1]	GPx[0]
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Register Name	Descriptions	Type	Initial Value
P0[7:0]	GPIO Register0	R/W	0x00
P1[7:0]	GPIO Register1	R/W	0x00
P2[7:0]	GPIO Register2	R/W	0x00
P3[7:0]	GPIO Register3	R/W	0x00
P4[2:0]	GPIO Register4	R/W	0x00

Table 24-3 RMW Commands

Command	Descriptions
ANL	Bitwise logical AND operation
ORL	Bitwise logical OR operation
XRL	Bitwise logical XOR operation
JBC	Jump if the bit is set to“1” and then cleared to “0”
CPL	Bitwise logical converse operation
INC,DEC	+1, -1 logical operation
DJNZ	Jump if the bit is not “0”
MOV Px,y, C	Assign carry bit C to Px, y
CLR Px,y	Px, y is cleared to “0”
SETB Px,y	Px, y is set to “1”

25 ADC

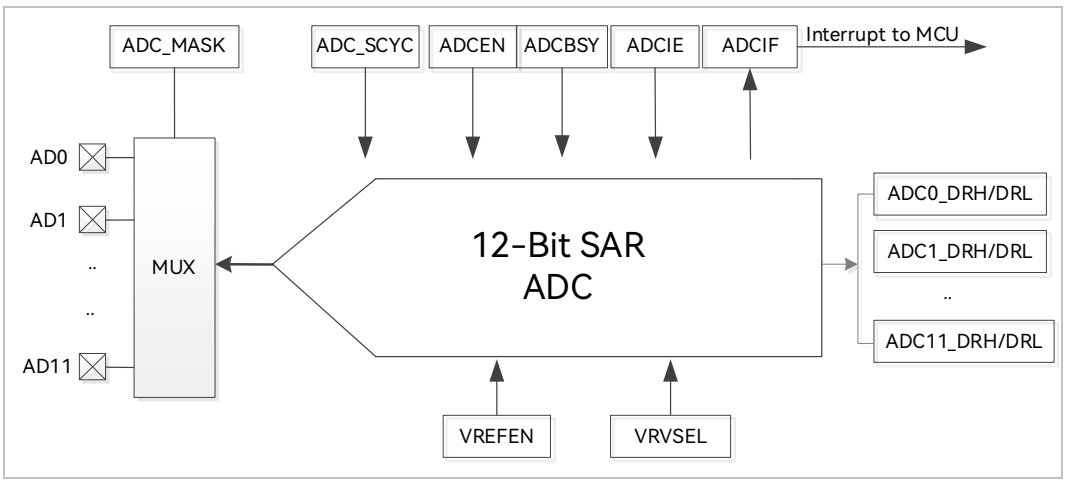
25.1 ADC Introduction

ADC module is a 12-bit successive approximation register ADC with 12 channels inside at most. The sampling mode supports sequential sampling and triggered sampling (triggered by FOC module). After FOC module is enabled (DRV_CR[FOCEN] = 1), it automatically starts ADC module and triggers ADC sampling when necessary. The result of triggered sampling is sent to FOC module for motor control. Triggered sampling is done automatically by hardware, and sequential sampling is controlled by software. The priority of triggered sampling is higher than that of sequential sampling. If both triggered sampling and sequential sampling are applied at the same time, the triggered sampling is performed first, and ADC automatically stores sequential sampling mode upon completion of triggered sampling.

The clock source for ADC sampling is 12MHz and the sampling time is set by ADC_SCYC. See for sample time and conversion time.

25.2 ADC Block Diagram

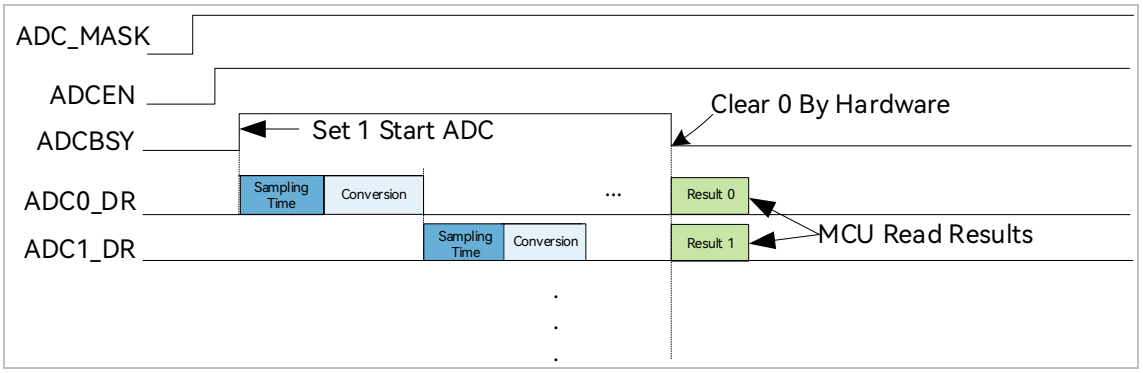
Figure 25-1 ADC Functional Block Diagram



25.3 ADC Operations

25.3.1 Sequential Sampling Mode

Figure 25-2 ADC Sequential Sampling Timing



ADC operations:

1. Set the appropriate ADC VREF;
2. Configure ADC_MASK to enable the corresponding channel required to sample;
3. Configure ADC_SCYC (minimum value is 3) to select the sampling period of each channel;
4. Configure ADC_CR[ADCEN] = 1 to enable ADC;
5. Configure ADC_CR[ADCBSY] = 1 to start ADC;
6. When ADC_CR[ADCBSY] = 0, read ADCx_DR to obtain ADC results.

Note

The ADC conversion sequence is from low to high based on the enabled channel (i.e., when channel 2/3/4 is enabled, the signal is sampled in order of 2/3/4, and a single conversion result is read after confirming ADC_CR[ADCBSY] = 0).

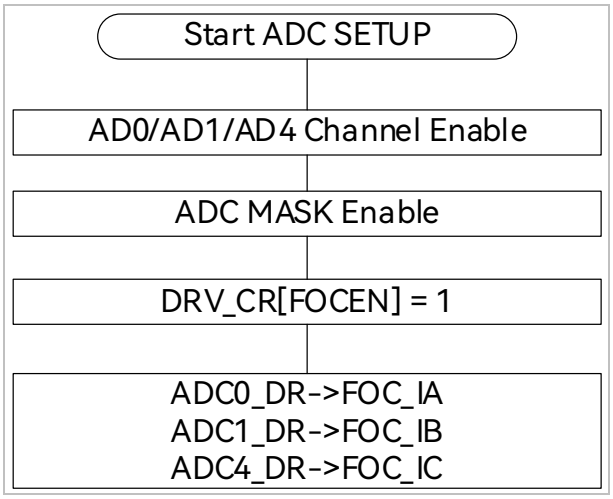
25.3.2 ADC Triggered Sampling Mode

After FOC module is enabled, ADC module can initiate ADC triggered sampling when required. ADC triggered sampling and sequential sampling can be requested at the same time. Internal circuit automatically matches the timing for the two different sampling modes, but different ADC channels shall be configured.

After FOC module is enabled (DRV_CR[FOCEN] = 1), FOC module automatically starts ADC module and

triggers ADC sampling when necessary. The result of triggered sampling is sent to FOC module for motor control.

Figure 25-3 ADC Triggered Sampling Process



As shown above, after ADC channel 0/1/4 is enabled and FOC module is enabled, FOC module can trigger ADC triggered sampling and directly read the results.

25.4 ADC Registers

25.4.1 ADC_CR (0x4039)

Bit	7	6	5	4	3	2	1	0
Name	ADCEN	ADCBSY	RSV			ADCALIGN	ADCIE	ADCIF
Type	R/W	R/W1	-	-	-	R/W	R/W	R/W0
Reset	0	0	-	-	-	0	0	0

Bit	Name	Description
[7]	ADCEN	ADC Enable 0: Disable 1: Enable
[6]	ADCBSY	ADC Startup & ADC Busy Flag Read: 0: Idle 1: Busy Write: 0: No effect 1: ADC transfer startup Note Writing “1” to this bit has no effect when ADC_MASK = 0.
[5:3]	RSV	Reserved
[2]	ADCALIGN	ADC Data Format Selection 0: ADC output is right-aligned 1: ADC output is left-second-high-aligned (invalid in triggered sampling mode) Note The triggerd sampling mode remains unaffected and is fixed to left-aligned with the second highest bit
[1]	ADCIE	ADC Interrupt Enable (excluding triggered sampling mode interrupt) This bit determines whether ADC_CR[ADCIF] sends ADC interrupt to MCU. 0: Disable 1: Enable
[0]	ADCIF	ADC Conversion End Flag After the ADC conversion is completed, ADC_CR[ADCIF] = 1. Read: 0: No interrupt pending 1: Interrupt pending Write:

		0: This bit is cleared to “0” 1: No effect

25.4.2 ADC_MASK (0x4036, 0x4037)

ADC_MASKH(0x4036)								
Bit	15	14	13	12	11	10	9	8
Name	ADC_SCYCH[3:0]				CH11EN	CH10EN	CH9EN	CH8EN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	0	0	0	0
ADC_MASKL(0x4037)								
Bit	7	6	5	4	3	2	1	0
Name	CH7EN	CH6EN	CH5EN	CH4EN	CH3EN	CH2EN	CH1EN	CH0EN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:12]	ADC_SCYCH[3:0]	ADC Sampling Cycle for ADC Channel 8, 9, 10 and 11 ADC_SCYCH[3] = 0: Sampling cycle is ADC_SCYCH[2:0] ADC clock cycles. ADC_SCYCH[3] = 1: Sampling cycle is (ADC_SCYCH[2:0]*8 + 7) ADC clock cycles.
[11]	CH11EN	ADC Channel 11 Enable 0: Disable 1: Enable
[10]	CH10EN	ADC Channel 10 Enable 0: Disable 1: Enable
[9]	CH9EN	ADC Channel 9 Enable 0: Disable 1: Enable
[8]	CH8EN	ADC Channel 8 Enable 0: Disable 1: Enable
[7]	CH7EN	ADC Channel 7 Enable 0: Disable 1: Enable
[6]	CH6EN	ADC Channel 6 Enable 0: Disable 1: Enable
[5]	CH5EN	ADC Channel 5 Enable 0: Disable 1: Enable

[4]	CH4EN	ADC Channel 4 Enable 0: Disable 1: Enable
[3]	CH3EN	ADC Channel 3 Enable 0: Disable 1: Enable
[2]	CH2EN	ADC Channel 2 Enable 0: Disable 1: Enable
[1]	CH1EN	ADC Channel 1 Enable 0: Disable 1: Enable
[0]	CH0EN	ADC Channel 0 Enable 0: Disable 1: Enable

Note

ADC_MASK is not necessary for triggered sampling mode

25.4.3 ADC_SCYC (0x4038)

Bit	7	6	5	4	3	2	1	0
Name	ADC_SCYC[7:4]				ADC_SCYC[3:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	0	0	1	1

Bit	Name	Description
[7:4]	ADC_SCYC[7:4]	ADC Sampling Cycle for ADC Channel 5, 6 and 7 ADC_SCYC[7] = 0: Sampling cycle is ADC_SCYC[6:4] ADC clock cycles. ADC_SCYC[7] = 1: Sampling cycle is (ADC_SCYC[6:4]*8 + 7) ADC clock cycles.
[3:0]	ADC_SCYC[3:0]	ADC Sampling Cycle for ADC Channel 0 ~ 4 ADC_SCYC[3] = 0: Sampling cycle is ADC_SCYC[2:0] ADC clock cycles. ADC_SCYC[3] = 1: Sampling cycle is (ADC_SCYC[2:0]*8 + 7) ADC clock cycles.

25.4.4 ADC0_DR (0x0300, 0x0301)

ADC0_DRH(0x0300)								
Bit	15	14	13	12	11	10	9	8
Name	RSV				DH[11:8]			
Type	-	-	-	-	R	R	R	R
Reset	-	-	-	-	0	0	0	0

ADC0_DRL(0x0301)								
Bit	7	6	5	4	3	2	1	0
Name	DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:12]	RSV	Reserved
[11:8]	DH	4 high-order bits of the result by ADC channel 0 after ADC conversion
[7:0]	DL	8 low-order bits of the result by ADC channel 0 after ADC conversion

25.4.5 ADC1_DR (0x0302, 0x0303)

ADC1_DRH(0x0302)								
Bit	15	14	13	12	11	10	9	8
Name	RSV				DH[11:8]			
Type	-	-	-	-	R	R	R	R
Reset	-	-	-	-	0	0	0	0
ADC1_DRL(0x0303)								
Bit	7	6	5	4	3	2	1	0
Name	DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:12]	RSV	Reserved
[11:8]	DH	4 high-order bits of the result by ADC channel 1 after ADC conversion
[7:0]	DL	8 low-order bits of the result by ADC channel 1 after ADC conversion

25.4.6 ADC2_DR (0x0304, 0x0305)

ADC2_DRH(0x0304)								
Bit	15	14	13	12	11	10	9	8
Name	RSV				DH[11:8]			
Type	-	-	-	-	R	R	R	R
Reset	-	-	-	-	0	0	0	0
ADC2_DRL(0x0305)								
Bit	7	6	5	4	3	2	1	0
Name	DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description

[15:12]	RSV	Reserved
[11:8]	DH	4 high-order bits of the result by ADC channel 2 after ADC conversion
[7:0]	DL	8 low-order bits of the result by ADC channel 2 after ADC conversion

25.4.7 ADC3_DR (0x0306, 0x0307)

ADC4_DRH(0x0306)								
Bit	15	14	13	12	11	10	9	8
Name	RSV				DH[11:8]			
Type	-	-	-	-	R	R	R	R
Reset	-	-	-	-	0	0	0	0
ADC4_DRL(0x0307)								
Bit	7	6	5	4	3	2	1	0
Name	DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:12]	RSV	Reserved
[11:8]	DH	4 high-order bits of the result by ADC channel 3 after ADC conversion
[7:0]	DL	8 low-order bits of the result by ADC channel 3 after ADC conversion

25.4.8 ADC4_DR (0x0308, 0x0309)

ADC4_DRH(0x0308)								
Bit	15	14	13	12	11	10	9	8
Name	RSV				DH[11:8]			
Type	-	-	-	-	R	R	R	R
Reset	-	-	-	-	0	0	0	0
ADC4_DRL(0x0309)								
Bit	7	6	5	4	3	2	1	0
Name	DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:12]	RSV	Reserved
[11:8]	DH	4 high-order bits of the result by ADC channel 4 after ADC conversion
[7:0]	DL	8 low-order bits of the result by ADC channel 4 after ADC conversion

25.4.9 ADC5_DR (0x030A, 0x030B)

ADC4_DRH(0x030A)								
Bit	15	14	13	12	11	10	9	8
Name	RSV				DH[11:8]			
Type	-	-	-	-	R	R	R	R
Reset	-	-	-	-	0	0	0	0
ADC4_DRL(0x030B)								
Bit	7	6	5	4	3	2	1	0
Name	DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:12]	RSV	Reserved
[11:8]	DH	4 high-order bits of the result by ADC channel 5 after ADC conversion
[7:0]	DL	8 low-order bits of the result by ADC channel 5 after ADC conversion

25.4.10 ADC6_DR (0x030C, 0x030D)

ADC4_DRH(0x030C)								
Bit	15	14	13	12	11	10	9	8
Name	RSV				DH[11:8]			
Type	-	-	-	-	R	R	R	R
Reset	-	-	-	-	0	0	0	0
ADC4_DRL(0x030D)								
Bit	7	6	5	4	3	2	1	0
Name	DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
Name	RSV	Reserved
Type	DH	4 high-order bits of the result by ADC channel 6 after ADC conversion
Reset	DL	8 low-order bits of the result by ADC channel 6 after ADC conversion

25.4.11 ADC7_DR (0x030E, 0x030F)

ADC4_DRH(0x030E)								
Bit	15	14	13	12	11	10	9	8
Name	RSV				DH[11:8]			
Type	-	-	-	-	R	R	R	R
Reset	-	-	-	-	0	0	0	0

ADC4_DRL(0x030F)								
Bit	7	6	5	4	3	2	1	0
Name	DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:12]	RSV	Reserved
[11:8]	DH	4 high-order bits of the result by ADC channel 7 after ADC conversion
[7:0]	DL	8 low-order bits of the result by ADC channel 7 after ADC conversion

25.4.12 ADC8_DR (0x0310, 0x0311)

ADC8_DRH(0x0310)								
Bit	15	14	13	12	11	10	9	8
Name	RSV				DH[11:8]			
Type	-	-	-	-	R	R	R	R
Reset	-	-	-	-	0	0	0	0
ADC8_DRL(0x0311)								
Bit	7	6	5	4	3	2	1	0
Name	DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:12]	RSV	Reserved
[11:8]	DH	4 high-order bits of the result by ADC channel 8 after ADC conversion
[7:0]	DL	8 low-order bits of the result by ADC channel 8 after ADC conversion

25.4.13 ADC9_DR (0x0312, 0x0313)

ADC9_DRH(0x0312)								
Bit	15	14	13	12	11	10	9	8
Name	RSV				DH[11:8]			
Type	-	-	-	-	R	R	R	R
Reset	-	-	-	-	0	0	0	0
ADC9_DRL(0x0313)								
Bit	7	6	5	4	3	2	1	0
Name	DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:12]	RSV	Reserved
[11:8]	DH	4 high-order bits of the result by ADC channel 9 after ADC conversion
[7:0]	DL	8 low-order bits of the result by ADC channel 9 after ADC conversion

25.4.14 ADC10_DR (0x0314, 0x0315)

ADC10_DRH(0x0314)								
Bit	15	14	13	12	11	10	9	8
Name	RSV				DH[11:8]			
Type	-	-	-	-	R	R	R	R
Reset	-	-	-	-	0	0	0	0
ADC10_DRL(0x0315)								
Bit	7	6	5	4	3	2	1	0
Name	DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:12]	RSV	Reserved
[11:8]	DH	4 high-order bits of the result by ADC channel 10 after ADC conversion
[7:0]	DL	8 low-order bits of the result by ADC channel 10 after ADC conversion

25.4.15 ADC11_DR (0x0316, 0x0317)

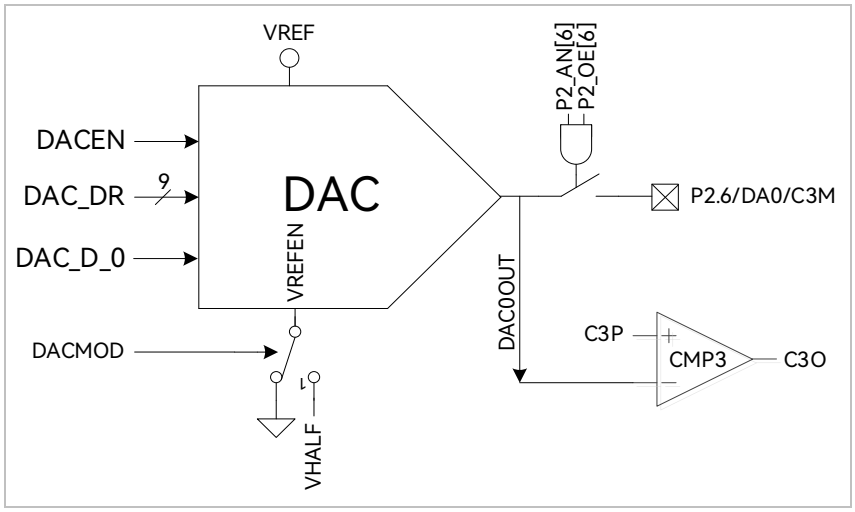
ADC11_DRH(0x0316)								
Bit	15	14	13	12	11	10	9	8
Name	RSV				DH[11:8]			
Type	-	-	-	-	R	R	R	R
Reset	-	-	-	-	0	0	0	0
ADC11_DRL(0x0317)								
Bit	7	6	5	4	3	2	1	0
Name	DL[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:12]	RSV	Reserved
[11:8]	DH	4 high-order bits of the result by ADC channel 11 after ADC conversion
[7:0]	DL	8 low-order bits of the result by ADC channel 11 after ADC conversion

26 DAC

26.1 DAC Functional Block Diagram

Figure 26-1 DAC Functional Block Diagram



Note

- DAC output has no current drive capability and can only carry capacitive load. To carry resistive load, operational amplifiers are used to follow the voltage output.
- Configure P2_AN[6] = 1 and P2_OE[6] = 1. DAC outputs the data to P2.6/DAC pin.
- Configure VREF_VHALF_CR[VREFEN] = 1 and DAC_CR[DACEN] = 1. DAC uses VREF as the reference voltage.

26.2 DAC Registers

26.2.1 DAC_CR (0x4035)

Bit	7	6	5	4	3	2	1	0
Name	DACEN	DACMOD	RSV					
Type	R/W	R/W	-	-	-	-	-	-
Reset	0	0	-	-	-	-	-	-

Bit	Name	Description
[7]	DACEN	DAC Enable 0: Disable 1: Enable

[6]	DACMOD	DAC Mode Setting 0: Full-voltage Output Mode. DAC output voltage ranges from 0 to VREF. 1: Half-voltage Output Mode. DAC output voltage ranges from VHALF to VREF.
[5:0]	RSV	Reserved

26.2.2 DAC_DR (0x404B)

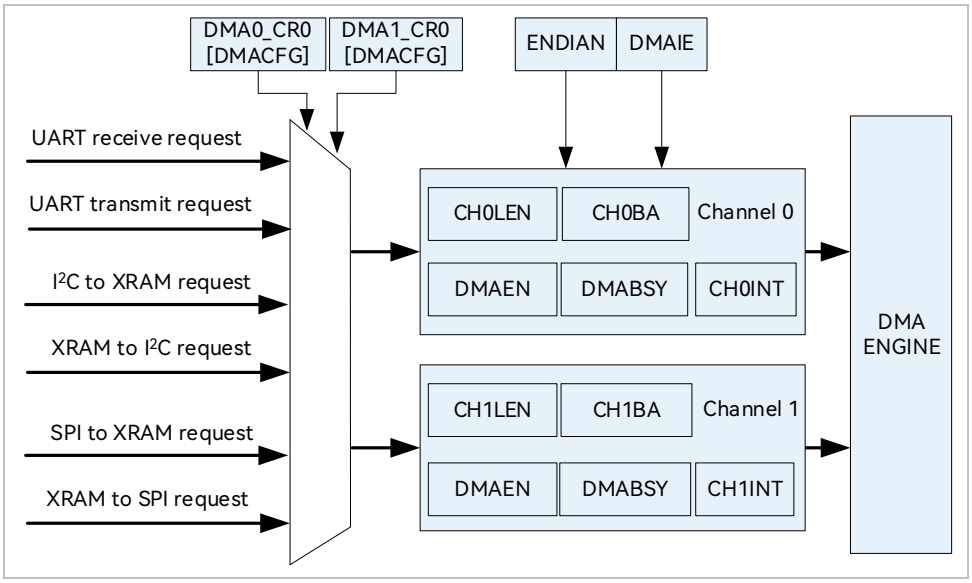
Bit	7	6	5	4	3	2	1	0
Name	DAC_DR							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	DAC_DR	Data Input of DAC Controller

27 DMA

27.1 DMA Instructions

Figure 27-1 Functional Block Diagram of DMA Module



The DMA module is a dual-channel DMA controller, which performs direct data transfer between peripherals (SPI, UART, I²C) and XRAM. DMA accessing to XRAM does not interfere with the normal CPU read/write operation to XRAM. The length of the transferred data and the start address of XRAM access are configurable. Data transfer mode is configurable and interrupt can be enabled.

DMA operations are as follows:

1. Configure and enable the peripheral, and set input and output channels taken over by DMA by DMAx_CR0[DMACFG];
2. Configure DMA interrupt enable, transfer order, transfer length and XRAM start address. Write “1” to DMAx_CR0[DMAEN] and DMAx_CR0[DMABSY] to start DMA;
3. Clear the interrupt flag bit after data transfer;
4. Set DMAx_CR0[DMABSY] to “1” to start DMA again.

27.2 DMA Registers

27.2.1 DMA0_CR0 (0x403A)

Bit	7	6	5	4	3	2	1	0
Name	DMAEN	DMABSY	DMACFG			DMAIE	ENDIAN	DMAIF
Type	R/W	R/W1	R/W	R/W	R/W	R/W	R/W	R/W0
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	DMAEN	DMA Channel 0 Enable 0: Disable 1: Enable
[6]	DMABSY	DMA Channel 0 Start/Busy Flag Read: 0: Channel 0 is idle. 1: Channel 0 is busy. Write: 0: No effect 1: Channel 0 starts for data transfer
[5:3]	DMACFG	DMA Channel 0 Peripherals and Transfer Direction Selection 000: From UART to XRAM 001: From XRAM to UART 010: From I²C to XRAM 011: From XRAM to I²C 100: From SPI to XRAM 101: From XRAM to SPI Note It cannot be configured when channel 0 is busy.
[2]	DMAIE	DMA Interrupt Request Enable 0: Disable 1: Enable. When the interrupt flag CH0INT or CH1INT is “1”, DMA module sends the interrupt request to MCU.
[1]	ENDIAN	DMA Data Transfer Sequence 0: High bytes are received or sent first 1: Low bytes are received or sent first Note This bit is set for 16-bit data mode, and shall be configured to “0” for 8-bit data mode. It cannot be configured when Channel 0 or 1 is busy.

[0]	DMAIF	DMA Channel 0 Transfer End Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect

27.2.2 DMA1_CR0 (0x403B)

Bit	7	6	5	4	3	2	1	0
Name	DMAEN	DMABSY	DMACFG			DBGSW	DBGEN	DMAIF
Type	R/W	R/W1	R/W	R/W	R/W	R/W	R/W	R/W0
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	DMAEN	DMA Channel 1 Enable 0: Disable 1: Enable
[6]	DMABSY	DMA Channel 1 Start/Busy Read: 0: Channel 1 is idle 1: Channel 1 is busy Write: 0: No effect 1: Channel 1 starts for data transfer
[5:3]	DMACFG	DMA Channel 1 Peripherals and Direction Selection 000: From UART to XRAM 001: From XRAM to UART 010: From I²C to XRAM 011: From XRAM to I²C 100: From SPI to XRAM 101: From XRAM to SPI Note It cannot be configured when channel 1 is busy
[2]	DBGSW	Sector Targeted in Debug Mode 0: XSFR as the Debug area 1: XRAM as the Debug area
[1]	DBGEN	Debug Mode Enable DMA module works in Debug mode when DMA1_CR0[DMACFG] is set to “101” and DMA1_CR0[DBGEN] to “1”. After SPI is enabled (SPI_CR1[SPIEN] = 1), DMA

		automatically sends relevant data in the sector defined by DMA1_CR0[DBGSW] via MOSI. DMA1_CR1[CH1BA]/DMA1_CR1[CH1LEN] defines the start address and range of the relevant data. NSS pin is automatically pulled low during data transmission. After each transmission, NSS pin is automatically pulled high. 0: Disable 1: Enable Note DMA Channel 1 Interrupt is automatically disabled in debug mode.
[0]	DMAIF	DMA Channel 1 Transfer End Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to "0" 1: No effect

27.2.3 DMA0_CR1 (0x403C, 0x403D)

DMA0_CR1H(0x403C)								
Bit	15	14	13	12	11	10	9	8
Name	CH0LEN						CH0BA[9:8]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DMA0_CR1L(0x403D)								
Bit	7	6	5	4	3	2	1	0
Name	CH0BA[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:10]	CH0LEN	Read: The number of the byte that is currently transferred by DMA Channel 0 (0 denotes the first byte) Write: XRAM data transfer length of DMA Channel 0 It cannot be configured when Channel 0 is busy. When DMA0_CR0 [ENDIAN] = 1, it is recommended that CH0LEN be set to an odd number.
[9:0]	CH0BA	Start address of XRAM data transfer by DMA Channel 0 It cannot be configured when Channel 0 is busy. Note

		XRAM address space for data transfer by Channel 0: CH0BA[9:0] ~ (CH0BA[9:0] + CH0LEN[5:0])

27.2.4 DMA1_CR1 (0x403E, 0x403F)

DMA1_CR1H(0x403E)								
Bit	15	14	13	12	11	10	9	8
Name	CH1LEN						CH1BA[9:8]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
DMA1_CR1L(0x403F)								
Bit	7	6	5	4	3	2	1	0
Name	CH1BA[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[15:10]	CH1LEN	Read: The number of the byte that is currently transferred by DMA Channel 1 (0 denotes the first byte) Write: XRAM data transfer length of DMA Channel 1 It cannot be configured when Channel 1 is busy. When DMA_CR0[ENDIAN] = 1, it is recommended that CH1LEN be set to an odd number.
[9:0]	CH1BA	Start address of XRAM data transfer by DMA Channel 1 It cannot be configured when Channel 1 is busy. Note XRAM address space for data transfer by Channel 1: CH1BA[9:0] ~ (CH1BA[9:0] + CH1LEN[5:0]).

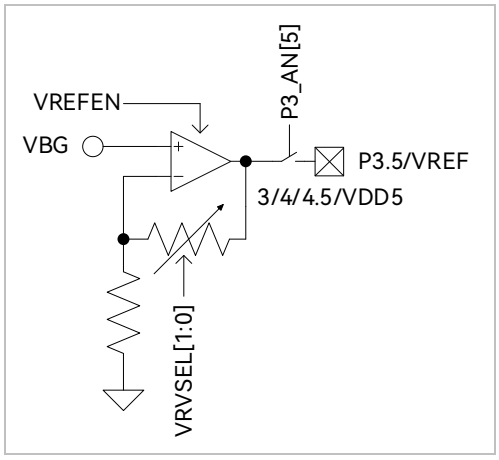
Note

When I²C is selected as DMA channel peripherals (including from I²C to XRAM and from XRAM to I²C) , START + Address interrupt of I²C communication still requires to be cleared to “0” by MCU software. In I²C slave mode, if STOP is received, I2C_SR[I2CSTP] = 0 is configured to clear I²C interrupt and restart the DMA transfer.

28 VREF

28.1 VREF Instructions

Figure 28-1 I/O Pins of VREF Module



The input and output ports of the VREF module are shown in Figure 28-1. VREF is the voltage reference generation block that provides internal voltage reference to ADC and DAC modules.

VREF is enabled when VREF_VHALF_CR[VREFEN] is set to "1". The output voltage is selected by configuring VREF_VHALF_CR[VRVSEL] (see 28.2.1 VREF_VHALF_CR (0x404F) for more details). When P3_AN[5] = 1, VREF is output to P3.5.

Note

Only the internal VDD5 can be used as the reference voltage selection terminal for FU6812S2/ FU6812V/FU6872P

28.2 VREF Register

28.2.1 VREF_VHALF_CR (0x404F)

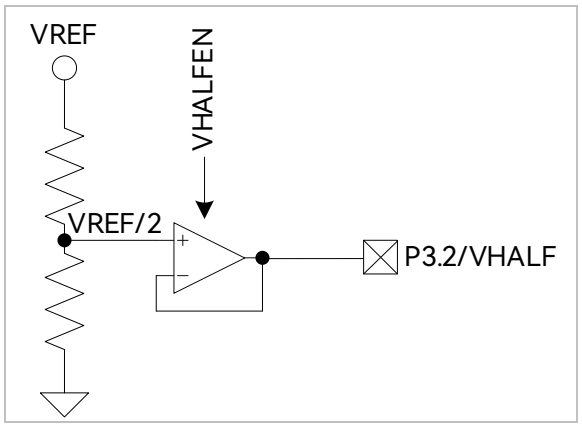
Bit	7	6	5	4	3	2	1	0
Name	VRVSEL		RSV	VREFEN	RSV	VHALFSEL		VHALFEN
Type	R/W	R/W	-	R/W	-	-	-	R/W
Reset	0	0	-	0	-	-	-	0

Bit	Name	Description
[7:6]	VRVSEL	VREF Module Output Voltage Selection 01: VDD5 00: 4.5V 11: 4V 10: 3V
[5]	RSV	Reserved
[4]	VREFEN	VREF Module Enable 0: Disable. P3_AN[5] is set to “1”, and external VREF is input from P3.5. 1: Enable. P3_AN[5] is set to “1”, and internal VREF is output to P3.5. A 1μF ~ 4.7μF capacitor can be added to improve the stability of VREF.
[3]	RSV	Reserved
[2:1]	VHALFSEL	VHALF Operation Voltage Selection (VREF Coefficient) 00: 1/8 01: 1/4 10: 25/64 11: 1/2 (Default)
[0]	VHALFEN	VHALF Enable 0: Disable 1: Enable

29 VHALF

29.1 VHALF Instructions

Figure 29-1 I/O Pins of VHALF Module



The input and output ports of VHALF module are shown in Figure 29-1. This module generates the voltage reference.

VHALF is enabled when VREF_VHALF_CR[VHALFEN] is set to “1”, and the voltage is output to P3.2.

29.2 VHALF Register

See section 28.2.1 for details.

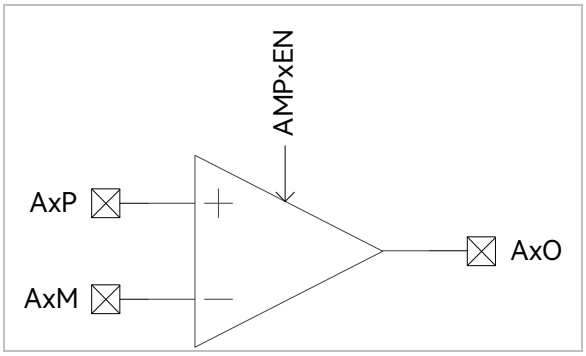
30 Operational Amplifier

30.1 Operational Amplifier Introduction

The chip integrates three high-speed independent operational amplifiers, AMP0, AMP1 and AMP2. Each operational amplifier has a separate enable bit.

FU6812N2 / FU6812S2 and FU6861N2 / FU6861NF2 integrate only one operational amplifier, AMP0.

Figure 30-1 Schematic Diagram of Operational Amplifier Module



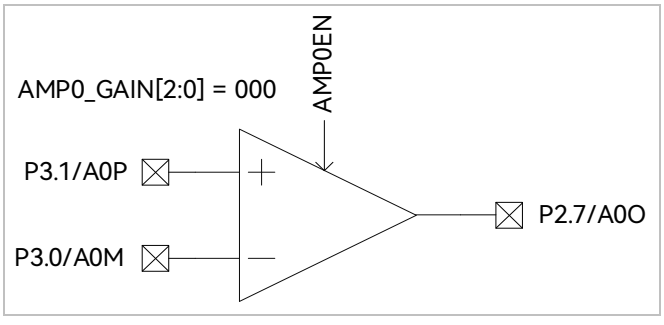
30.2 Operational Amplifier Instructions

30.2.1 Bus Current Sampling Operational Amplifier (AMP0)

AMP0 operates in three modes: normal mode, PGA differential input mode or PGA single-ended input mode.

30.2.1.1 AMP0 Normal Mode

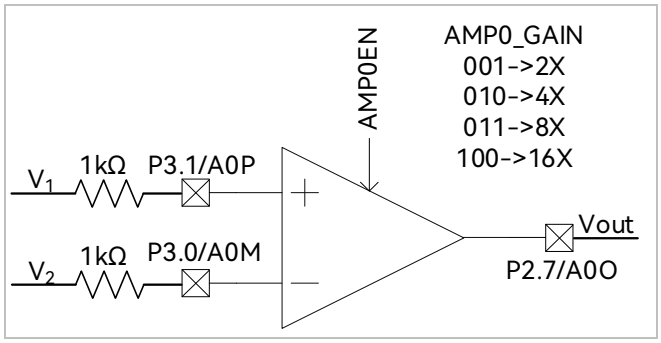
Figure 30-2 Bus Current AMP0



The I/O pins of AMP0 are shown in Figure 30-2. AMP0 is enabled when AMP_CR[AMP0EN] = 1. Before AMP0 is enabled, P2.7, P3.0, and P3.1 shall be configured to analog signal mode, i.e., P2_AN[7] is set to “1” and P3_AN[1:0] to “11”.

30.2.1.2 AMP0 PGA Differential Input Mode

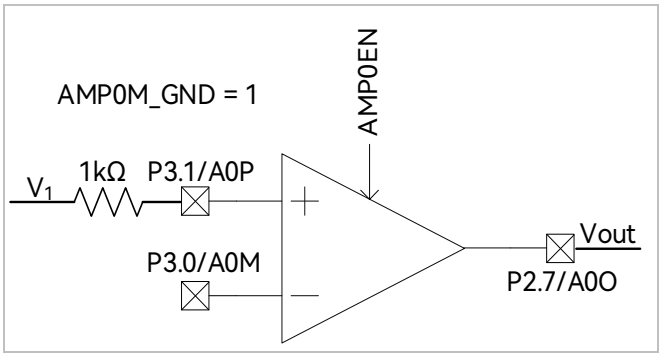
Figure 30-3 AMP0 Operating in PGA Differential Input Mode



As shown in Figure 30-3, positive and negative inputs of AMP0 are connected with a 1kΩ resistor respectively. In this mode, the amplification gain is set by CMP_AMP[AMP0_GAIN], and AMP0 is enabled when AMP_CR0[AMP0EN] = 1. The relation between output and input of operational amplifier: Vout = VHALF + (V1 - V2)*AMP0_GAIN.

30.2.1.3 AMP0 PGA Single-ended Input Mode

Figure 30-4 AMP0 Operating in PGA Single-ended Input Mode



As shown in Figure 30-4, positive input of AMP0 is connected with a 1kΩ resistor, and negative input is left floating. After TSD_ADJ[AMP0M_GND] is enabled via software, the negative input is connected to GND. In this case, VHALF is equal to 25/64*VREF.

Note

When the negative terminal of AMP0 is grounded, P3.0 cannot be used as an I/O pin

When negative input of AMP0 is connected to GND, the output voltage is calculated as follows:

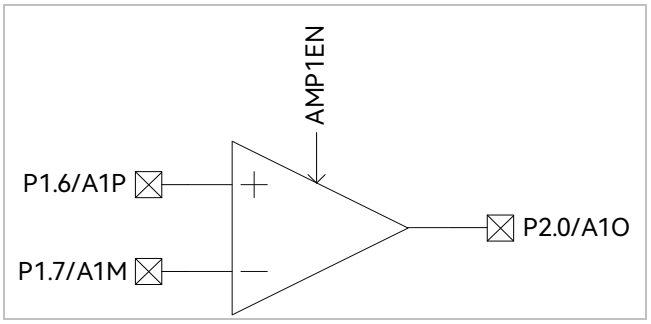
- When CMP_AMP[AMP0_GAIN] = 2, Vout = 7/6*Vhalf + 7/3*V1
- When CMP_AMP[AMP0_GAIN] = 4, Vout = 6/5*Vhalf + 24/5*V1
- When CMP_AMP[AMP0_GAIN] = 8, Vout = 11/9*Vhalf + 88/9*V1
- When CMP_AMP[AMP0_GAIN] = 16, Vout = 21/17*Vhalf + 336/17*V1

30.2.2 Phase Current Operational Amplifier (AMP1)

AMP1 operates in three modes: normal mode, PGA differential input mode or PGA single-ended input mode.

30.2.2.1 AMP1 Normal Mode

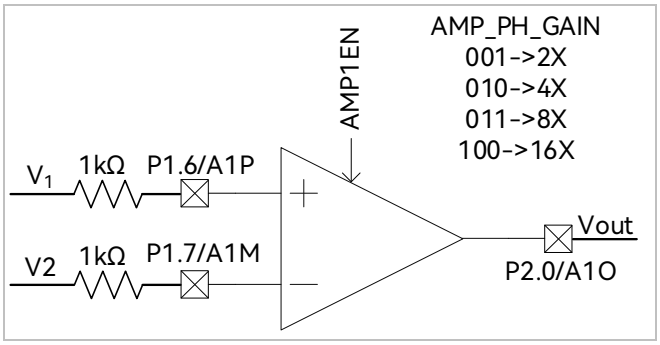
Figure 30-5 AMP1 I/O Pins



The I/O pins of AMP1 are shown in Figure 30-5. AMP1 is enabled when AMP_CR0[AMP1EN] = 1. Before AMP1 is enabled, P1.6, P1.7 and P2.0 pins shall be configured to analog signal mode, i.e., P1_AN[7:6] is set to “11” and P2_AN[0] to “1”.

30.2.2.2 AMP1 PGA Differential Input Mode

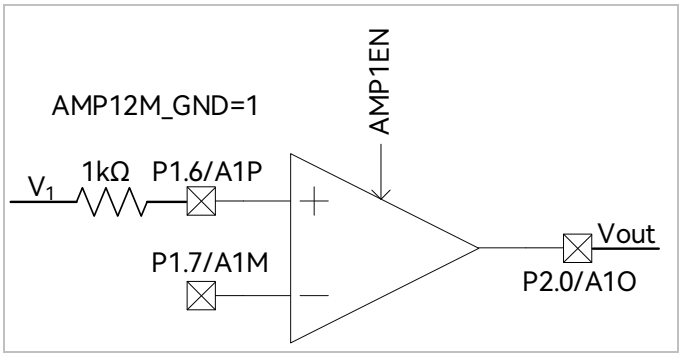
Figure 30-6 AMP1 Operating in PGA Differential Input Mode



As shown in Figure 30-6, positive and negative inputs of AMP1 are connected with a 1kΩ resistor respectively. In this mode, the amplification gain is set by CMP_AMP[AMP_PH_GAIN], and AMP1 is enabled when AMP_CR0[AMP1EN] = 1.

30.2.2.3 AMP1 PGA Single-ended Input Mode

Figure 30-7 AMP1 Operating in PGA Single-ended Input Mode



As shown in Figure 30-7, positive input of AMP1 is connected with a 1kΩ resistor, and negative input is left floating. After TSD_ADJ[AMP12M_GND] is enabled via software, the negative input is connected to GND. In this case, VHALF is equal to 25/64*VREF.

Note

When the negative terminal of AMP1 is grounded, P1.7 cannot be used as an I/O pin

When negative input of AMP1 is connected to GND, the output voltage is calculated as follows:

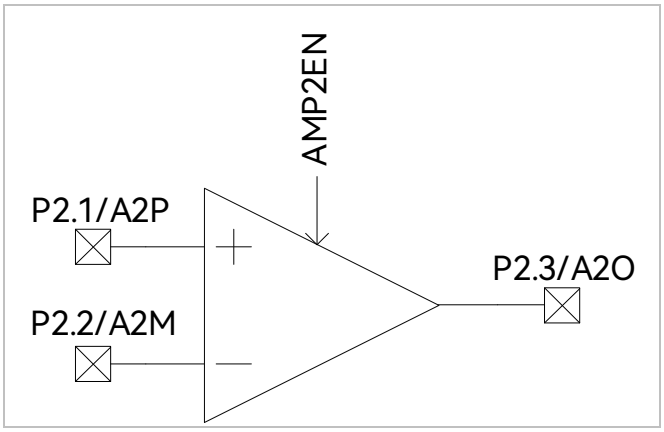
- When CMP_AMP[AMP_PH_GAIN] = 2, Vout = 7/6*Vhalf + 7/3*V1
- When CMP_AMP[AMP_PH_GAIN] = 4, Vout = 6/5*Vhalf + 24/5*V1
- When CMP_AMP[AMP_PH_GAIN] = 8, Vout = 11/9*Vhalf + 88/9*V1
- When CMP_AMP[AMP_PH_GAIN] = 16, Vout = 21/17*Vhalf + 336/17*V1

30.2.3 Phase Current Operational Amplifier (AMP2)

AMP2 operates in three modes: normal mode, PGA differential input mode or PGA single-ended input mode.

30.2.3.1 AMP2 Normal Mode

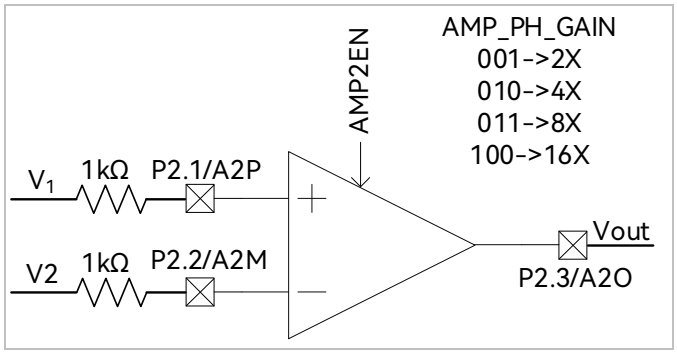
Figure 30-8 AMP2 I/O Pins



The I/O pins of AMP2 are shown in Figure 30-8. AMP2 is enabled when AMP_CR0[AMP2EN] = 1. Before APM2 is enabled, P2.1, P2.2 and P2.3 shall be configured to analog signal mode, i.e., P2_ AN[3:1] is set to “111”.

30.2.3.2 AMP2 PGA Differential Input Mode

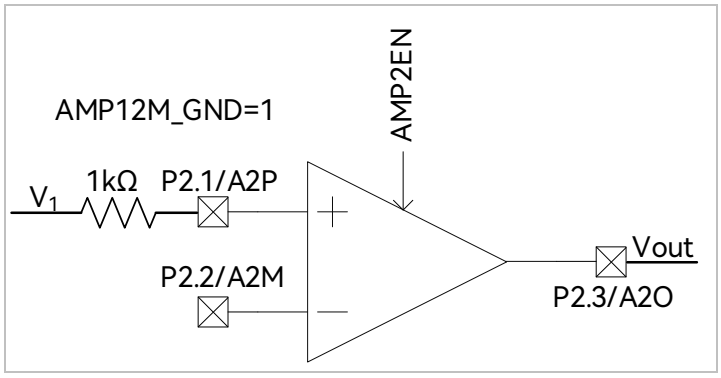
Figure 30-9 AMP2 Operating in PGA Differential Input Mode



As shown in Figure 30-9, positive and negative inputs of AMP2 are connected with a 1kΩ resistor respectively. In this mode, the amplification gain is set by CMP_AMP[AMP_PH_GAIN], and AMP2 is enabled when AMP_CR0[AMP2EN] = 1.

30.2.3.3 AMP2 PGA Single-ended Input Mode

Figure 30-10 AMP2 Operating in PGA Single-ended Input Mode



As shown in Figure 30-10, positive input of AMP2 is connected with a 1kΩ resistor, and negative input is left floating. After TSD_ADJ[AMP12M_GND] is enabled via software, the negative input is connected to GND. In this case, VHALF is equal to 25/64*VREF.

Note

When the negative terminal of AMP2 is grounded, P2.2 cannot be used as an I/O pin

When negative input of AMP2 is connected to GND, the output voltage is calculated as follows:

- When CMP_AMP[AMP_PH_GAIN] = 2, Vout = 7/6*Vhalf + 7/3*V1
- When CMP_AMP[AMP_PH_GAIN] = 4, Vout = 6/5*Vhalf + 24/5*V1
- When CMP_AMP[AMP_PH_GAIN] = 8, Vout = 11/9*Vhalf + 88/9*V1
- When CMP_AMP[AMP_PH_GAIN] = 16, Vout = 21/17*Vhalf + 336/17*V1

30.3 Operational Amplifier Registers

30.3.1 AMP_CR0 (0x404E)

Bit	7	6	5	4	3	2	1	0
Name	RSV					AMP2EN	AMP1EN	AMP0EN
Type	-	-	-	-	-	R/W	R/W	R/W
Reset	-	-	-	-	-	0	0	0

Bit	Name	Description
[7:3]	RSV	Reserved
[2]	AMP2EN	AMP2 Enable 0: Disable

		1: Enable
[1]	AMP1EN	AMP1 Enable 0: Disable 1: Enable
[0]	AMP0EN	AMP0 Enable 0: Disable 1: Enable

30.3.2 CMP_AMP (0x40F2)

Bit	7	6	5	4	3	2	1	0
Name	DAC_D_0	AMP_PH_GAIN			AMP0_GAIN			CMP3P4M_FS
Type	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset	0	-	-	-	0	0	0	0

Bit	Name	Description
[7]	DAC_D_0	LSB of the 9-bit DAC data
[6:4]	AMP_PH_GAIN	Amplification Gain Setting of AMP1&2 (with a 1kΩ external resistor) 000: The gain is configured by external circuit 001: 2X 010: 4X 011: 8X 100: 16X 101: Reserved 110/111: The gain is configured by external circuit
[3:1]	AMP0_GAIN	Amplification Gain Setting of AMP0 (with a 1kΩ external resistor) 000: The gain is configured by external circuit 001: 2X 010: 4X 011: 8X 100: 16X 101: Reserved 110/111: The gain is configured by external circuit
[0]	CMP3P4M_FS	CMP3 positive input and CMP4 negative input are switched to P3.4 0: Disable 1: Enable

30.3.3 TSD_ADJ (0x40F3)

Bit	7	6	5	4	3	2	1	0
Name	RSV				AMP12M_GND	AMP0M_GND	TSDADJ3	TSDADJ0
Type	-	-	-	-	R/W	R/W	R/W	R/W

Reset	-	-	-	-	0	0	0	0

Bit	Name	Description
[7:4]	RSV	Reserved
[3]	AMP12M_GND	After this bit is enabled, negative input of AMP1&2 (P1.7/P2.2) is connected to GND internally in PGA input mode, and VHALF = 25/64*VREF. 0: Disable 1: Enable
[2]	AMP0M_GND	After this bit is enabled, negative input of AMP0 (P3.0) is connected to GND internally in PGA input mode, and VHALF = 25/64*VREF. 0: Disable 1: Enable
[1:0]	TSDADJ3/ TSDADJ0	It works with EVT_FILT. TSDADJ3 are the most significant bits, EVT_FILT[TSDADJ] are the medium significant bits and TSDADJ0 are the least significant bits.

Table 30-1 TSDADJ and Corresponding Temperature

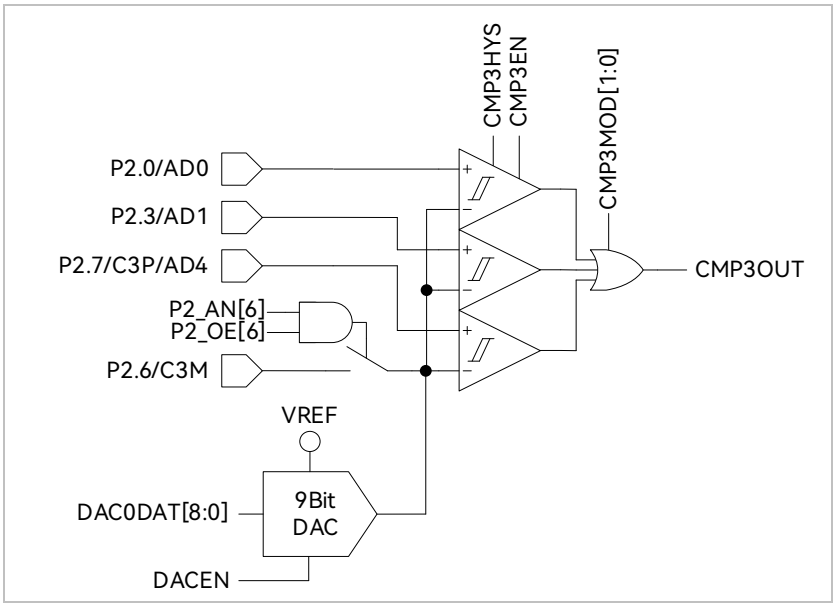
TSDADJ[3:0]	Temperature (℃)
1000	65
1001	70
1010	75
1011	80
1100	86
1101	91
1110	97
1111	103
0000	105
0001	115
0010	120
0011	128
0100	135
0101	142
0110	150
0111	Reserved

31 Comparators

31.1 Comparator Operations

31.1.1 CMP3

Figure 31-1 CMP3 I/O Pins



The I/O pins of CMP3 are shown in Figure 31-1.

CMP3 configurations are as follows:

1. The VREF source can be on-chip DAC output voltage or external circuit input voltage.
   - Apply external circuit input voltage: Set P2_AN[6] and P2_OE[6] to “1” to output the negative inputs of CMP3 to P2.6;
   - DAC output voltage: Set DAC_CR[DACEN] to “1” to enable DAC0 and then configure corresponding DAC code;
   - Select DAC output, set Set P2_AN[6] and P2_OE[6] to “1”, and place an external capacitor between P2.6 pin and GND (the recommended capacitance value is 100pF, and the output voltage stabilizes after DAC output for a period of time);
2. Configure CMP_CR1[CMP3MOD] to select single-comparator input mode, dual-comparator input mode

or triple-comparator input mode:

- When CMP_CR1[CMP3MOD] = 00, CMP3 works in Single-comparator Input Mode. The connection of input and output pins are shown in Figure 31-2.
- When CMP_CR1[CMP3MOD] = 01, CMP3 works in Dual-comparator Input Mode. The connection of input and output pins are shown in Figure 31-3.
- When CMP_CR1[CMP3MOD] = 1X, CMP3 works in Triple-comparator Input Mode. The connection of input and output pins are as shown in Figure 31-4.

3. Configure CMP_CR1[CMP3HYS] to enable or disable hysteresis voltage;
4. Set CMP_CR1[CMP3EN] = 1 to enable CMP3.

Figure 31-2 Single-comparator Input Mode

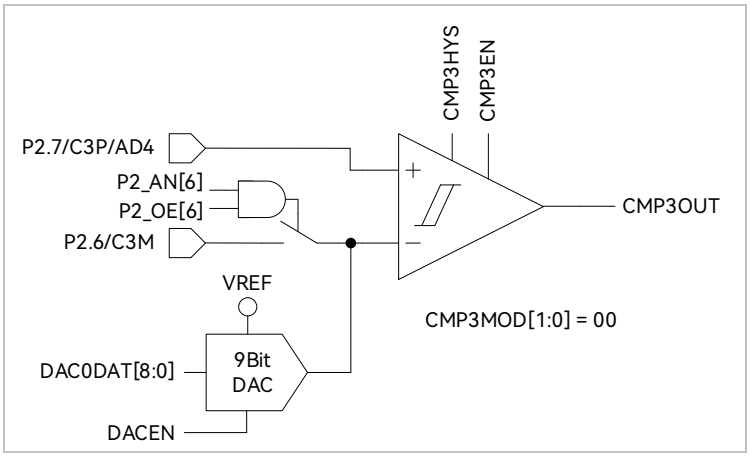


Figure 31-3 Dual-comparator Input Mode

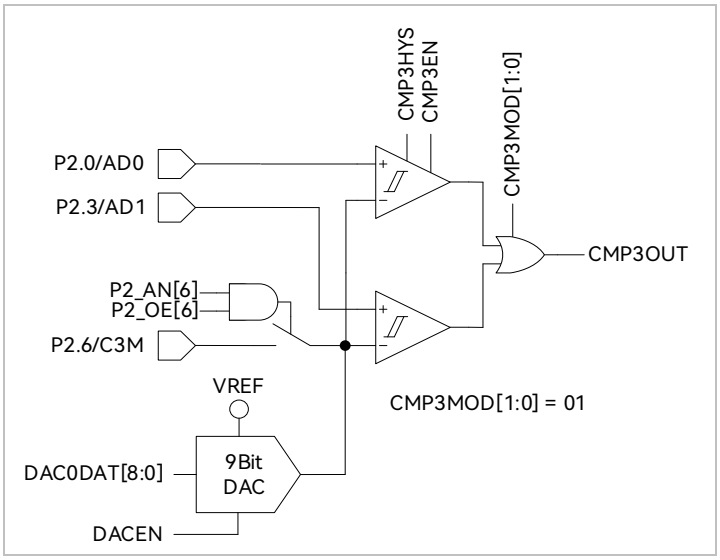
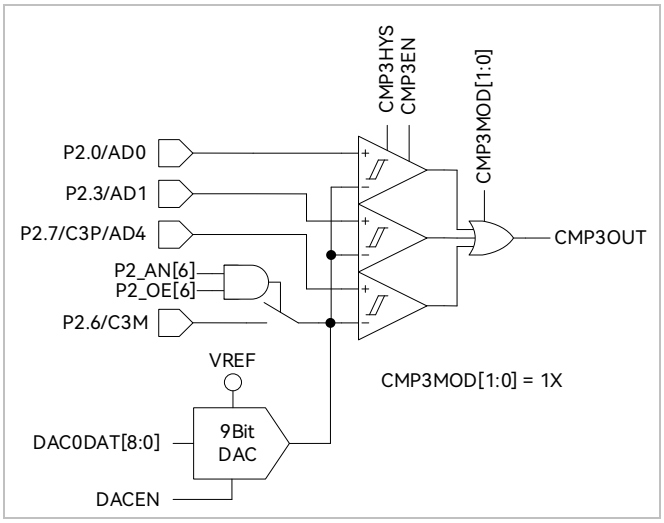


Figure 31-4 Triple-comparator Input Mode



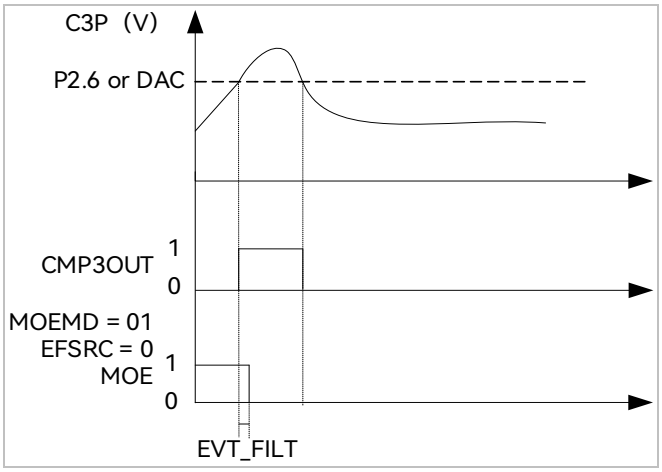
31.1.1.1 Overcurrent Protection (OCP)

When an overcurrent protection signal is generated, DRV_OUT[MOE] is automatically cleared to output idle voltage to stop motor drive for chip and motor protection. OCP feature is enabled when EVT_FILT[MOEMD] = 01, which automatically turns off the output and generates an OCP interrupt request if the current exceeds the threshold. When EVT_FILT[MOEMD] = 00, the output is not automatically turned off if the current exceeds the threshold. However, an OCP request is generated by the hardware.

The source of OCP interrupt is selected by configuring EVT_FILT[EFSRC], namely CMP3 interrupt or external interrupt INT0. When EVT_FILT[EFSRC] = 1, TCON[IT0] bit is programmed to select the trigger edge of the external interrupt INT0 which generates an OCP output. At this time, the source of OCP interrupt is INT0. When EVT_FILT[EFSRC] = 0 and CMP_CR0[CMP3IM] = 01, the OCP output is generated on the raising edge of CMP3. At this time, the source of OCP interrupt is CMP3. In triple-shunt current sampling mode, CMP_CR1[CMP3MOD] is configured to select triple-comparator input mode. When current of any phase is over the threshold, CMP3 generates an OCP signal. For other sampling modes, CMP_CR1[CMP3MOD] is configured to choose single-comparator input mode. When bus current is over the threshold, CMP3 generates an OCP signal.

Configuring EVT_FILT[EFDIV] enables the filtering of interrupt signals for OCP, and programming EVT_FILT[EFDIV] = 01/10/11 selects filter width of 4/8/16 clock cycles. When the filtering feature is enabled, the filtered signal is delayed by 4/8/16 clock cycles compared to the signal before filtering.

Figure 31-5 MOE Disabled upon Bus Overcurrent Protection



When CMP_CR0[CMP3IM] = 11, the OCP output is generated on the raising edge of CMP3. If EVT_FILT[MOEMD] = 01, the output is automatically turned off when a protection event occurs and a protection interrupt is reported. If EVT_FILT[EFSRC] = 0, the bus current protection signal is generated by CMP3, and sampled voltage on the bus is compared to generate the protection signal. Setting EVT_FILT[EFDIV] = 01/10/11 selects filter width of 4/8/16 clock cycles. When the filtering feature is enabled, the filtered signal is delayed by 4 ~ 5/8 ~ 9/16 ~ 17 clock cycles compared to the signal before filtering. As shown in Figure 31-5, when voltage on positive input of the comparator is higher than that on negative input, CMP3_OUT1 is set to “1” to generate CMP3 comparison interrupt for filtering (based on EVT_FILT[EFDIV]). MOE (DRV_OUT[MOE]) is automatically cleared to “0” to turn off six-channel outputs to implement overcurrent protection.

31.1.1.2 Cycle-by-cycle Current Limiting

The cycle-by-cycle current limiting feature is applied to square-wave-based drive control of BLDC motors. When EVT_FILT[MOEMD] = 10, MOE is automatically enabled to turn off outputs and DRV_OUT[MOE] is automatically enabled upon DRV timer overflow events. When EVT_FILT[MOEMD] = 11, MOE is automatically enabled to turn off outputs and DRV_OUT[MOE] is automatically enabled upon DRV timer overflow/underflow events or every 5 μs.

CMP_CR0[CMP3IM] must be configured for cycle-by-cycle current limiting, which generates CMP3 interrupt. The priority of CMP3 interrupt can be set to the lowest with an empty process function if the interrupt is not required.

Figure 31-6 Cycle-by-cycle Current Limiting Waveform at EVT_FILT[MOEMD] = 10

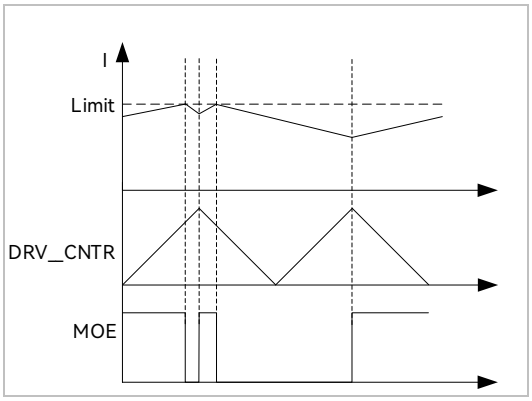
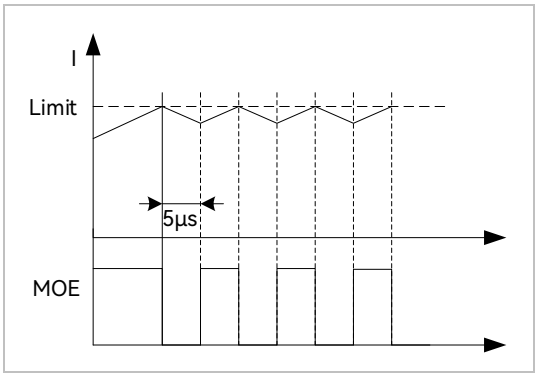


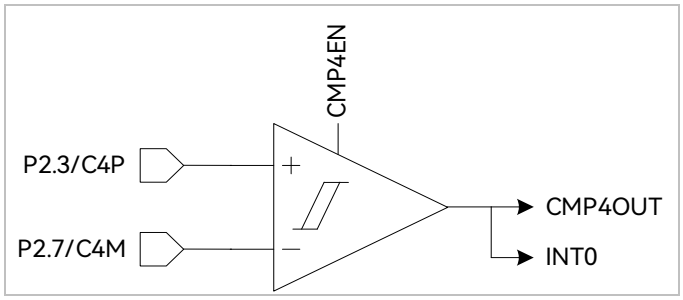
Figure 31-7 Cycle-by-cycle Current Limiting Waveform at EVT_FILT[MOEMD] = 11



31.1.2 CMP4

The I/O pins of CMP4 are shown in Figure 31-8. CMP4 output signals can be reversed on external interrupt INT0. CMP_CR[CMP3MOD] cannot be set as “01” when CMP4 is enabled. Generally, CMP4 is not used independently. It usually works with CMP3 for cycle-by-cycle current limiting protection.

Figure 31-8 CMP4 I/O Pins



Configurations are as follows:

1. Configure P2_AN[3] = 1 and P2_AN[7] = 1 to assign analog signals to P2.3 and P2.7;
2. Configure CMP_CR2[CMP4EN] = 1 to enable CMP4;

3. Clear INT0 flag bits and enable INT0;
4. Set LVSR[EXT0CFG] as “111” to select CMP4 as the source of INT0;
5. INT0 is triggered when the comparator output changes from “1” to “0”.

31.1.3 Comparator Group (CMPG)

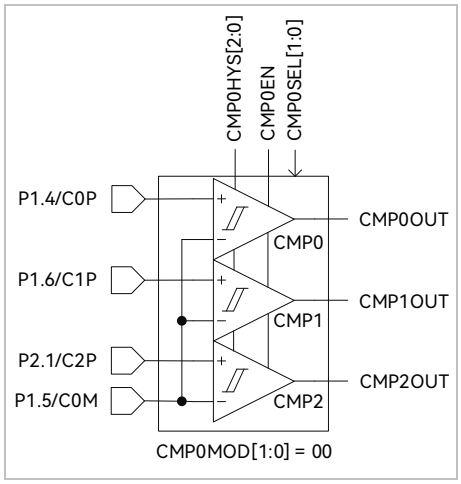
Comparator Group (CMPG) is a collection of CMP0, CMP1 and CMP2. It supports multiple comparison modes for real-time detection on rotor position and motor speed. CMP0, CMP1 and CMP2 are automatically enabled according to the configurations.

Since the 3-channel output signals CMP0OUT ~ CMP2OUT of CMPG are first sent to position detection module of Timer1, TIM1_CR3[T1TIS] must be configured as “01” to ensure comparison results held by CMP_SR is generated based on CMPG, instead of Hall signals.

31.1.3.1 Three Comparators without Built-in Resistors Mode

When CMP_CR2[CMP0MOD] = 00, CMPG works with three comparators but without built-in resistors. It is used for BEMF detection with the external virtual neutral point resistors. The I/O pins are shown in Figure 31-9. The negative inputs of the three comparators are connected to P1.5, and the positive inputs to P1.4, P1.6 and P2.1 respectively. The outputs are sent to CMP0OUT, CMP1OUT and CMP2OUT respectively. In this mode, the number of operational comparators is determined by CMP_CR2[CMP0SEL]. When CMP_CR2[CMP0SEL] = 00, all three comparators (CMP0, CMP1, and CMP2) operate simultaneously, which is the recommended configuration; when CMP_CR2[CMP0SEL] = 01, only CMP0 is active while the other two remain idle; when CMP_CR2[CMP0SEL] = 10, only CMP1 is active while the other two remain idle; when CMP_CR2[CMP0SEL] = 11, only CMP2 is active while the other two remain idle.

Figure 31-9 CMPG with Built-in Three Comparators (without Built-in Resistors)



31.1.3.2 Three Comparators and Built-in Resistors Mode

When CMP_CR2[CMP0MOD] = 01, CMPG works with three comparators and built-in resistors. The I/O pins are shown in Figure 31-10. It is used for BEMF detection with the internal virtual neutral point resistors. The outputs are sent to CMP0OUT, CMP1OUT and CMP2OUT respectively. In this mode, the number of active comparators is determined by CMP_CR2[CMP0SEL]. When set to 00, all three comparators (CMP0, CMP1, and CMP2) operate simultaneously, which is the recommended configuration. When set to 01, only CMP0 is active while the other two remain idle. When set to 10, only CMP1 is active while the other two remain idle. When set to 11, only CMP2 is active while the other two remain idle.

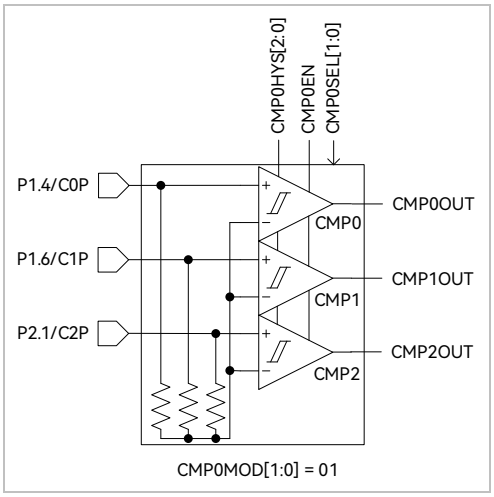
The negative inputs of the comparators are connected to the neutral point of the built-in resistor, and the positive inputs to P1.4, P1.6 and P2.1 respectively.

Configurations are as follows:

1. Set TIM1_CR3[T1TIS] = 01 to select the comparator as the input;
2. Configure CMP_CR2[CMP0MOD] = 01 to enable CMPG works with three comparators;
3. Set P1_AN[6] = 1, P1_AN[4] = 1 and P2_AN[1] = 1 to assign analog signals to the port pins;
4. Set P1_PU[4] = 0 and Reset as 0. Skip this step if no modification is required;
5. Configure CMP_CR1[CMP0HYS] to select the hysteresis voltage and Reset as 000;
6. Configure CMP_CR2[CMP0EN] = 1 to enable the comparator;
7. Configure CMP_CR2[CMP0SEL] to select one-channel or multiple-channel output(s). See Table 31-1;

8. The output results are sent to registers CMP2OUT ~ CMP0OUT.

Figure 31-10 CMP0 with Built-in Three Comparators



31.1.3.3 Triple-differential-comparator Mode

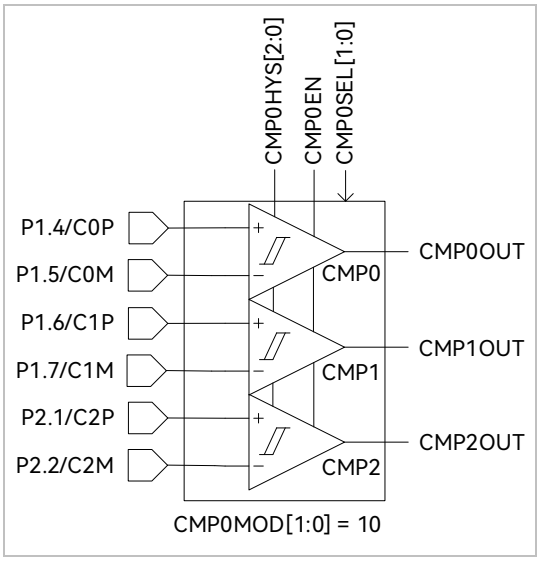
When CMP_CR2[CMP0MOD] = 10, CMPG works in triple-differential-comparator mode, where the motor rotor position is detected by differential Hall signals. The I/O pins are shown in Figure 31-11. The negative inputs of the three comparators are respectively connected to P1.5, P1.7 and P2.1, and the positive inputs to P1.4, P1.6 and P2.1. The outputs are sent to CMP0OUT, CMP1OUT and CMP2OUT respectively. In this mode, the number of active comparators is determined by the CMP_CR2[CMP0SEL] register setting. When CMP_CR2[CMP0SEL] = 00, all three comparators (CMP0, CMP1, and CMP2) operate simultaneously, which is the recommended configuration. When set to 01, only CMP0 remains active while the other two comparators are idle. When set to 10, only CMP1 is functional with the other two inactive. When configured as 11, only CMP2 operates while CMP0 and CMP1 remain disabled.

Configurations are as follows:

1. Set TIM1_CR3[T1TIS] = 01 to select the comparator as the input;
2. Configure CMP_CR2[CMP0MOD] = 10 to enable CMPG works in triple-differential-comparator mode;
3. Set P1_AN[7:4] = 1111 and P2_AN[2:1] = 11 to assign analog signals to the port pins;
4. Set P1_PU[4] = 0 and Reset as 0. Skip this step if no modification is required;
5. Configure CMP_CR1[CMP0HYS] to select the hysteresis voltage and Reset as 000;

6. Configure CMP_CR2[CMP0EN] = 1 to enable the comparator;
7. Configure CMP_CR2[CMP0SEL to select one-channel or multiple-channel output(s). See Table 31-1;
8. The output results are sent to registers CMP2OUT ~ CMP0OUT.

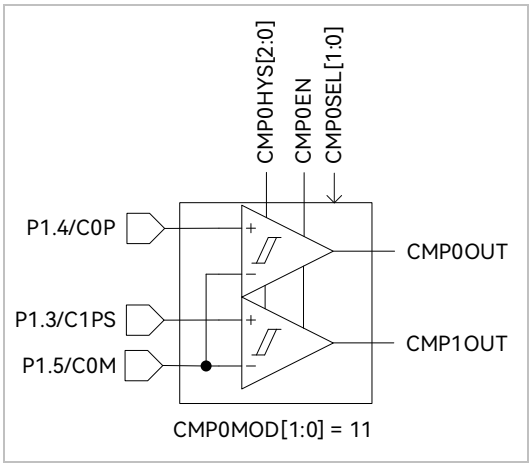
Figure 31-11 CMPG in Triple-differential-comparator Mode



31.1.3.4 Dual-comparator Mode

When CMP_CR2[CMP0MOD = 11, CMPG works in dual-comparator mode. The I/O pins are shown in Figure 31-12. The negative inputs of the two comparators are connected to P1.5, and the positive inputs to P1.4 and P1.3 respectively. The outputs are sent to CMP0OUT and CMP1OUT respectively. In this mode, the number of operational comparators is determined by the CMP_CR2[CMP0SEL] setting. When CMP_CR2[CMP0SEL] = 00, both comparators (CMP0 and CMP1) operate simultaneously, which is the recommended configuration. When set to 01, only CMP0 is active while CMP1 remains idle. When set to 10, only CMP1 is functional while CMP0 is inactive.

Figure 31-12 CMPG in Dual-comparator Mode

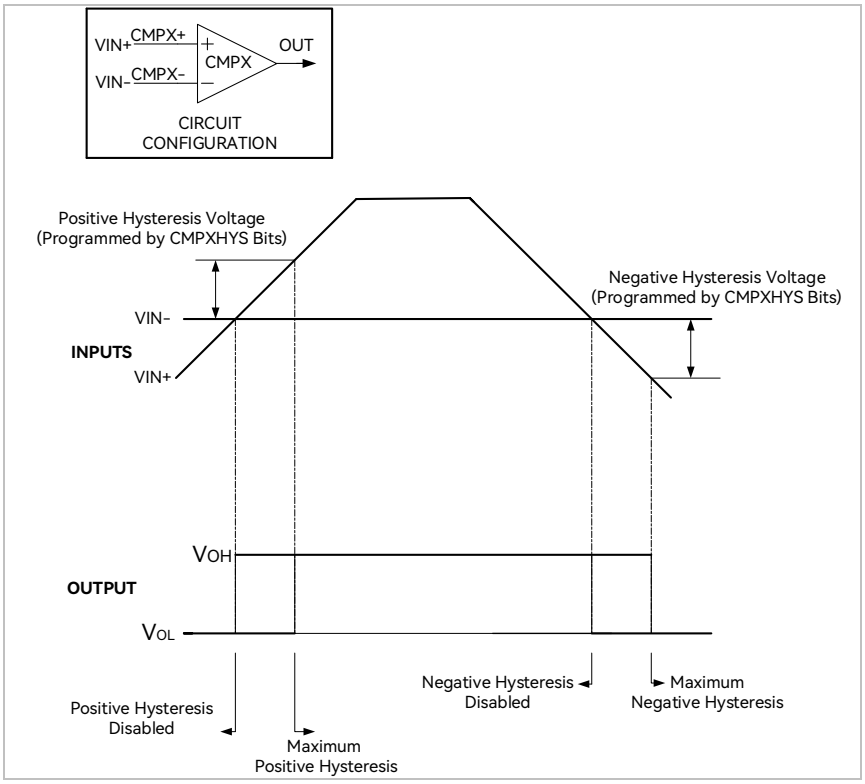


Configurations are as follows:

1. Set TIM1_CR3[T1TIS] = 01 to select the comparator as the input;
2. Configure CMP_CR2[CMP0MOD] = 11 to enable CMPG works in dual-comparator mode;
3. Set P1_AN[5:3] = 111 and P1_OE[3] = 0 to assign analog signals to the port pins;
4. Pull-up resistor of P1[5:3] can be enabled (P1_PU[5:3] = 111) or disabled (P1_PU[5:3] = 000) as required, and set Reset as 0. Skip this step if no modification is required. In dual-comparator mode, pull-up resistor of P1[5:3] is generally disabled and used for special applications.
5. Configure CMP_CR1[CMP0HYS] to select the hysteresis voltage and Reset as 000;
6. Configure CMP_CR2[CMP0EN] = 1 to enable the comparator;
7. Configure CMP_CR2[CMP0SEL] to select one-channel or multiple-channel output(s). See Table 31-1;
8. The output results are sent to registers CMP1OUT ~ CMP0OUT.

Hysteresis voltage of CMPG is set by register, and shall be properly configured according to actual demand.

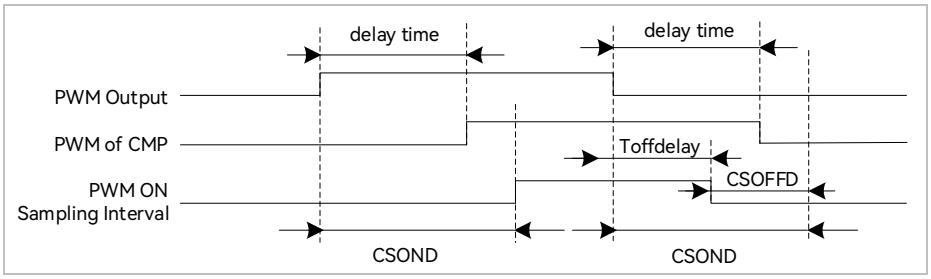
Figure 31-13 CMPG Input and Output under Hysteresis Voltage



31.1.4 Comparator Sampling

The comparator sampling feature is used for the square-wave control and RSD (tailwind/headwind detection), which eliminates the switching interference from driving circuit. See section Sampling for square-wave control.

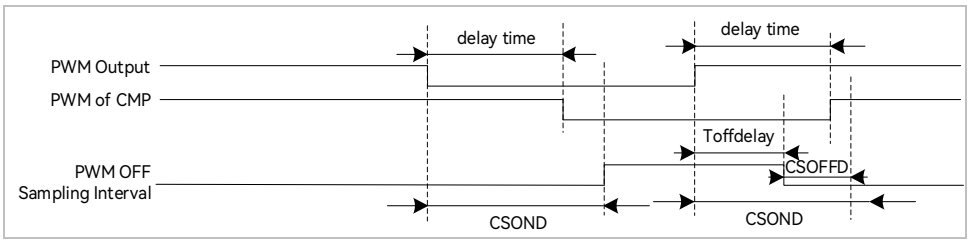
Figure 31-14 PWM ON Sampling Mode



There is a delay from the PWM output to the output of the comparator, which is mainly affected by the following factors: resistance value of drive resistor, MOS switch speed, and input delay and hysteresis settings of the comparator. As shown in the figure, the delay time is from the chip output to the comparator output. When high-level sampling is performed, the sampling interval shall be enveloped by actual high-level output of the comparator. First, the sampling ON-delayed time CMP_SAMR[CSOND] is set to

overcome output delay and ringing due to MOS switches. At the end of the sampling interval, CMP_SAMR[CSOND] is delayed after the falling edge of PWM, at which time the actual sampling window has exceeded the corresponding high-level interval. Configure the sampling stop advance time CMP_SAMR[CSOFFD] so that the sampling window closes after a delay of Toffdelay (where Toffdelay = CMP_SAMR[CSOND] - CMP_SAMR[CSOFFD]) following the falling edge of the PWM output. By configuring both CMP_SAMR[CSOND] and CMP_SAMR[CSOFFD], the sampling interval can be positioned within the actual high-level duration of the comparator output.

Figure 31-15 PWM OFF Sampling Mode



Similarly, when low-level sampling is performed, the delayed sampling time in PWM ON mode CMP_SAMR[CSOND] and advanced sampling time in PWM OFF mode CMP_SAMR[CSOFFD] shall be set reasonably to ensure that the actual sampling interval is located in the actually low-level output interval of the comparator.

Method for measuring the delay of PWM output to comparator: Set CMP_CR3[SAMSEL] = 00 to disable the comparator sampling delay feature. Enable the PWM output and comparator, manually rotate the motor to change the comparator value, and measure the delay between the PWM output and the comparator output.

31.2 Comparator Registers

31.2.1 CMP_CR0 (0xD5)

Bit	7	6	5	4	3	2	1	0
Name	CMP3IM		CMP2IM		CMP1IM		CMP0IM	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:6]	CMP3IM	CMP3 Interrupt Mode See descriptions on CMP_CR0[CMP0IM]
[5:4]	CMP2IM	CMP2 Interrupt Mode See descriptions on CMP_CR0[CMP0IM]
[3:2]	CMP1IM	CMP1 Interrupt Mode See descriptions on CMP_CR0[CMP0IM]
[1:0]	CMP0IM	CMP0 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge. 10: An interrupt is generated upon falling edge. 11: An interrupt is generated upon both rising/falling edges.

31.2.2 CMP_CR1 (0xD6)

Bit	7	6	5	4	3	2	1	0
Name	HALLSEL	CMP3MOD		CMP3EN	CMP3HYS	CMP0HYS		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	HALLSEL	Hall Input Selection 0: P0.2/P3.7/P3.6 1: P1.4/P1.6/P2.1
[6:5]	CMP3MOD	CMP3 Mode Selection See Figure 31-1 for details. The negative input is connected to P2.6 or DAC output. 00: Single-comparator mode, where P2.7 is connected to the positive input, as shown in Figure 31-2. 01: Dual-comparator mode, where P2.0 and P2.3 are connected to the positive inputs, as shown in Figure 31-3 1X: Triple-comparator mode, where P2.0, P2.3 and P2.7 are connected to the positive inputs, as shown in Figure 31-4
[4]	CMP3EN	CMP3 Enable

		0: Disable 1: Enable
[3]	CMP3HYS	CMP3 Hysteresis Voltage Selection 0: No hysteresis 1: Hysteresis voltage is selected
[2:0]	CMP0HYS	CMP0/1/2 Hysteresis Voltage Selection 000: No hysteresis 001: ±2.5mV 010: -5mV 011: +5mV 100: ±5mV 101: -10mV 110: +10mV 111: ±10mV

31.2.3 CMP_CR2 (0xDA)

Bit	7	6	5	4	3	2	1	0
Name	CMP4EN	CMP0MOD		CMP0SEL		CMP0CSEL		CMP0EN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	CMP4EN	CMP4 Enable 0: Disable 1: Enable
[6:5]	CMP0MOD	CMPG Mode Setting 00: CMP0 with built-in three comparators (without built-in resistors), as shown in Figure 31-9 01: CMPG with three comparators and built-in resistors, as shown in Figure 31-10 10: CMPG in triple-differential-comparator mode, as shown in Figure 31-11 11: CMPG in dual-comparator mode, as shown in Figure 31-12
[4:3]	CMP0SEL	CMPG Pin Combination Selection, used with CMP_CR2[CMP0MOD]. It is set to 00 by default. In square-wave drive applications, TIM1_DBRx[T1CPE] automatically controls CMP_CR2[CMP0SEL] to enable or disable each comparator. Table 31-1 Function Description of CMPG Port and CMP_CR2[CMP0MOD] Combination

CMP0MOD	CMP0SEL	Descriptions
00	00	CMP0/1/2 work simultaneously. The inputs of these 3 comparators are connected to neutral point of built-in resistor. The hardware automatically compares the positive inputs C0P, C1P and C2P with

				C0M. The output results are sent to CMP0OUT, CMP1OUT and CMP2OUT respectively.
			01	Only CMP0 works. The positive input is connected to C0P, and the negative input to neutral point of the built-in BEMF resistor. The output results are sent to CMP0OUT.
			10	Only CMP1 works. The positive input is connected to C1P, and the negative input to neutral point of the built-in BEMF resistor. The output results are sent to CMP1OUT.
			11	Only CMP2 works. The positive input is connected to C2P, and the negative input to neutral point of the built-in BEMF resistor. The output results are sent to CMP2OUT.
		01	00	CMP0/1/2 work simultaneously. The inputs of these 3 comparators are connected to neutral point of built-in resistor. The hardware automatically compares the positive inputs C0P, C1P and C2P with C0M. The output results are sent to CMP0OUT, CMP1OUT and CMP2OUT respectively.
			01	Only CMP0 works. The positive input is connected to C0P, and the negative input to neutral point of the built-in BEMF resistor. The output results are sent to CMP0OUT.
			10	Only CMP1 works. The positive input is connected to C1P, and the negative input to neutral point of the built-in BEMF resistor. The output results are sent to CMP1OUT.
			11	Only CMP2 works. The positive input is connected to CMP2P, and the negative input to neutral point of the built-in BEMF resistor. The output results are sent to CMP2OUT.
		10	00	CMP0/1/2 work simultaneously. The positive inputs of these 3 comparators are connected to C0P, C1P, and C2P respectively, and the negative inputs to C0M, C1M, and C2M respectively. The output results are sent to CMP0OUT, CMP1OUT and CMP2OUT respectively.
			01	Only CMP0 works. The positive input of the comparator is connected to C0P, and the negative input to C0M. The output results are sent to CMP0OUT.

			10	Only CMP1 works. The positive input of the comparator is connected to C1P, and the negative input to C1M. The output results are sent to CMP01UT.
			11	Only CMP2 work. The positive input of the comparator is connected to C2P, and the negative input to C2M. The output results are sent to CMP2OUT.
		11	00	CMP0/1 work simultaneously. The positive inputs of the comparator are connected to C0P and C1PS respectively, and negative inputs to C0M. The output results are sent to CMP0OUT and CMP1OUT respectively.
			01	Only CMP0 works. The positive input of the comparator is connected to C0P, and negative input to C0M. The output results are sent to CMP0OUT.
			10	Only CMP1 works. The positive input of the comparator is connected to C1PS, and negative input to C0M. The output results are sent to CMP1OUT.
			11	Reserved
[2:1]	CMP0CSEL	CMP0/1/2 Polling Speed Selection 00: Normal polling 01: Fast polling 10: Reduced polling 11: Low-speed polling		
[0]	CMP0EN	CMP0/1/2 Enable 0: Disable 1: Enable		

31.2.4 CMP_CR3 (0xDC)

Bit	7	6	5	4	3	2	1	0
Name	CMPDTEN	DBGSEL		SAMSEL		RSV		
Type	R/W	R/W	R/W	R/W	R/W	-	-	-
Reset	0	0	0	0	0	-	-	-

Bit	Name	Description
[7]	CMPDTEN	Comparator Deadtime Sampling Enable 0: Disable 1: Enable

[6:5]	DBGSEL	Debug Output Selection, connected to P0.1 pin 00: Debug Output Disable 01: Freewheeling shielding is completed and ZCP signal is detected. See Diode Freewheeling Masking. 10: ADC Trigger Signal 11: Comparator Sampling Interval. See Comparator Debugging.
[4:3]	SAMSEL	Sampling Delay of CMP0, CMP1, CMP2 and ADC in PWM ON/OFF Modes. See Comparator Sampling. 00: Sampling at both PWM ON and OFF modes without time delay 01: Sampling at PWM OFF only, with time delay according to CMP_SAMR 10: Sampling at PWM ON only, with time delay according to CMP_SAMR 11: Sampling at both PWM ON and OFF, with time delay according to CMP_SAMR
[2:0]	RSV	Reserved

31.2.5 CMP_SAMR (0x40AD)

Bit	7	6	5	4	3	2	1	0
Name	CSOND				CSOFFD			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bit	Name	Description
[7:4]	CSOND	CMP0/1/2 Delayed Sampling Time in PWM ON Mode When PWM module switches from OFF to ON or from ON to OFF, turn-on/off of the power IC affects input signal of the comparator. In this case, CMP_SAMR[CSOND] is configured to delay the sampling of CMP0/1/2. The delay generated by drive circuit shall be taken into account when CMP_SAMR[CSOND] is calculated. If MCU clock runs at 24MHz(41.67ns) Delayed sampling time in PWM ON mode = CSOND x 41.67 x 8ns Note › CMP_SAMR[CSOND] must be greater than or equal to ≥ CMP_SAMR[CSOFFD] › See section Sampling for square-wave control and section RSD Comparator Sampling for RSD.
[3:0]	CSOFFD	CMP0/1/2 Advanced Sampling Time in PWM OFF Mode When PWM module switches from OFF to ON or from ON to OFF, turn-on/off of the power IC affects input signal of the comparator. In this case, CMP_SAMR[CSOFFD] is configured to reduce comparator interference. If MCU clock runs at 24MHz(41.67ns) Advanced sampling time in PWM OFF mode = CSOFFD x 41.67 x 8ns

		Note › CMP_SAMR[CSOND] must be greater than or equal to ≥ CMP_SAMR[CSOFFD] › See section Sampling for square-wave control and section RSD Comparator Sampling for RSD.

31.2.6 CMP_SR (0xD7)

Bit	7	6	5	4	3	2	1	0
Name	CMP3IF	CMP2IF	CMP1IF	CMP0IF	CMP3OUT	CMP2OUT	CMP1OUT	CMP0OUT
Type	R/W0	R/W0	R/W0	R/W0	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	CMP3IF	CMP3 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[6]	CMP2IF	CMP2 Interrupt Flag TIM1_CR3[T1TIS] must be configured to “01”, otherwise, it is the Hall interrupt flag. Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[5]	CMP1IF	CMP1 Interrupt Flag TIM1_CR3[T1TIS] must be configured to “01”, otherwise, it is the Hall interrupt flag. Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect
[4]	CMP0IF	CMP0 Interrupt Flag TIM1_CR3[T1TIS] must be configured to “01”, otherwise, it is the Hall interrupt flag. Read: 0: No Interrupt Pending 1: Interrupt Pending Write:

		0: This bit is cleared to “0” 1: No effect
[3]	CMP3OUT	CMP3 Comparison Result 0: CMP3 comparison result is 0. 1: CMP3 comparison result is 1.
[2]	CMP2OUT	CMP2 Comparison Result TIM1_CR3[T1TIS] must be configured to “01”, otherwise, the results are generated by Hall signals. 0: CMP2 comparison result is 0. 1: CMP2 comparison result is 1.
[1]	CMP1OUT	CMP1 Comparison Result TIM1_CR3[T1TIS] must be configured to “01”, otherwise, the results are generated by Hall signals. 0: CMP1 comparison result is 0. 1: CMP1 comparison result is 1.
[0]	CMP0OUT	CMP0 comparison result TIM1_CR3[T1TIS] must be configured to “01”, otherwise, the results are generated by Hall signals. 0: CMP0 comparison result is 0. 1: CMP0 comparison result is 1.

31.2.7 EVT_FILT (0xD9)

Bit	7	6	5	4	3	2	1	0
Name	TSDEN	TSDADJ2	TSDADJ1	MOEMD		EFSRC	EFDIV	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	0	0	0	0	0

Bit	Name	Description
[7]	TSDEN	TSD Enable 0: Disable 1: Enable
[6]	TSDADJ2	TSD Temperature Selection. See Table 30-1
[5]	TSDADJ1	TSD Temperature Selection. See Table 30-1
[4:3]	MOEMD	MOE Cleared and Enabled by Hardware MOE is cleared and enabled by hardware upon current protection event. 00: MOE is not automatically cleared. 01: MOE is automatically cleared. 10: MOE is automatically cleared and enabled by hardware upon DRV timer overflow events (for square-wave drive). 11: MOE is automatically cleared and enabled automatically upon DRV timer overflow/underflow events or every 5 μs (for square-wave drive).
[2]	EFSRC	Input Source of Filtering Module Upon Current Protection Event

		0: CMP3 interrupt 1: INT0 interrupt
[1:0]	EFDIV	Filter Width for Current Protection 00: Disable 01: 4 system clock cycles 10: 8 system clock cycles 11: 16 system clock cycles

32 Power Supply

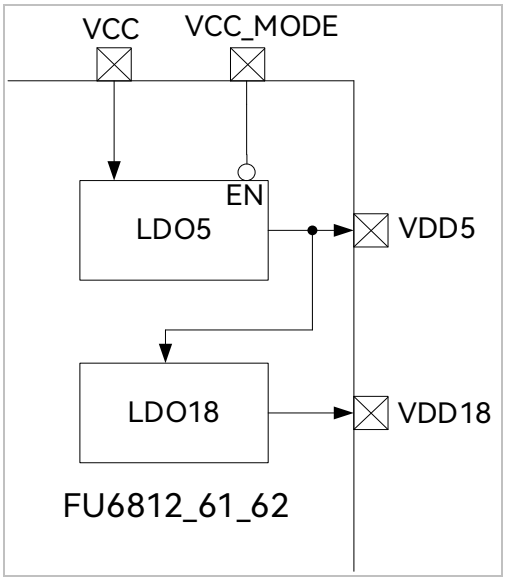
32.1 LDO

FU6812_61_62 contains two LDO output modules: LDO5 and LDO18.

FU6872 contains three LDO output modules: BUCK, LDO5, and LDO18.

32.1.1 FU6812_61_62 LDO Operations

Figure 32-1 Functional Block Diagram of Power Supply of FU6812_61_62



The I/O pins of LDO module is shown in Figure 32-1. The LDO module converts the input supply voltage to 5V VDD5 or 1.85V VDD18 as the power supply for built-in analog and digital modules. Wherein, VDD5 can be selected to be generated either by the internal LDO5 or supplied externally, as determined by VCC_MODE.

- FU6812x2:
  - Single-power high voltage supply mode: (VCC_MODE = 0), VCC = 5V ~ 24V。See Figure 32-2
  - Duaal-power mode: (VCC_MODE = 1), VCC ≥ VDD5, VCC = 5V ~ 36V, VDD5 = 5V。See Figure 32-3
  - Single-power low voltage supply mode: (VCC_MODE = 1), VCC = VDD5 = 3V ~ 5.5V。See Figure 32-4
- FU6862L/FU6862Q:

- Single-power high voltage supply mode: VCC = 12V ~ 20V。See Figure 32-2.

- FU6861Q2:
  - Mode1: VCC_MODE = 0, VCC = 5V ~ 24V，VDRV = 7V ~ 18V
  - Mode2: VCC_MODE = 1, VCC = VDD5 = 3V ~ 5.5V，VDRV = 7V ~ 18V
- FU6861N2/FU6861NF2:
  - Mode1: VCC = 5V ~ 24V，VDRV = 7V ~ 18V

Note

VDD5 is the voltage of VCC_MODE = 1

Figure 32-2 Connection of Single-power High Voltage Supply mode of FU6812_61_62

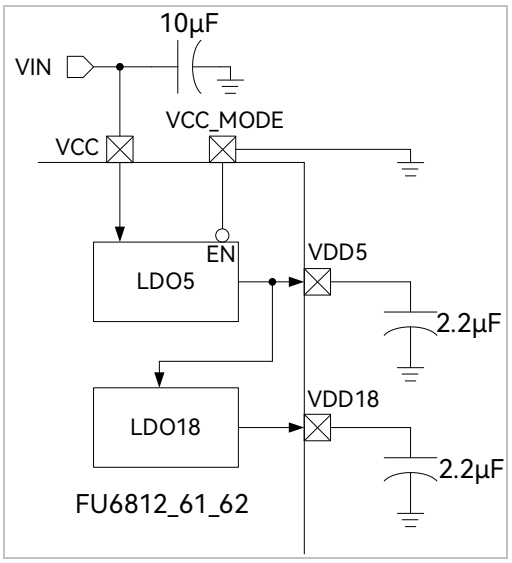


Figure 32-3 Connection of Dual-power Supply mode of FU6812_61_62

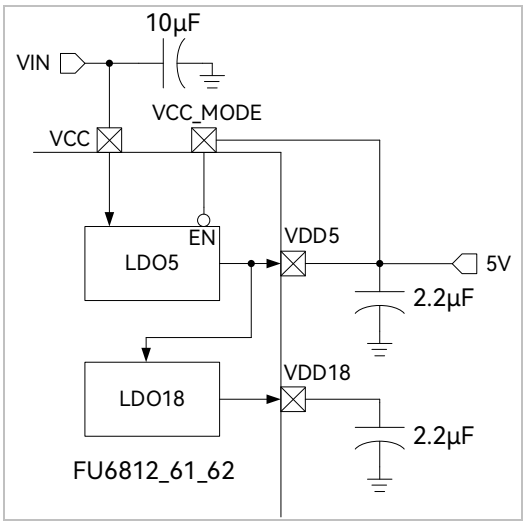
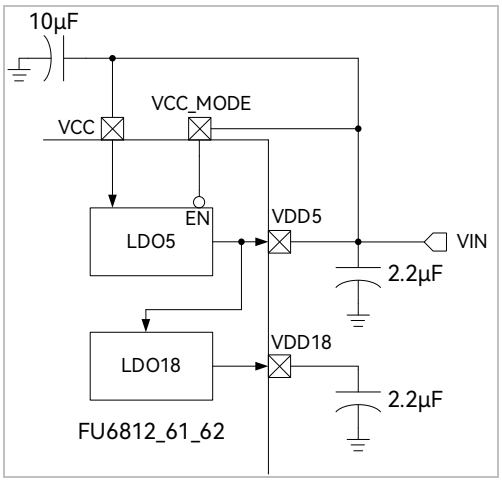
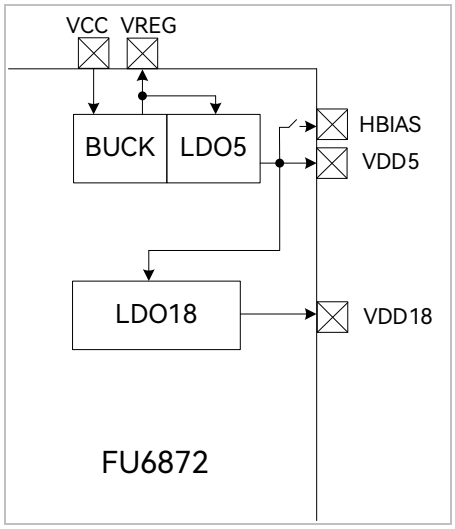


Figure 32-4 Connection of Single-power Low Voltage Supply mode of FU6812_61_62



32.1.2 FU6872 LDO Operations

Figure 32-5 Functional Block Diagram of Power Supply of FU6872



The I/O ports corresponding to the FU6872 LDO module are shown in Figure 32-5. The BUCK circuit generates VREG (12V) as the input for LDO5. The function of the LDO is to step down the input voltage to 5V (VDD5) and 1.85V (VDD18), which supply power to the analog and digital modules within the chip, respectively.

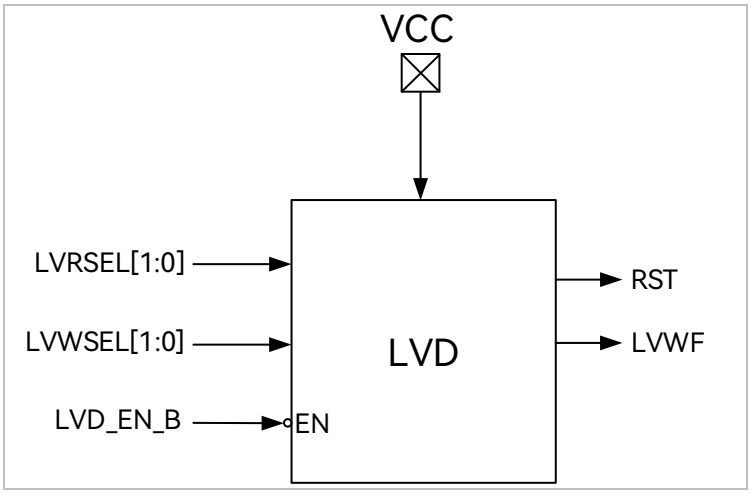
32.2 Low Voltage Detection (LVD)

32.2.1 LVD Introduction

The low voltage detection includes low voltage warning and low voltage reset.

32.2.2 LVD Operations

Figure 32-6 LVD Module



Configuring CCFG1[LVD_EN_B] = 0 enables LVD module.

32.2.3 LVD Register

LVD module is enabled by configuring CCFG1[LVD_EN_B] = 0. See 37.1.1 CCFG1 (0x401E) (bits [7] and [6]) and 37.1.2 CCFG2 (0x401D) (bits [7:6] and [1:0]) for the configurations of low voltage warning threshold voltage and low voltage reset threshold voltage.

32.2.3.1 LVSR (0xDB)

Bit	7	6	5	4	3	2	1	0
Name	RSV		EXT0CFG			TSDF	LVWF	LVWIF
Type	-	-	R/W	R/W	R/W	R	R	R/W0
Reset	-	-	0	0	0	0	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5:3]	EXT0CFG	INT0 Pin Selection 000: P0.0 001: P0.1 010: P0.2

		011: P0.3 100: P0.4 101: P0.5 110: P0.6 111: CMP4 Output Note If EXT0[EXT0_P11] = 1 is configured, it enables P1.1 as the interrupt trigger source for external interrupt INT0, and the interrupt request from P1.1 has a higher priority
[2]	TSDF	Over Temperature State Indicator 0: The current temperature does not exceed the threshold 1: The current temperature exceeds the threshold Note This flag bit often works with TSD interrupt flag TCON[TSDIF]
[1]	LVWF	VCC Low Voltage (LV) Flag This bit indicates whether the chip is in the low voltage state. 0: The chip is not in the LV warning state. 1: The chip is in the LV warning state.
[0]	LVWIF	VCC LV Interrupt Flag This bit indicates whether a low voltage event occurs. It is set to “1” by hardware after low voltage detection interrupt is enabled and an low voltage detection interrupt is detected. A write of “0” in software clears this bit. This bit is not set to “1” by hardware when LVD interrupt is disabled. Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0” 1: No effect Note Low-voltage detection interrupt is enabled when the bit is set to 1 by hardware

33 Flash

33.1 Flash Introduction

- 16kB Flash;
- 128 sectors in total, each with a size of 128 bytes
- The first 127 sectors support erase, write, on-line programing and in-application programming.
- Last sector (the 128th sector) cannot be erased at any time

33.2 Flash Operations

- All interrupts must be disabled before programming to ensure the security of Flash operations and avoid mis-operation of Flash using MOVX instruction during interrupt processing.
- Sector Erasure Operations:

1. Disable all interrupts by IE[EA];
2. Write 0x03 to FLA_CR;
3. Write 5A to FLA_KEY, and then 0x1F to unlock Flash;
4. Write any value to the Flash sector that is to be erased with MOVX instruction;
5. Write “1” to FLA_CR[FLAACT] to perform sector erase. After the command is executed, the Flash is automatically locked.

- Flash Programming Operations:

1. Disable all interrupts by IE[EA];
2. Write 0x01 to FLA_CR;
3. Write 0x5A to FLA_KEY, and then 0x1F to unlock Flash;
4. Write data to the specified Flash sector with MOVX instruction;
5. Write “1” to FLA_CR[FLAACT] to program 1-byte data. After this command is executed, data is written and Flash is automatically locked.

Note

- All interrupts must be disabled before programming to ensure your program is secured and prevent rom_code is written with MOVX instruction.
- It requires quite a long time for the internal circuit to completed Flash operations. For example, it costs about 120ms~150ms to erase a section.

- Each sector has a size of 128 bytes and the last sector (address range: 0x3F80 ~ 0x3FFF) cannot erased at any time. MCU is reset when any instruction in unprotected areas accesses the protected areas (including read, write or erase operations).

33.3 Flash Registers

33.3.1 FLA_CR (0x85)

Bit	7	6	5	4	3	2	1	0
Name	RSV			FLAERR	FLAACT	RSV	FLAERS	FLAEN
Type	-	-	-	R/W	R/W	-	R/W	R/W
Reset	-	-	-	0	0	-	0	0

Bit	Name	Description
[7:5]	RSV	Reserved
[4]	FLAERR	Programming Error Flag 0: Programming or pre-programming succeeds. 1: Programming or pre-programming fails.
[3]	FLAACT	Flash Erase/Write Trigger A write of “0” has no effect and a write of “1” starts Flash operations, including programing, sector erase, etc.
[2]	RSV	Reserved
[1]	FLAERS	Erase Enable 0: Disable 1: Enable Note This bit works only when FLA_CR[FLAEN] = 1.
[0]	FLAEN	Programming Enable 0: Disable 1: Enable Note FLA_CR[FLAERS] works only when this bit is set to “1”.

33.3.2 FLA_KEY (0x84)

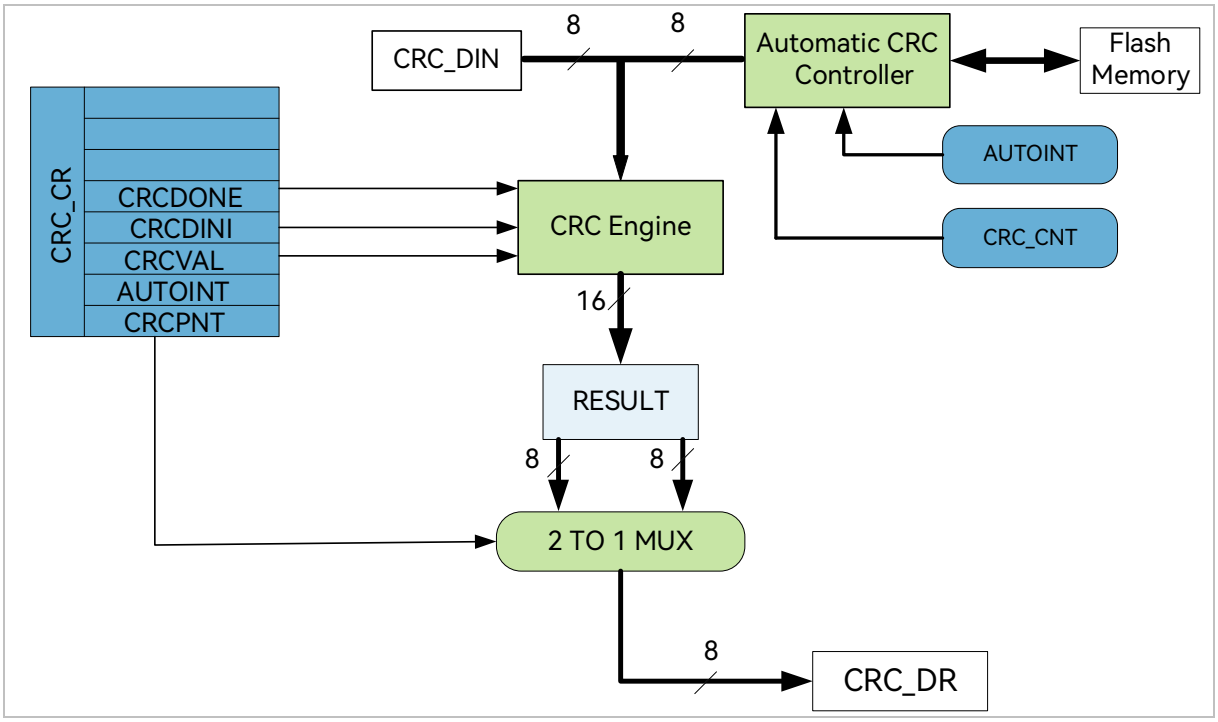
Bit	7	6	5	4	3	2	1	0
Name	FLA_KEY							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	FLA_KEY	Flash Erase/Write Release The Flash software programming feature is activated after “0x5A” and “0x1F” are written to register FLA_KEY in sequence. If the sequence is incorrect or other values are written, Flash space is frozen until the next reset. After unlocking, any write to the FLA_CR register causes the FLA_KEY to be locked again. Read: The lowest 2 bits reflect internal status, and 6 high-order bits obtains 0x00: 00: Locked 01: 0x5A is written, waiting for 0x1F 10: Frozen 11: Unlock

34 CRC

34.1 CRC Functional Block Diagram

Figure 34-1 CRC Functional Block Diagram



CRC module outputs the result of CRC calculation for any 8-bit data based on a fixed polynomial. As shown in Figure 34-1, CRC receives the 8-bit data from CRC_DIN and sends the 16-bit result to the internal register after the calculation is completed. The result can be indirectly accessed through CRC_CR[CRCPNT] and CRC_DR.

34.2 CRC16 Polynomial

The chip uses CRC16/CCITT-FALSE polynomial.

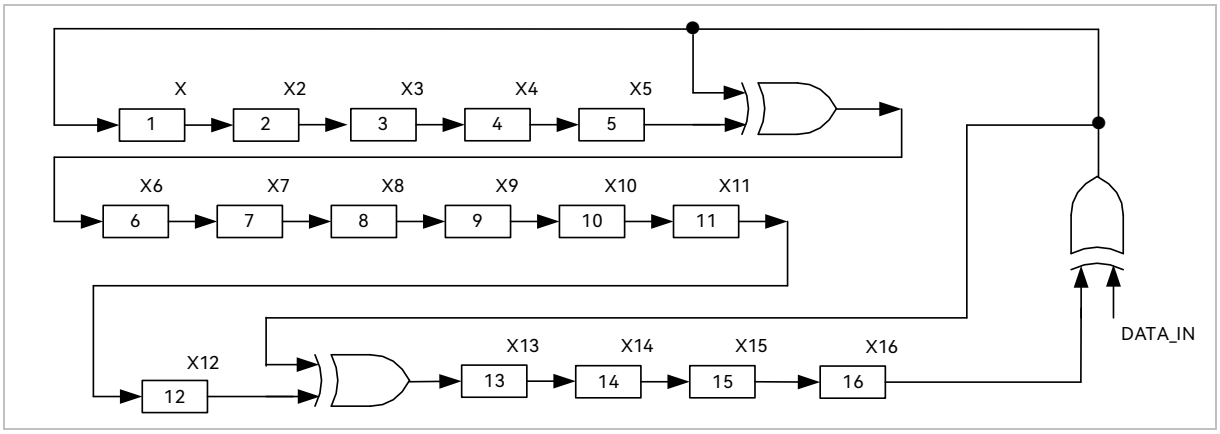
Table 34-1 CRC Criteria and Polynomial

CRC Criteria	Polynomial	Hexadecimal Representation
CRC16-CCITT-FALSE	x^16+x^12+x^5+1	0x1021

34.3 CRC16 Logic Diagram

The schematic diagram of CRC16 is shown in Figure 34-2. The chip implementation is based on parallel algorithm. For each input byte, MCU calculates the results within one system clock cycle.

Figure 34-2 CRC16 Schematic Diagram



34.4 CRC Operations

34.4.1 CRC Calculation of Single Byte

CRC of a single byte is calculated as follows:

1. Initialize CRC_DR with two options: Configure CRC_CR[CRCVAL] and set CRC_CR[CRCDINI] to “1”, with an initial value of 0x0000 or 0xFFFF. Or configure CRC_CR[CRCPNT] and CRC_DR, where any initial value can be set.
2. Write data (0x63 for example) to CRC_DIN, and the CRC calculation is completed in the next clock cycle;
3. Read CRC results: Configure CRC_CR[CRCPNT] = 1, and read CRC_DR in software to get the high bytes. Configure CRC_CR[CRCPNT] = 0, and read CRC_DR to get the low bytes.

34.4.2 CRC Calculation of ROM Sector

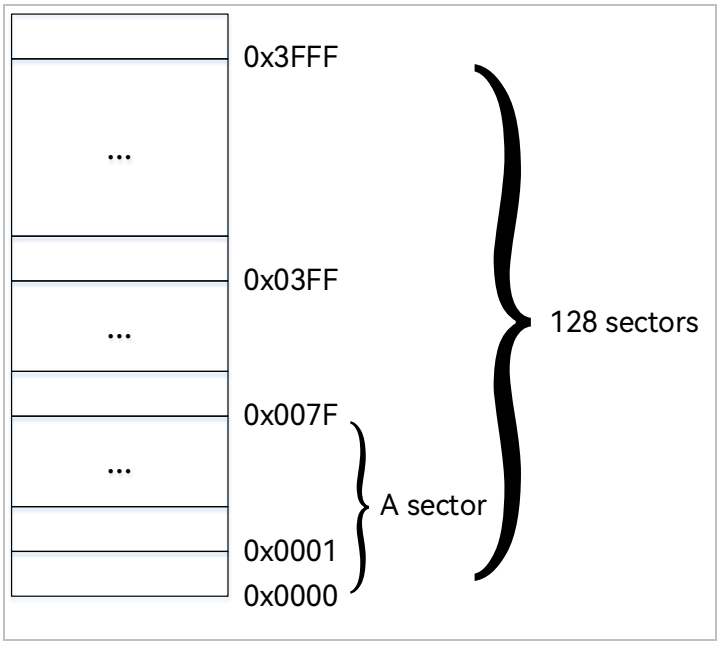
CRC of a continuous area of data in the ROM is calculated as follows:

1. Initialize CRC_DR in the same way as that of single-byte CRC calculation;
2. Configure CRC_BEG to define starting sector of the ROM to be calculated;
3. Configure CRC_CNT to set the offset from the starting sector to the ending sector;

4. Write “1” to CRC_CR[AUTOINT] and keep other bits unchanged. The calculation starts automatically;

5. Read the CRC results in the same way as that of single-byte CRC calculation.

Figure 34-3 ROM Sectors



As shown in Figure 34-3, ROM contains 16k bytes and is divided into 128 sectors, numbered from sector0 to sector127. Each sector contains 128 bytes. For CRC calculation of sectors, the value of CRC_BEG (the starting sector) can be any value falling between 0x00 and 0x7F, including 0x00 and 0x7F. The CRC_CNT (total number of sectors to be calculated) can be any value between 0x00 ~ 0x7F, including 0x00 and 0x7F.

As CRC_BEG increases, CRC_CNT decreases accordingly. For example, if CRC_BEG is 0x7F, CRC_CNT can be 0x00 only, i.e., the CRC value of the data in the last sector is calculated. In this case, if CRC_CNT is set as 0x01 or larger, CRC controller will automatically limits the number of sectors to be calculated. Finally, CRC module only calculates CRC value of the last sector.

34.5 CRC Registers

34.5.1 CRC_CR (0x4022)

Bit	7	6	5	4	3	2	1	0
Name	RSV			CRCDONE	CRCDINI	CRCVAL	AUTOINT	CRCPNT
Type	-	-	-	R	R/W	R/W	R/W	R/W
Reset	-	-	-	1	0	0	0	0

Bit	Name	Description
[7:5]	RSV	Reserved
[4]	CRCDONE	CRC Sector Calculation Completion Flag During the calculation, this bit is automatically set to “0” and the software program stops. In other cases, this bit is automatically set to “1” by the hardware, so the software always returns “1” when reading this bit.
[3]	CRCDINI	CRC Result Initialization Trigger 0: No effect 1: CRC result initialization is triggered. When “1” is written to this bit by software, the hardware does not actually write “1” to this bit but synchronously generates a high level pulse of a clock cycle, which is sent to CRC engine for the initialization of CRC results. Therefore, it always returns “0” when it is read, no matter what value is written by the software.
[2]	CRCVAL	CRC Result Initialization Selection 0: CRC result is initialized to 0x0000. 1: CRC result is initialized to 0xFFFF.
[1]	AUTOINT	CRC Sector Calculation Launch A write of “1” to this bit launches CRC batch calculation with CRC_BEG as the start block. A total of CRC_CNT blocks are to be calculated. Note Other bits shall be configured first. In other words, this bit cannot be configured at the same time as other bits.
[0]	CRCPNT	CRC Result Pointer 0: Read CRC_DR to access 8 low-order bits (7-0 bits) of the 16-bit CRC result 1: Read CRC_DR to access 8 high-order bits (15-8 bits) of the 16-bit CRC result

Note

CRC calculation can be performed on single byte or ROM sector. When CRC_CR[AUTOINT] is set to “1”, ROM sector CRC calculation is implemented. When CRC_CR[AUTOINT] is set to “0”, single-byte CRC calculation is implemented.

34.5.2 CRC_DIN (0x4021)

Bit	7	6	5	4	3	2	1	0
Name	CRC_DIN							
Type	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	CRC_DIN	CRC Input Data Each time a data frame is written to this register, CRC module automatically calculates a new CRC result based on the existing CRC result, and overwrites the original one. Note It is a virtual register, so the written data is not saved. 0x00 is returned when the address is accessed.

34.5.3 CRC_DR (0x4023)

Bit	7	6	5	4	3	2	1	0
Name	CRC_DR							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
[7:0]	CRC_DR	CRC Result Output Each time this register is read or written, the configuration of CRC_CR[CRCPNT] determines whether to access the 8 high-order or the 8 low-order bits of the CRC result.

Note

Because the value of this register can be changed by other signals, this register is placed directly inside the CRC module, instead of register-specific module.

34.5.4 CRC_BEG (0x4024)

Bit	7	6	5	4	3	2	1	0
Name	RSV	CRC_BEG						
Type	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	0	0	0	0	0	0	0

Bit	Name	Description
[7]	RSV	Reserved

[6:0]	CRC_BEG	First ROM Sector Pending Automatic CRC Calculation Example: If CRC_BEG is set to “1”, CRC calculation starts from location 1*128 = 128, or rather from the first byte of sector 2.

34.5.5 CRC_CNT (0x4025)

Bit	7	6	5	4	3	2	1	0
Name	RSV	CRC_CNT						
Type	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	0	0	0	0	0	0	0

Bit	Name	Description
[7]	RSV	Reserved
[6:0]	CRC_CNT	Offset of Sector Pending Automatic CRC Calculation This bit defines the offset of ROM sector for CRC calculation and determines the last sector pending CRC calculation.

35 Sleep Mode

35.1 Introduction

The chip operates in three modes: normal mode, standby mode and sleep mode. These modes are selected by setting PCON[IDLE] and PCON[STOP]. The operating states of the module under different power modes are summarized as below.

Table 35-1 Power Consumption Modes

Power Mode	Description	Wakeup Source	Power Consumption Performance
Normal	All modules work at full speed except for peripherals that are disabled	NA	High power consumption with best performance
Standby	CPU clock is controlled by an electronic gate and other functional modules are either enabled or disabled depending on their control bit setting. WDT is controlled by an electronic gate.	Any interrupt Reset/Debug on external interrupt	Low power performance with flexible performance
Sleep	The analog fast clock circuit is disconnected and software shall ensure that ADC, FOC, and driver modules are idle before the chip enters the Sleep Mode. WDT is disabled.	External interrupt, RTC interrupt, Reset/Debug on external interrupt	Extremely low power performance with flexible performance
	Ultra-low power sleep mode. To enter this mode, PCON[LDOM: STOP] must be configured as 11.	External interrupt, RTC interrupt, Reset/Debug on external interrupt	Extremely low power performance with flexible performance

Note

It is recommended to insert 3 null statements in the Sleep mode.

```
PCON = 0x02;
_nop_();
_nop_();
_nop_();
```

35.2 Sleep Mode Register

35.2.1 PCON (0x87)

Bit	7	6	5	4	3	2	1	0
Name	RSV		GF3	GF2	GF1	LDOM	STOP	IDLE
Type	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	-	0	0	0	0	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5]	GF3	General-purpose flag bit 3
[4]	GF2	General-purpose flag bit 2
[3]	GF1	General-purpose flag bit 1
[2]	LDOM	This bit determines whether the chip enters the ultra-low power sleep mode after it enters the sleep mode. 0: Sleep mode 1: Ultra-low power sleep mode A write of “1” makes the chip enter ultra-low power sleep mode. The hardware automatically clears this bit to “0” after wakeup. Note This bit is valid only when STOP=1, or the chip enters the sleep mode.
[1]	STOP	A write of “1” makes the chip enter the Sleep mode. This bit is automatically cleared to “0” by the hardware after wakeup.
[0]	IDLE	A write of “1” makes the chip enter the Standby mode. This bit is automatically cleared to “0” by the hardware after wakeup.

Power consumption mode PCON[LDOM:STOP:IDLE]:

000: Normal

001: Standby

01X: Sleep

11X: Ultra-low Power Sleep

36 Code Protection

Figure 36-1 Code Protection Configurations

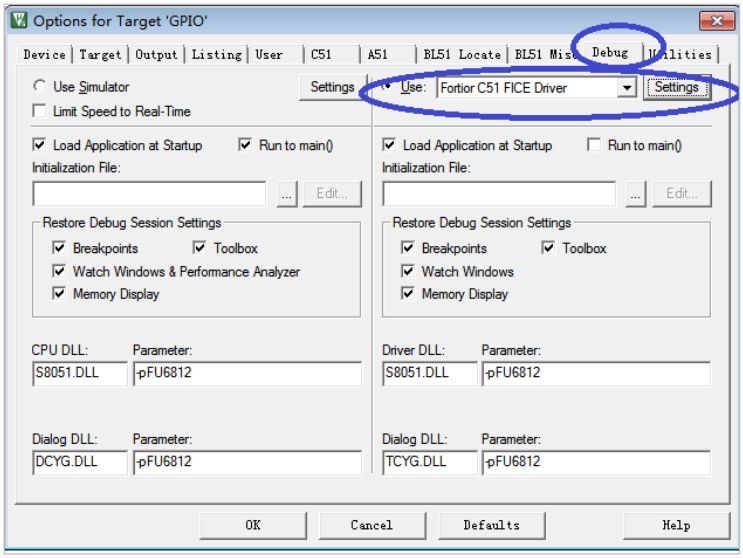


Figure 36-2 Full Code Protection Mode

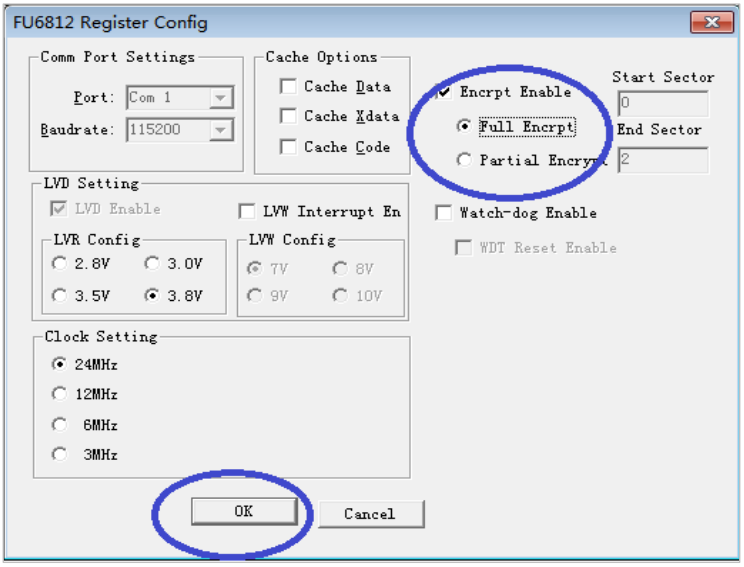
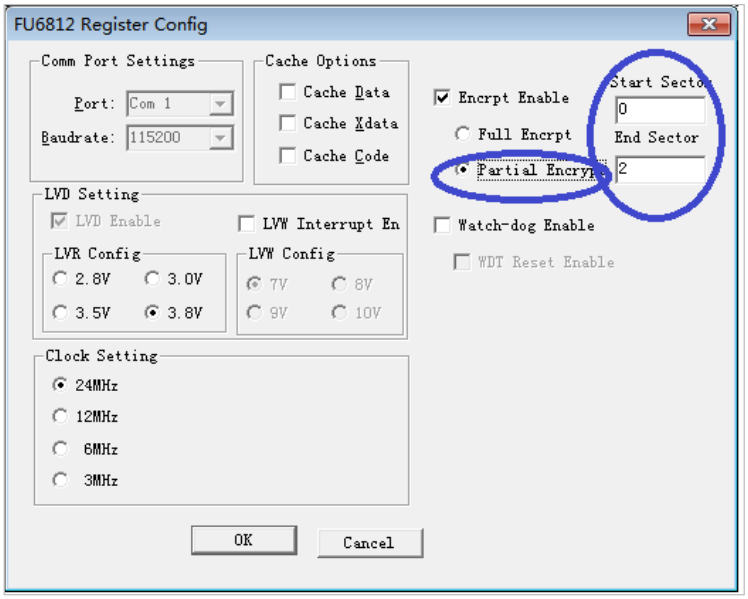


Figure 36-3 Partial Code Protection Mode



The chip supports Flash space encryption to protect your software intellectual property. Operation steps are as follows:

1. Start 8051 IDE, enter Target Options and select Debug tab. As shown in Figure 36-1, click Settings to proceed with the setting;
2. Select the options as shown in Figure 36-2, and click OK. Then compile the project and download it. Get the BIN file and program it to Flash.

The chip support full code protection mode and partial code protection mode. After Full Encrypt is selected as shown in Figure 36-2, all codes in Flash are protected. After Partial Encrypt is selected as shown in Figure 36-3, the codes from sector 0 to END SECTOR are protected. The last sector is always protected in any case.

37 Configuration Registers

37.1 CCFG

37.1.1 CCFG1 (0x401E)

This register can be directly accessed by software. It is recommended that you set these parameters in the IDE, so that you do not have to configure them again in software.

Bit	7	6	5	4	3	2	1	0
Name	LVD_EN_B	LVW_IE	WDT_EN	RSV		FCK_SEL		RSV
Type	R/W	R/W	R/W	-	-	R/W	R/W	-
Reset	0	0	0	-	-	0	0	-

Bit	Name	Description
[7]	LVD_EN_B	LV Reset Detection Enable 0: Enable. The system resets if VDD5 is lower than the threshold voltage set by CCFG2[LVRSEL]. 1: Disable. Note The low voltage detector has two main features: low voltage reset and low voltage warning. The chip is reset when VDD5 is lower than the threshold voltage set by CCFG2[LVRSEL], and LV warning interrupt is generated when VCC is lower than the threshold voltage set by CCFG2[LVWSEL]. The above two features work only after LV Reset Detection is enabled (CCFG1[LVD_EN_B]=0) and LVW Detection Interrupt is enabled (CCFG1[LVW_IE]=1).
[6]	LVW_IE	LVW Detection Interrupt Enable. CCFG2[LVWSEL] decides VCC LV warning voltage threshold. 0: Disable 1: Enable. LV reset detection circuit shall be enabled (i.e. CCFG1[LVD_EN_B] = 0).
[5]	WDT_EN	WDT Enable 0: Disable 1: Enable
[4:3]	RSV	Reserved
[2:1]	FCK_SEL	System Clock Rate Selection 00: 24MHz

		01: 12MHz 10: 6MHz 11: 3MHz
[0]	RSV	Reserved

Note

This register can be directly accessed by software. The recommended practice is to configure it during initialization via the IDE tool. Once set, rewriting in the software is unnecessary

37.1.2 CCFG2 (0x401D)

This register can be configured by IDE only. The register configurations are compiled and merged with ROM_CODE to produce a BIN file for programming. The register can be read by software only.

Bit	7	6	5	4	3	2	1	0
Name	LVRSEL		WDTBTEN	WDTRSTEN	RSV		LVWSEL	
Type	R/W	R/W	R/W	R/W	-	-	R/W	R/W
Reset	0	0	0	0	-	-	0	0

Bit	Name	Description
[7:6]	LVRSEL	Low Voltage Reset Threshold Voltage. VDD5 is detected for the low voltage reset. 00: Low voltage reset is enabled when VDD5 is lower than 2.8V. 01: Low voltage reset is enabled when VDD5 is lower than 3.0V. 10: Low voltage reset is enabled when VDD5 is lower than 3.5V. 11: Low voltage reset is enabled when VDD5 is lower than 3.8V.
[5]	WDTBTEN	1: BOOT is activated when WDT is reset.
[4]	WDTRSTEN	WDT Reset Enable after Overflow 1: WDT is rest after it is overflowed.
[3:2]	RSV	Reserved
[1:0]	LVWSEL	Low Voltage Warning Threshold Voltage. VCC is detected for the low voltage warning. 00: Low voltage warning is enabled when VCC is lower than 7V. 01: Low voltage warning is enabled when VCC is lower than 8V. 10: Low voltage warning is enabled when VCC is lower than 9V. 11: Low voltage warning is enabled when VCC is lower than 10V.

38 Revision History

Rev.	Description	Date	Prepared By
V1.4	First release, translated from Chinese version 1.4.	2023/02/14	Leslie Shi/ Lydia Zhu
V1.5	1. Deleted descriptions on LQFP32_7x7; 2. Updated section 1.1 Features; 3. Updated section 1.2 Applications; 4. Updated section 1.3 Overview; 5. Updated section 1.4 Functional Block Diagram; 6. Updated section 1.5.4 XSFR, and added descriptions on (0x0328~0x03f8) SMDU; 7. Separated Table 2-9 FU6862L LQFP48/FU6862Q QFN48 Pin Descriptions as Table 2-8 FU6862L LQFP48 Pin Descriptions and Table 2-9 FU6862Q QFN48_38 Pin Descriptions; 8. Updated descriptions on section 2 Pin Definitions; 9. Updated Figure 2-9 FU6862L LQFP48 Pinout Diagram; 10. Updated chapter 4 Ordering Information; 11. Updated chapter 5 Electrical Characteristics and separated sections by chip models; 12. Modified “fcpu_clk” as “SYS_CLK” in chapter 10 UART; 13. Rewrote chapter 14 SMDU; 14. Corrected the sampling points in section 15.1.8.2 Dual/Triple-shunt Current Sampling Mode; 15. Updated descriptions in section 15.2.6 FOC_TRGDLY (0x40A5); 16. Modified the bit name “T1RUIE” in section 16.4.6 TIM1_IER (0x406D) as “T1ROIE”; 17. Added Note to Table 38-1 Mapping between Clock Rate and TIMx_CR0[TxPSC]; 18. Updated 24.3.3 ADC_SCYC={ADC_MASKH[7:4],ADC_SCYCL) (0x4036[7:4],0x4038); 19. Deleted “Flash Deep Sleep” in Table 34-1 Power Consumption Modes;	2023/04/28	Eric Deng

	20. Corrected wrong sentences and grammar mistakes; 1. Standardized document format.		
V1.6	1. Updated section 1.1 Features; 2. Updated section 1.4 Functional Block Diagram; 3. Updated descriptions on section 2 Pin Definitions; 4. Updated chapter 3 Package Information; 5. Modifies the number of operational amplifier of FU6862L/ FU6862Q as “3” from “1” in chapter 4 Ordering Information, and modified the number of comparator as “2” from “4”; 6. Updated section 5.8 Operational Amplifier Electrical Characteristics; 7. Modified the test condition “VCC = 7V ~ 30V” of VDD5 voltage in section 5.12 LDO Electrical Characteristics as “VCC = 7V ~ 24V”; 8. Corrected “The chip includes an interrupt system with a total of 15 interrupt sources” as “The chip includes an interrupt system with a total of 16 interrupt sources” in section 7.2 Interrupt Summary; 9. Corrected “When MDU_CR[MDUMOD] = 010, SMDU module works in the 16-bit signed multiplication mode” as “When MDU_CR[MDUMOD] = 001, SMDU module works in the 16-bit signed multiplication mode” in section 14.2.3 16-bit Signed Multiplication; 10. Modified the bit name “SPWMSEL” as “RSV” in section 15.2.1 FOC_CR1 (0x40A0); 11. Updated section 20.1.4 6N Pre-driver Mode; 12. Updated section 23 IO; 13. Updated chapter 26 DMA; 14. Modified “FU6812x2/61x2 integrates three high-speed independent operational amplifiers.... FU6812N/S and FU6861N/NF integrates one operational amplifier AMP0” As “FU6812x2/61x2/62 integrates three high-speed independent operational amplifiers... FU6812N/S and FU6861N/NF integrates one operational amplifier AMP0” in chapter 29 Operational Amplifier; 15. Proofread the overall document and standardized document format.	2023/11/22	Eric Deng
V1.7	1. Corrected the number of ADC channels of FU6812S2 from “5”	2024/05/14	Eric Deng

	to “6”; 2. Added descriptions on Clk feature of I²C for P0.1 of FU6862L and FU6862Q; 3. Updated the sequence of P0.6 pin names in section 2 Pin Definitions; 4. Added INT0 input to the descriptions of P1.1; 5. Updated package information of QFN40_5X5 and SSOP24_8.65X3.9; 6. Corrected the number of GPIOs of FU6812V from “12” to “13” in section 4 Ordering Information; 7. Added the parameter “Operating Ambient Temperature T_A” in section 5.2 Global Electrical Characteristics; 8. Updated descriptions in section 7 Interrupt, 9 SPI, 10.1 UART Introduction ~ 10.2.5 UART Interrupt Sources, 12.1 PI Introduction, 14.2.6 SMDU LPF, 17.1 Timer2 Instructions ~ 17.1.8 Step Mode; 9. Corrected the number of GPIOs in section 23.1 IO Introduction; 10. Modified the name of bit [15:12] in section 24.3.2 ADC_MASK = {ADC_MASKH,ADC_MASKL} (0x4036 ~ 0x4037), and added descriptions; 11. Deleted section 24.3.3 ADC_MASKH(0x4036); 12. Modified some wrong descriptions and sentences; Standardized the document format.		
V1.8	Added the Max. and Min. of VHALF in section 5.7 VREF and VHALF Electrical Characteristics	2025/03/11	Freya Fu
V2.0	1. Updated standard format V2.0 2. Added model FU6872P; 3. Modified DAC as 9-bit DAC; 4. Deleted CMPXO to P0.7; 5. Divided SPI and UART according to types in 1.1 Features; 6. Modifeid 7 Interrupt; 7. Added descriptions of polling speed selection to CMPG; 8. Reviewed some other mistakes before.	2025/10/24	Freya Fu

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